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Heterogeneous Integration and Fabrication of III-V MOS Devices in a 200mm Processing Environment

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We report on the fabrication of MOS capacitors on 200 mm virtual GaAs substrates using a Si CMOS processing environment. The fabricated capacitors were comparable to those processed on bulk GaAs material. Topside contact was made to the GaAs using a novel CMOS compatible self-aligned NiGe contact scheme resulting in a measured contact resistance of 0.26 Ω.cm. Cross-contamination from various III-V substrates was investigated and it was found that by limiting the thermal budget to ≤ 300 ˚C cross-contamination from the outgassing of In, Ga and As could be eliminated. For wet processing the judicious choice of recipe and processing conditions resulted in no significant cross-contamination being detected as determined by TXRF monitoring. This achievement enables III-V device production using state-of-the-art Si processing equipment.

Introduction

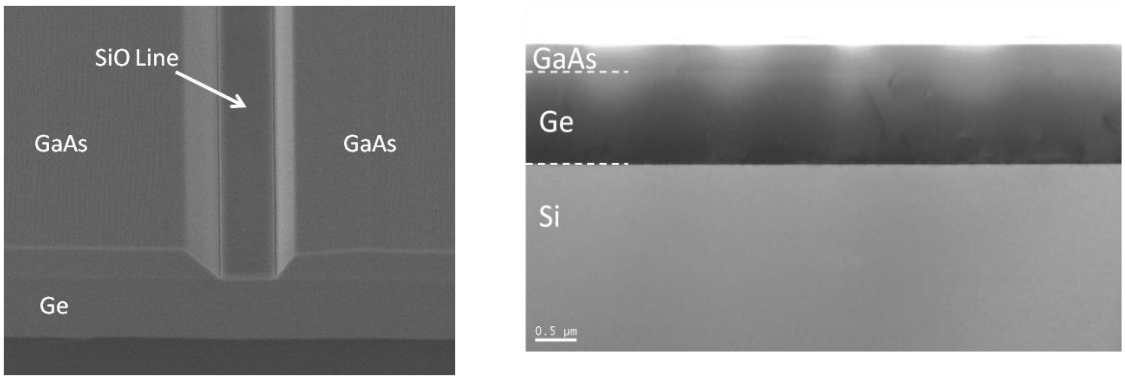
As CMOS scales beyond the 16 nm node it is widely expected that new higher mobility channel materials will have to be introduced as an alternative to Si in order to meet power and performance requirements [1]. III-V and Ge materials have emerged as an attractive option for nMOS and pMOS respectively by virtue of their high electron or hole mobility. However, there are a number of challenges associated with introducing III-V materials for VLSI. The most pressing of these issues include the need to find suitable passivation methodologies for the gate stack [2] and the growth and processing of III-V material on 300 mm or even 450 mm wafers. From an economical and technological standpoint it is required to implement III-V devices on such large scale wafers in a Si CMOS fabrication environment in order to leverage the advantages of state-of-the-art Si equipment. The integration challenges of introducing III-V semiconductor compounds into a Si line include safety risk assessments from toxic materials, maintenance of tools after processing III-V wafers, cross-contamination from high-temperature and wet etch steps, and modifying standard recipes where III-V is exposed on the surface.

Ultimately the architecture of a III-V MOS device is likely to be a planar or finfet version of an implant free quantum well (IFQW) with an InGaAs based channel [3,4]. Such an approach will require the selective growth of III-V heterostructures and also Ge layers in small active areas to provide a CMOS solution. One promising technique for this approach is the use of the aspect-ratio-trapping technique and Ge buffer engineering [5,6]. However, the main goal of this work is to demonstrate the feasibility of processing III-V virtual substrates in a Si line following a CMOS based approach in which any potential cross-contamination from the III-V is minimized. Therefore, for simplicity we have used n-type capacitors fabricated on virtual 200mm GaAs substrates as our test vehicle. The results obtained from this work help us to identify and debug the potential issues of processing III-V materials in a Si CMOS environment and allow us to establish a path to production for large scale III-V device wafers.

Substrate Preparation and Device Fabrication

GaAs Substrate Preparation

The 200mm virtual GaAs substrates were grown using a Crius Close-Coupled Showerhead MOCVD system from AIXTRON [7]. First a Germanium-on-Si (GOS) template was prepared by epitaxially growing a 1 μm strain relaxed Ge layer on a Si (100) wafer in a separate CVD reactor [8]. Miscut wafers (6° off-orientation toward <111>) were used in order to avoid the formation of anti-phase domain (APD) boundaries. Use of an intermediate Ge buffer layer allows for the lattice mismatch between the Si substrate and GaAs to be almost completely accommodated. After a NH_4OH/H_2O_2 pre-clean the GOS substrates are loaded in the reactor and a 300 nm layer of n-type doped GaAs was grown. Details of the GaAs growth are reported elsewhere [9]. 300 nm thick n-doped GaAs material was grown as a blanket layer and also selectively in islands on the GOS. For the selective GaAs growth a SiO grid pattern was processed on top of the Ge surface resulting in the definition of 200 μm x 1200 μm windows. An XSEM and TEM of the selective growth is shown in Fig. 1. Few defects were seen in the GaAs layer and the corresponding TDD is not believed to be higher than that of the underlying Ge at $\leq 10^8$ cm^{-2}. The RMS roughness was measured by AFM to be 1.2 nm. The n-type Si doping level determined by SIMS was $9x10^{16}$ cm^{-3} (Fig 2). From the SIMS analysis it can be seen that the Ge from the underlying layer readily diffuses into GaAs layer to a depth of about 100nm. Fig. 3 shows an excellent within-wafer thickness uniformity (<2%); in addition, a good wafer-to-wafer distribution (not shown). Both are requirements for standard large scale Si manufacturing.



(a) (b)

Figure 1: (a) Tilted cross-section SEM view of GaAs grown selectively on a SiO2-patterned 6° miscut GOS template and (b) normal TEM view of the GaAs layer. The oxide line is 1 µm wide.

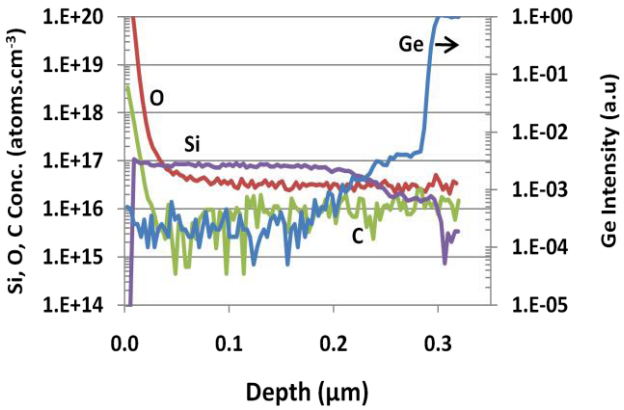


Figure 2: SIMS profile of Si, O, C and Ge in the GaAs layer. Ge concentration is not calibrated.

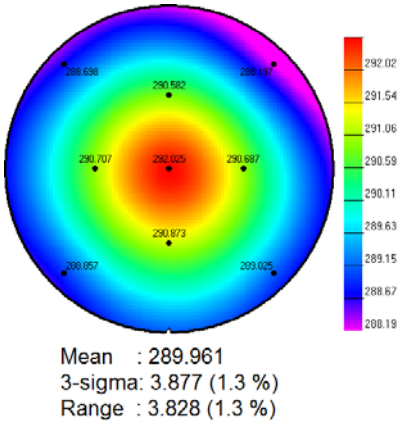
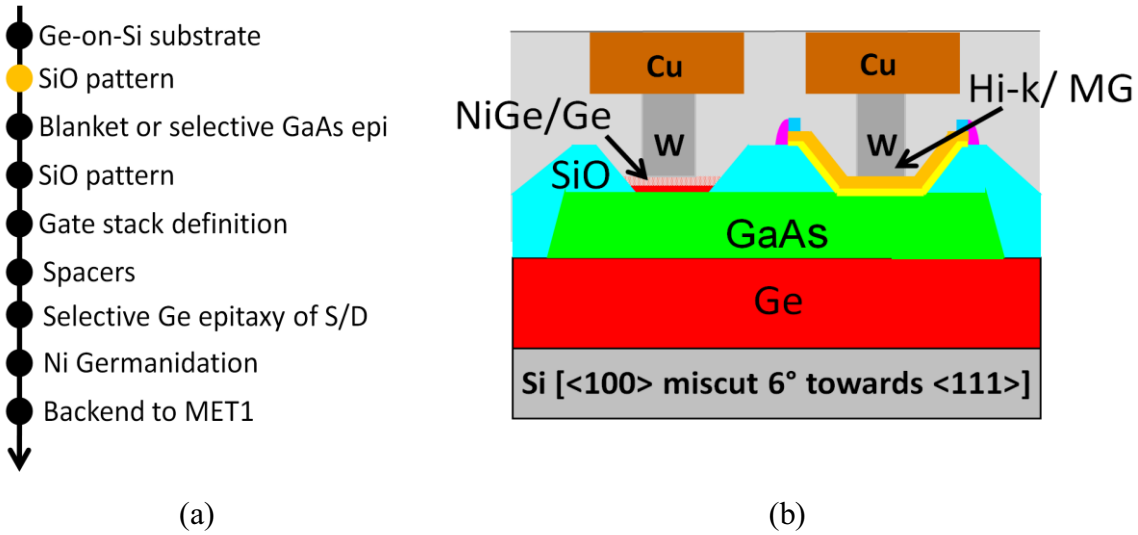


Figure 3: Wafer map of GaAs thickness uniformity on 200mm GOS substrate.

Capacitor Process Flow

After the GaAs substrates were prepared capacitors were fabricated in our 200mm Si pilot line following the flow outlined in Fig. 4. First a 350 nm layer of CVD SiO is deposited on the GaAs. Active areas are defined in the oxide layer by etching windows in the SiO by means of HF 0.5% wet etch. Immediately after this wet etch the wafers were loaded in an ALD reactor and 4nm of Al_2O_3 was deposited. A gate metal of 10 nm TiN was used and the gate stack was completed by the deposition of 80 nm SiO as a hard mask. The gate stack was then patterned with the dry etch stopping on the high-κ layer. The Al_2O_3 was removed by Imec-Mixture (0.03M HF/10% HCl @55°C). Spacers were defined with a 10 nm SiO liner and 60 nm SiN layer. Topside contact is made to the GaAs by a novel self-aligned Ge/NiGe scheme which is discussed in more detail in a later section. Device fabrication is completed by standard a W contact plug and Cu Metal 1 processing.

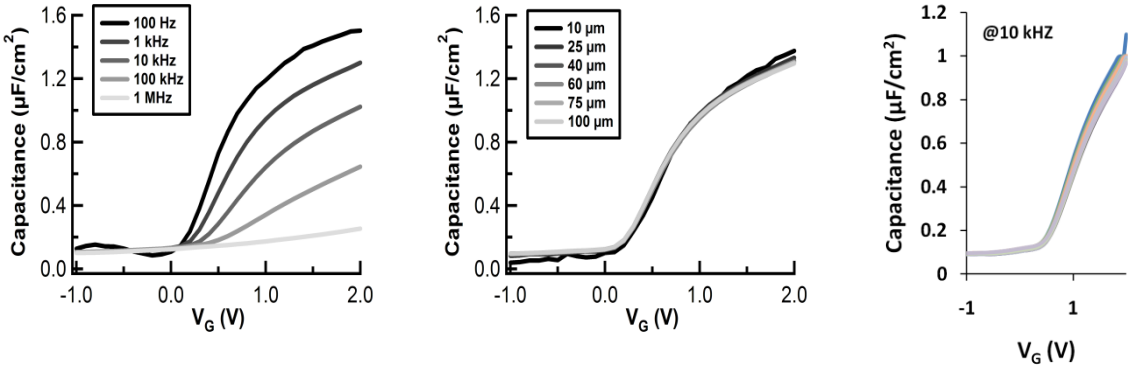


(a) (b)

Figure 4: (a) Description of GaAs capacitor process flow in 200mm Si line (b) schematic of capacitor structure.

C-V Characterization

In order to evaluate the quality of the GaAs layer and gate stack, the fabricated capacitors were characterized by means of capacitive-voltage (C-V) measurements. C-V curves of a 100x100 μm^2 capacitor are shown in Fig. 5 (a) for the blanket GaAs layer. No significant differences between the C-V characteristics of the blanket or selective layers were observed. The extracted electrical oxide thickness (EOT) of 2 nm is consistent with the deposited high-k thickness. The frequency dispersion is typical of GaAs capacitors without a Gd_2O_3 interface layer or S passivation [10]. This 100x100 μm^2 capacitor was measured at 30 sites across the wafer and was found to be repeatable (Fig. 5b). Test structures of different areas were also measured and the capacitance was found to be scalable (Fig. 5c). The leakage through the gate stack was measured across wafer and an average value of 0.1 A/cm^2 at a gate bias of 1V was found to be typical for the 4nm Al_2O_3 thickness (Fig 6). Again no observable differences were noted between the blanket and selectively grown GaAs. The interface trap density (D_{it}) was extracted from C-V measurements carried out at 25 °C and 150 °C. Interface trap densities on the order of mid $10^{12}/eVcm^2$ values were measured close to the conduction band which then increases towards the midgap. This D_{it} profile is very consistent with those we have previously measured on bulk GaAs samples with a similar passivation treatment [11] (Fig. 7).



(a) (b) (c)

Figure 5: (a) C-Vs curve of 100x100 μm^2 capacitor on blanket GaAs at multiple frequencies, (b) C-V curves of different area capacitors at a frequency of 1 kHz and (c) cross-wafer C-V curves of the 100x100μm^2 capacitor.

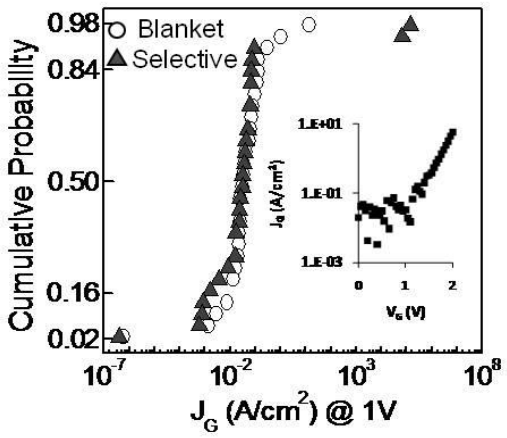


Figure 6: Normal probability distribution of plot of J_G @1V for selective and blanket GaAs wafers. Inset shows typical J-V curve

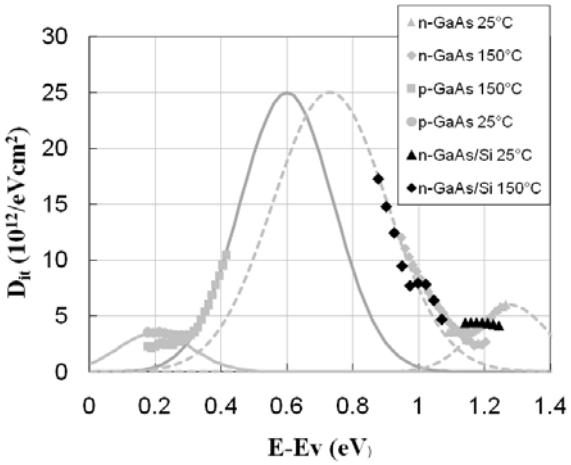


Figure 7: Extracted D_{it} from the 200mm GaAs capacitors process on selective GaAs compared to data from bulk GaAs

Self-aligned Ge/NiGe Contact Scheme

For the topside contact in this work we developed a self-aligned Ge/NiGe scheme. The most common contact schemes for III-Vs are non self-aligned and Au based which are incompatible with VLSI processing. The equivalent of the CMOS salicide process does not typically exist for III-V although recent results from the literature show that a direct Ni reaction with InGaAs is promising for self-aligned contacts [12]. For this work with GaAs we take advantage of the fact that the Ge and GaAs conduction bands are closely aligned. By selectively depositing highly doped n-Ge on GaAs and utilizing a selective

Ni germanide process that was previously developed for advanced Ge devices [13] we are able to realize low resistance self-aligned ohmic contacts.

The Ge CVD growth process was developed on 2" bulk GaAs semi-insulating substrates. An optimized in-situ n-Ge growth process which is described elsewhere [14] resulted in a high quality epitaxial layer. 3D (three dimensional) islanding which was reported by other groups [15,16] was avoided and 2D layers as thin as 7 nm were achieved (Fig. 8a). TOF-SIMS of the 7nm Ge layer showed Ga and As segregation into the Ge layer (Fig 8b). An electrically active p-type concentration as high as $1x10^{19}$ cm^{-3} was measured in the Ge as a result of the autodoping from the GaAs substrate. This p-type doping is problematic for the formation of n-type contacts on GaAs as a p-n junction is formed at the interface. To counteract this autodoping effect the Ge was heavily n-type doped by adding PH_3 in the growth step. An n-type doping of $3x10^{19}$ cm^{-3} was thus achieved. CTLM test structures were fabricated on n-GaAs test wafers to evaluate the contact resistance achievable using this n-doped Ge layer. The CTLM pattern was first defined in an oxide layer on n-GaAs substrates. Ge was selectively grown on the wafers and this was followed by a selective Ni-germanide process. A contact resistance of 0.26 Ω.cm was measured (Fig. 8c). For the 200mm GaAs wafers, 40 nm of n-type Ge was selectively grown followed by a 10 nm Ni deposition for the selective Ni germanide process. This Ge/NiGe process was confirmed to be selective to the SiN spacer (Fig. 9a). As expected from the results of 2" substrates, ohmic contact behaviour was observed from the I-V curves (Fig. 9b).

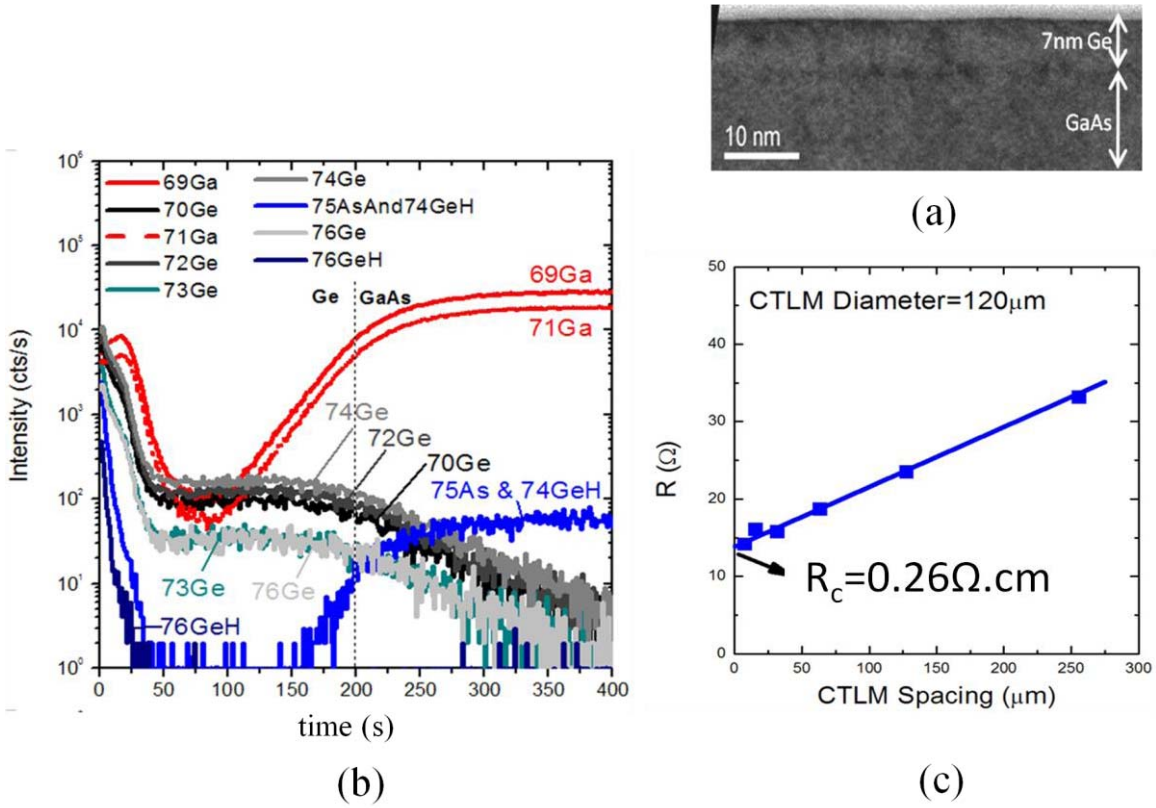
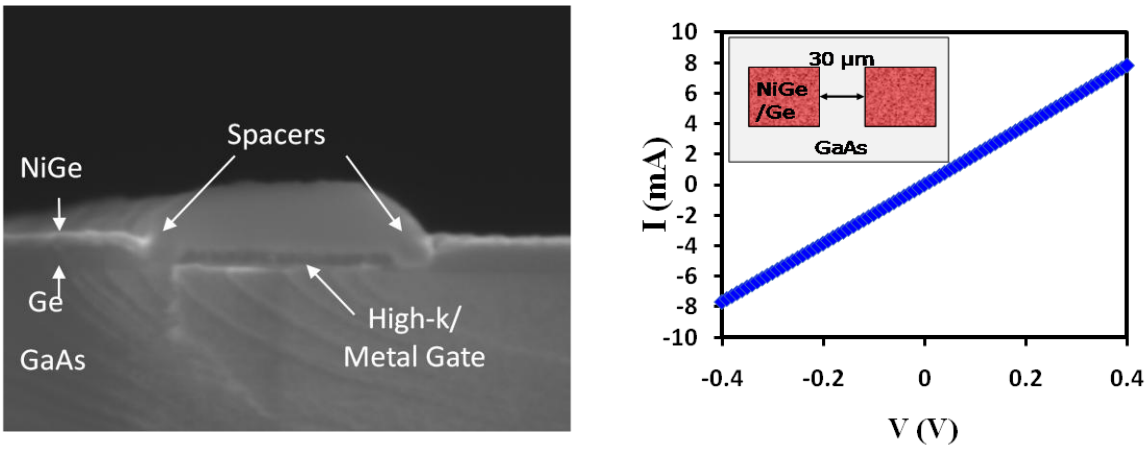


Figure 8: (a) TEM cross section view of ultrathin 7 nm Ge layer grown on GaAs show the layer is continuous and (b) TOF-SIMS of the 7 nm Ge layer. As and Ga are detected within the first few Ge top surface monolayers. (c) CTLM measurement of the contact resistance of the Ge/NiGe using a 40 nm Ge layer on n-GaAs substrates



(a) (b)

Figure 9: (a) Cross-sectional SEM of a GaAs capacitor with self-aligned Ge/NiGe contacts and (b) I-V characteristics of the ohmic contacts on the n-GaAs substrate.

Cross contamination

Within-wafer and tool cross-contaminations are expected from III-V materials when they are integrated in a Si process flow. This can pose problems for Si wafers subsequently processed in the tool or even Si or Ge active areas on the same wafer as In, Ga and As are dopants of these materials. Also from an environmental, health and safety (EHS) perspective it is important to be aware if a tool or the waste products from a tool are contaminated with In, Ga or As as these materials and their related compounds can be toxic. Extra safety procedures will then need to be implemented for tool maintenance and waste disposal. In this work we have investigated the cross-contamination risk for both the thermal and wet processing steps used in the integration flow and propose guidelines to minimize this risk.

Thermal processing

First, the risk of cross-contamination from the thermal processing of a GaAs, $In_{0.53}Ga_{0.47}As$ or InP layer was investigated by use of 2" test wafers. The test wafers (GaAs, InP and 30nm $In_{0.53}Ga_{0.47}As$ on GaAs) were sandwiched between two 200mm B-doped Si wafers. The Si wafers received an HF-last clean before the experiment. These wafer stacks were then annealed from 350 ˚C to 500 ˚C for 10' in an N2 environment. The In, Ga and As concentrations were measured by means of TXRF at 3 points in the centre of the Si wafer and 3 cm next to the contact area of the Si with the test wafer. The level of P contamination could not be measured by TXRF as the detection limit is on the order of 10^{14} atoms/cm^2. As this tool is routinely used for annealing of III-V substrates the background level of each of these contaminants was determined by measuring a bare Si wafer that was annealed in the oven. The results are shown in Fig. 10. In all cases it was found that direct contact resulted in detectable levels of contamination. In the case of gas phase contamination, which is of more concern from a tool perspective, As was found to be the most problematic and outgassed at temperatures ≥ 350°C from GaAs and at ≥ 450°C from InGaAs. In outgassing was detected from InP at temperatures ≥ 450°C. No

In outgassing was detected from InP. Also no Ga outgassing was detected in this temperature range for any substrate.

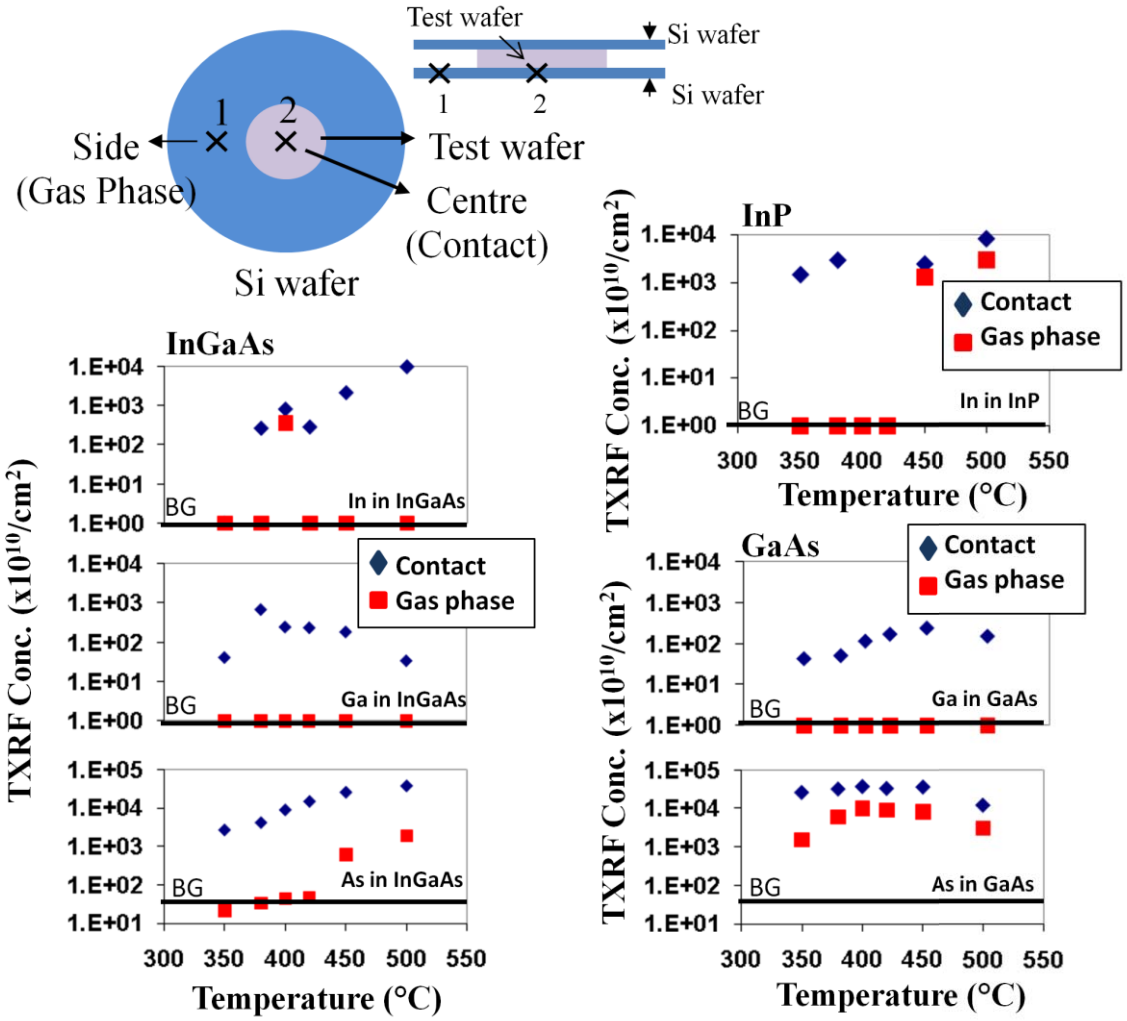


Figure 10: Cross-contamination outgassing test results as measured from 2" InP, GaAs and InGaAs wafers. BG refers to the background level of In, Ga or As measured in the RTA annealing tool. Inset shows the setup of the experiment

Based on these results outgassing experiments were carried out in a 200mm CVD deposition tool. 12x 2" GaAs wafers were processed through the tool with a 350nm SiO layer deposited at 400°C. A Si wafer was processed directly afterwards with a 10nm SiO growth and then measured by Vapor Phase Decomposition Droplet Collection (VPD-DC) TXRF. Noticeably higher levels of As were detected on the Si wafer (Fig. 11). This confirms that contamination caused by III-V processing in the tool can effect subsequently processed wafers. Next 200mm GaAs substrates were processed at a 300°C deposition temperature and it was found that the Ga and As levels did not increase from the background levels in the tool. Testing of InP and InGaAs substrates at the same 300°C deposition temperature also showed no evidence of cross-contamination.

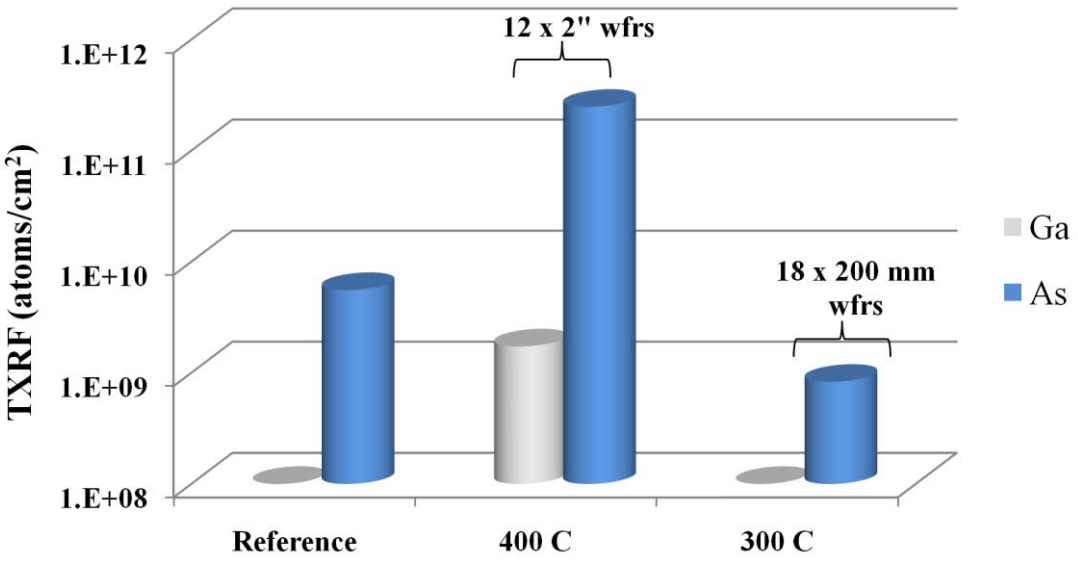


Figure 11: Ga and As outgassing as measured by TXRF from GaAs wafers processed in the 200mm CVD deposition tool. Reducing the deposition temperature from 400 ˚C to 300 ˚C eliminated cross-contamination to the tool from the GaAs wafers.

Wet Processing

Based on our previous work on the etch rates of III-V layers [17] HF 0.5% and Imec-Mixture (0.03M HF/10% HCl @55°C) were chosen for wet etch and clean steps for the 200mm wafers where the GaAs was exposed during processing. The HF0.5% was used for the wet etch to define the active area windows in an SiO layer and the removal of the SiO spacer liner layer. The Imec-Mixture was used for the removal of the high-κ Al_2O_3 layer after gate etch. The etch rate of GaAs test wafers in both these chemicals was determined to be low: 0.14nm/min for HF 0.5% and less than the detection limit of 0.22nm/min for 0.03M HF/10% HCl @55°C. The 200m wafers were processed in a single wafer production tool. TXRF testing of Si test wafers cycled through the acid immediately after the 200mm GaAs wafers were processed showed no increase the levels of Ga and As detected compared to a reference wafer processed before the GaAs lot (Fig. 12a). Ga and As levels were also measured in a 50 ml sample taken from the acid tanks pre and post III-V processing. There was a slight increase noticed in the HF 0.5% but levels were still below 2.5 ppb, while no change was detected for the 0.03M HF/10% HCl @55°C (Fig. 12b).

These results show that cross-contamination from III-V substrates can be minimized by limiting the thermal budget of the process flow, in this case to ≤ 300°C. For wet processing choosing chemicals for etch or clean steps that are known to have very low etch rates of the underlying III-V layer minimizes the dissolution of these compounds into the re-circulated or waste acid.

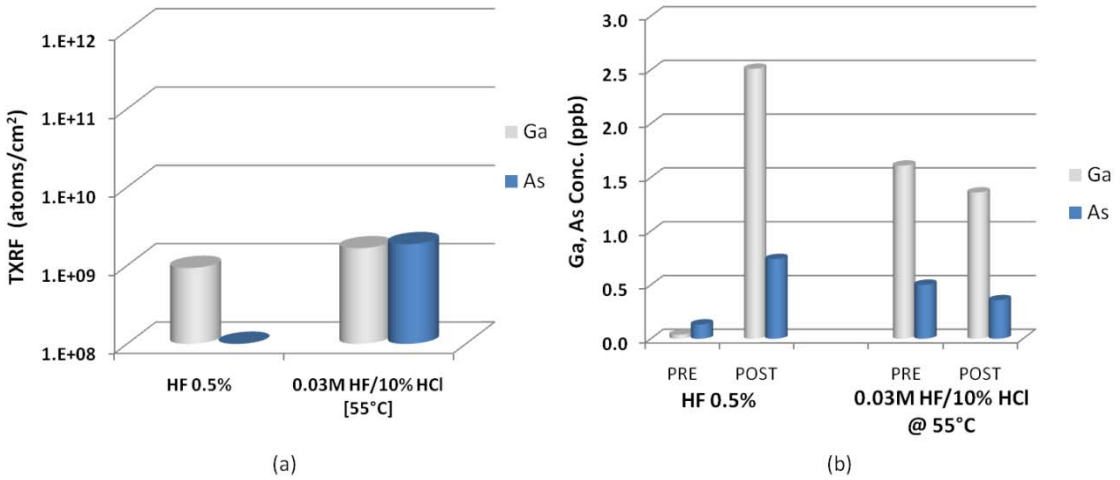


Figure 12: Cross-contamination assessment during wet processing on (a) on Si test wafer processed immediately after GaAs wafers were run and (b) from acid samples

Conclusions

We have demonstrated the feasibility of running III-V substrates in a standard Si CMOS production line. N-type capacitors fabricated on 200mm GaAs virtual substrates showed showed comparable electrical characteristics to those of capacitors processed on bulk GaAs substrates. Topside contact to the GaAs was made with a self-aligned Ge/NiGe scheme. The n-type Ge growth on GaAs was optimized allowing for the growth of highly doped ($3x10^{19}$ cm^{-3}) continuous layers as thin as 7 nm. The contact resistance achieved was 0.26 Ω.cm. We have performed a cross contamination assessment for both thermal and wet processing by means of TXRF monitoring and have outlined guides line that allow processing of III-V materials in a Si environment. We have found that exposed GaAs, InGaAs and InP surfaces do not suffer from any outgassing issues if the thermal processing is carried out at 300 ˚C or below. With the correct choice of chemicals and tools for wet processing the risk of cross-contamination in these steps can be minimized. The results achieved in this work support a path to production for large scale III-V wafers.

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