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Hetrogeneous Integration and Fabrication of III-V MOS Devices in a 200mm Processing Environment

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As CMOS continues to scales to more advanced nodes, new higher mobility channel materials have been considered as an alternative to Si in order to meet power and performance requirements [1]. Various III-V materials have recently emerged as an attractive option for nMOS. However, from an economical and technological standpoint it is imperative to implement III-V devices in a Si CMOS fabrication environment in order to leverage the advantages of both large scale wafers and state-of-the-art Si equipment. The integration challenges of introducing III-V into a Si line include safety risk assessments from toxic materials, maintenance of tools after processing III-V, cross-contamination from high-temperature and wet etch steps, and modifying standard recipes wherever bare III-V materials are exposed during process. In this work we demonstrate the feasibility of processing III-V virtual substrates on a Si platform following a standard CMOS based approach without cross-contamination from the III-V.

The test vehicle used in this study is an n-type capacitor. It is processed in our standard 200mm Si pilot line on virtual 200mm GaAs substrates. These substrates are prepared by growing a 300nm n-type doped GaAs on a Ge-on-Si template (Fig 1). The details of the GaAs growth are described elsewhere [2]. After GaAs epi growth, windows are opened in a deposited oxide and the gate stack is deposited and patterned. Following spacer processing, topside contact to the GaAs is made by a novel self-aligned Ge/NiGe scheme. A contact resistance of 0.13 Ω.cm was achieved using this approach. Device fabrication is completed by standard W contact plug and Cu Metal 1 processing.

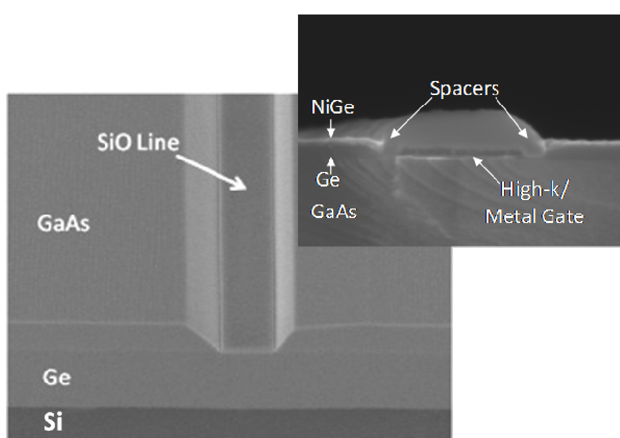

Fig 1: Tilted XSEM view of GaAs selective growth on GOS substrate. Inset shows capacitor structure fabricated on the GaAs layer using a selective Ge/NiGe contacting scheme.

Capacitors ranging in size from 10µm x 10µm to 100 µm x 100 µm were fabricated. The capacitance was found to be scalable and repeatable across the wafer. The CV curves obtained showed a frequency dispersion typical of GaAs capacitors without non-optimzed passivation. The optimization of the surface passivation is the subject of another study. In addition, the interfacial defect density Dit extracted from conudctance measurements, carried out at 25 ˚C and 150 ˚C, were also very consistent with those of bulk GaAs samples previously measured (Fig. 2). This illustrates the intrinsic properties of the 200mm GaAs substrates.

Within wafer and tool cross-contaminations are expected from III-V materials when they are integrated in a Si process flow. In this work we have performed a cross contamination assessment for both thermal and wet processing by means of TXRF monitoring and have outlined guides line that allow processing of III-V materials in a Si environment. We have found that the exposed GaAs surface does not suffer from any outgassing issue if the thermal processing is carried out at 300 ˚C or below. It will also be shown that with the correct choice of chemicals and tools for wet processing the risk of cross-contamination in these steps can be minimized.

In conclusion, 200mm virtual III-V substrates were successfully run entirely through a Si processing line. The resulting electrical results were comparable to those of bulk GaAs. A CMOS compatible contacting scheme was developed. Guidelines have been set up to avoid cross-contamination. The results reported support a path to production for large scale III-V device wafers.

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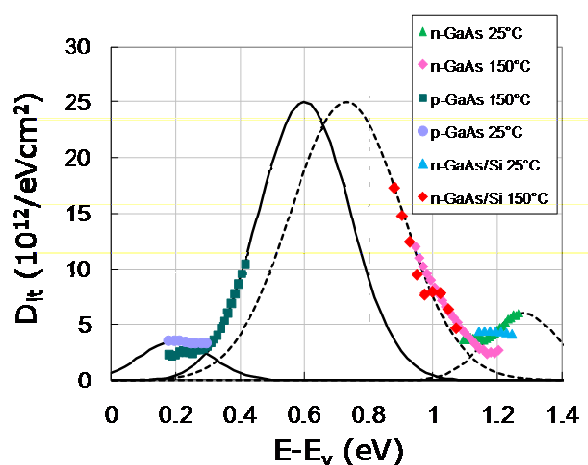

Fig 2: Extracted D_{it} of the fabricated n-type GaAs capacitors measured at 25 ˚C and 150 ˚C compared to those of bulk GaAs samples with a similar passivation treatment.