

Selective epitaxial growth of III-V semiconductor heterostructures on Si substrates for logic applications

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Sub-22 nm high-performance digital circuits based on metal-oxide semiconductor (MOS) devices call for the introduction of high-mobility channel materials such as Ge for pMOS and III-V compounds for nMOS. The successful integration of these semiconductors on Si substrates, which would lead to a cost-effective CMOS manufacturing option, relies on the deposition of thin layers without extended defects. A promising technical solution to the achievement of this task is provided by the selective epitaxial growth (SEG) of the required materials in shallow trench isolation (STI) structures. This approach, based on the extended defect necking effect [1-3], alleviates the large lattice mismatch between the III-V semiconductors and the Si substrate and leads to defect-free regions in the filled STI structure, on which devices can be fabricated. However, additionally to the challenge of hetero-epitaxial growth of a polar semiconductor on a non-polar surface, other issues, related to the generation of undesired stacking faults or twin defects, have to be solved. Furthermore, in the perspective of application in a standard low-cost very-large-scale integration scheme, these high-mobility materials have to be fabricated on large-area Si substrates in order to meet the requirements of the CMOS industry.

In this paper, we report results on the epitaxial growth of III-V layers on 200 mm Si wafers by means of metal-organic chemical vapor deposition (MOCVD). Our processes were developed using a specially designed Crius Close-Coupled Showerhead system from AIXTRON AG [4]. The formation of anti-phase domain boundaries, which lead to strong detrimental effects on the electrical properties of the epilayer, was avoided by the use of off-oriented Si (100) wafers (6° off-orientation towards <111>). Moreover, in our approach, a strain-relaxed epitaxial Ge layer is first deposited on Si and subsequently serves as an intermediate buffer between the substrate and the III-V material. In the case of GaAs, the lattice mismatch between the substrate and the layer is accommodated and, thus, no additional threading dislocation is introduced in the deposited III-V film. In contrast to Si surfaces, the Ge buffer also allows us to work with a reduced thermal budget for the in-situ pre-epi surface clean.

In the first part of this study, we demonstrate that smooth GaAs layers can be epitaxially grown on large-area Si substrates with high wafer-scale thickness uniformity. Photoluminescence spectroscopy and electron microscopy confirmed the excellent quality of the deposited GaAs. Very high selectivity of the growth process was achieved on patterned wafers with an SiO₂ mask. This enabled the fabrication of capacitor structures using an integration process flow very similar to standard

high volume Si manufacturing lines. The capacitance-voltage characteristics were similar to the ones obtained on a bulk GaAs substrate, and showed extremely tight within-wafer and wafer-to-wafer distributions as is standard to Si manufacturing.

In the second part of the paper, we report a detailed investigation of the SEG of InP in STI structures (Fig. 1). After a planarization step, this InP layer serves as a virtual substrate for the subsequent growth of high-electron-mobility channel materials such as the lattice-matched In_{0.53}Ga_{0.47}As ternary compound. The wider band gap of InP also provides a potential barrier which can prevent electrical leakage from the channel to the substrate. We show that the morphology of the InP nucleation layer on the Ge buffer depends on the pre-epi bake ambient conditions and expresses a high sensitivity on the deposition temperature. The impact of the InP seed on the overall quality of the layer grown in the trench was clearly evidenced: a smooth seed layer could lead to the reduction of extended defects and resulted in vertical crystal growth above the STI surface whereas a rougher seed induced distorted overgrowth.

Excellent selectivity of the InP growth with respect to SiO₂ could be demonstrated. However, strong loading effects were observed, irrespective of the growth pressure, leading to local variations of the growth rate. We also studied the formation of crystal facets and of stacking faults, which depends on the trench orientation. By an adequate choice of the latter one with respect to the direction of the substrate off-orientation, stacking faults could be trapped at the bottom of trenches with aspect ratio greater than 2 and extended-defect-free InP material could be obtained in the top region.

We investigated on the epitaxial growth of III-V semiconductor compounds on 200 mm patterned Si wafers. High selectivity towards SiO₂ was demonstrated for GaAs and InP using different mask sets. These results highlight the significant challenges faced by epi process technologists to achieve a successful combination of Ge and III-V materials on one Si substrate, which is key to high performance CMOS devices.

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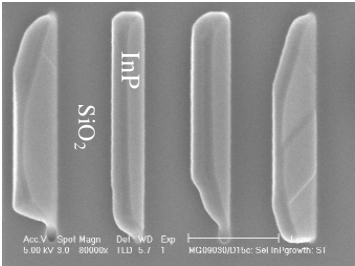


Fig. 1. Top-view scanning electron microscope image of 150 nm wide and 3 μm long InP-filled STI structures on Si (100) substrates with 6° off-cut.