Low-temperature chemical vapor deposition of highly doped *n*-type epitaxial Si at high growth rate

N.D. Nguyen, R. Loo, M. Caymax IMEC, Kapeldreef 75, B-3001 Leuven, Belgium

ABSTRACT

We investigated the growth of in-situ π -type doped epitaxial Si layers with arsenic and phosphorus by means of low-temperature chemical vapor deposition using trisilane as Si-precursor. Indeed, in order to prevent the alteration of the characteristics of the devices which are already present on the wafer, an epitaxy process at low temperature is highly desired for applications such as BiCMOS. In this work, the varying parameters are the deposition temperature, the Si-precursor mass flow and the dopant gas flow. As a result, a process for the deposition of heavily doped epilayers was demonstrated at 600 °C with high deposition rate, which is important for maintaining high throughput and low process cost. We showed that using trisilane as a Si-precursor resulted in a much more linear π -type doping behavior than using dichlorosilane. Therefore it allowed an easier process control and a wider dynamic doping range. Our process is an interesting route for the epitaxy of a low-resistance emitter layer for bipolar transistor application.

PACS: 68.55.ag; 73.61.Cw; 81.05.Cy; 81.10.Bk; 81.15.Gh

Keywords : Si-precursor ; Trisilane ; Growth rate ; *n*-Type doping ; Low-temperature chemical vapor deposition

1. Introduction

Chemical vapor deposition (CVD) with low thermal budget [1] is a key process step in (bipolar) complementary metal oxide semiconductor (CMOS, BiCMOS) technology applications such as epitaxial strained layers for high channel mobility, elevated sources and drains with SiGe [2] and Si:C [3] and emitter layers [4]. For such applications, growth temperatures of 700 °C or lower are desired in order to prevent changing the characteristics of devices which have already been processed on the wafer. However, at low temperature, it is difficult to obtain high growth rates, which are necessary to sustain high throughput and low process cost.

The general trend of enhanced epitaxial growth rates in using higher order silanes is well known, although the microscopic growth mechanisms are not well understood [5]. Agnello et al. showed that low-temperature CVD with dichlorosilane (DCS) and hydrogen as carrier gas leads to a very high dopant concentration. Deposition rate of about 10 nm/min had been obtained at a growth temperature of 700 °C [6]. In Ref. [5], a growth rate in the order of 100 nm/min was achieved at 650 °C during the epitaxy of undoped Si using neopentasilane as Siprecursor gas.

In this paper, we present results of the epitaxial deposition of undoped and *n*-type doped Si with arsenic and phosphorus using trisilane (Si₃H₈) as Si-precursor gas, for the fabrication of monocrystalline emitters in bipolar transistors. In this particular application, high growth rates are desired to minimize the process time of the deposition step, as the typical thickness of the epilayer is 150 nm. As a source of trisilane, we used Silcore[®] which is a commercial grade of specially purified and conditioned trisilane. The *n*-type in-situ doping with arsenic and phosphorus was investigated by using arsine and phosphine, respectively, as dopant precursor gases. We show that the sensitivity of the growth rate on the dopant gas flow with trisilane is much higher than with DCS. Furthermore, no saturation was observed as function of the dopant gas flow. We also observed that using trisilane as Si-precursor resulted in a much more linear *n*-type doping behavior than DCS. Growth rates of 55 nm/min could be achieved at 600 °C. These results are very promising for the epitaxy of highly doped Si layers in a production environment.

2. Experimental

The epitaxial layers were deposited on 200 mm Si (0 0 1) wafers, using a standard horizontal cold wall, loadlocked, Advanced Semiconductor Materials (ASM) EpsilonTM 2000 reactor, a reduced pressure CVD (RPCVD) system designed for production environment. Before deposition, the blanket wafers received a NH₄OH/O₃-based clean followed by an in-situ bake at 1050 °C for 60 s in H₂ in order to remove the native oxide. Deposition was performed using reduced pressure of 15 Torr and H₂ as carrier gas. Arsine (AsH₃) and phosphine (PH₃), 0.1% diluted in H₂, were used as *n*-type sources with gas flows up to 200 standard cubic centimeters per minute (sccm). The temperature was varied between 500 °C and 600 °C. Trisilane was used as Si-precursor. Because this material is a liquid at room temperature and atmospheric pressure, it is injected into the process chamber by bubbling hydrogen through the liquid.

Using the growth conditions described here above results in non-selective deposition. Therefore, the epilayer thickness cannot be estimated by step height measurement. Instead, scanning electron microscopy (SEM) or weight measurements were used to provide input for a more accurate measurement by spectroscopic ellipsometry (SE). The SEM inspection was done with a Nova 200 system from FEI Company and weight measurements were performed with a Mentor SF³ system, a fully automated tool from Metryx. SE measurements were made with an Advanced Spectroscopic Ellipsometry Technology system from KLA-TENCOR. With this method, the thickness of Si layers grown on SiGe films can be determined [7,8]. In this study, the typical thickness of the grown layers ranged from 100 nm to 1 μ m, depending on the expected doping level.

The sheet resistance was obtained using a classical four-point-probe method. Combined to thickness measurement, this allowed us to determine the resistivity of the epilayer. Finally, from well-known carrier mobility data, the carrier concentration in the grown layer could be estimated. In the standard curve of the dopant concentration as function of the resistivity of *n*-type Si [9], it is assumed that the impurities are fully active. As we will show here below, the activation level of As and P in the in-situ doped layers of the present work is lower than 100%, leading to a depression of the carrier mobility. As a consequence, the active dopant concentration could be underestimated. This effect was not taken into account in our discussion of the results.

3. Results and discussion

Layers with good epitaxial quality were obtained under various growth conditions. This was routinely checked by the inspection of the processed wafers with an optical microscope operating in Nomarski mode and confirmed by channeling Rutherford back-scattering spectroscopy measurements.

The effect of the dopant gas flow on the deposition rate of the Si film is shown in Fig. 1 for a growth temperature of 600 °C and a trisilane mass flow of 200 mg/min. We show in Fig. 2 the corresponding dependence of the carrier concentration on dopant gas flow under similar conditions for the Si-precursor. These results indicate that with a PH₃ flow of 200 sccm, the active P concentration is about 10¹⁹ cm⁻³ with a growth rate as high as 56 nm/min. For As-doped Si layers, the growth rate ranges from 40 nm/min up to 50 nm/min. In Fig. 1, the results corresponding to two batches are shown. The second data set was obtained after a hardware intervention and no optimization was made to match these results with those obtained with P-doped Si.





Fig. 2. Carrier concentration as function of dopant gas flow, for As (with trisilane and with DCS) and P (with trisilane).



In the case of AsH₃, we also compared the results obtained with trisilane with those obtained with dichlorosilane (DCS) at a temperature of 700 °C and atmospheric pressure under similar doping parameters. Those conditions are known to yield highly doped *n*-type Si epilayers [6,10]. The benefit of using trisilane as a Si-precursor gas over that of using DCS is demonstrated in terms of the achievable active As concentration at high growth rate.

Indeed, with AsH₃ and Si₃H₈, an active dopant concentration of 7×10^{19} cm⁻³ could be achieved with a dopant gas flow of 200 sccm. This is comparable to the value that was obtained with DCS, but the corresponding growth rate was lower than 15 nm/min in the latter case whereas the deposition rate with Si₃H₈ reached 43 nm/ min. The comparison with DCS also shows that, although carrier concentrations are similar, the sensitivity on the dopant gas flow with trisilane is much higher than with DCS. With trisilane, the active dopant concentration increases by one order of magnitude for every decade of increase of the dopant gas flow, whereas, with DCS, this rate is about 0.2 decade per decade of AsH₃ flow. Apparently, using trisilane as Si-precursor results in a much more linear *n*-type doping behavior than DCS, and hence allows an easier process control and a wider dynamic doping range with a lower marginal cost in the high doping regime. However, it is expected that this trend does not continue for very high AsH₃ flows because the solid solubility of the dopant in Si at the given deposition temperature will be reached. The activation levels were determined by comparing the carrier concentration with the total dopant concentration as extracted from secondary ion mass spectrometry. At 600 °C, we obtained an activation level between 65% and 75%, with a dopant flow of 200 sccm and trisilane flow of 200 mg/min. This incomplete activation could be explained by the formation of non active As-As or P-P dimers [11] due to dopant surface mobility. This interpretation is supported by the dependence of the carrier concentration on the growth rate, as described here below.

In order to understand the growth regime for the Si deposition, we investigated the effect of the temperature on the growth rate of As-doped Si as well as on the corresponding carrier concentration in the temperature range between 500 °C and 600 °C. The trisilane flow was fixed at 200 mg/min. As shown in Fig. 3, the deposition rate shows a strong temperature-dependence in that range. This behavior illustrates the effect of kinetics on the epitaxial growth. The analysis of the Arrhenius plot led to a thermal activation energy of 41.7 kcal/mole (1.81 eV). This value is only weakly dependent on the AsH₃ flow. This indicates that the limiting factor in the deposition rate is not related to the reaction of the dopant with the growing surface but rather to the pyrolysis of the Si₃H₈ reactant. We also show in Fig. 3 that the As incorporation can be slightly increased by using a lower deposition temperature, if one can afford to trade a significantly reduced growth rate for an enhanced active concentration. The contribution of the kinetic control to the growth regime can be beneficially used to improve the uniformity of the layer thickness through the optimisation of the temperature profile in the deposition chamber. This latter procedure is illustrated in Fig. 4 for the growth with a Si₃H₈ flow of 200 mg/min and an AsH₃ flow of 200 sccm/min.

The impact of the Si-precursor mass flow on the properties of the grown layers is shown in Fig. 5. At a deposition temperature of 600 °C, the deposition rate linearly increases with the Si_3H_8 flow, which indicates that the growth is partially controlled by mass transport limitations. The influence of the dopant flow on this behavior is almost negligible. The active concentration also increases with the Si-precursor flow and thus with the growth rate. These observations led us to the interpretation that, due to the dopant surface mobility during the growth and before dopant incorporation, a higher trisilane flow, which is related to a higher growth rate, is in favor of the incorporation of dopant atoms at a higher level. Indeed, surface diffusion is decreased by a higher deposition

Published in : Applied Surface Science (2007), vol. 254, pp. 6072-6075. Authors : N.D. Nguyen, R. Loo, M. Caymax Status : Postprint (Author's version)

rate. As a consequence, the risk of formation of non active dopant dimers decreases and higher activation can be achieved. It is also shown in Fig. 5 that the growth rate can be substantially enhanced by a higher trisilane flow while keeping high carrier concentration values.

Fig. 3. Growth rate and carrier concentration as function of (reciprocal) temperature for n-type Si grown with trisilane and AsH₃.



Fig. 4. Si epilayer thickness profile across the wafer for different settings of the temperature profile in the *RPCVD* reactor.







4. Conclusions

The growth of *n*-type epitaxial Si layers doped with As and P by means of low-temperature CVD using trisilane was studied as a function of the deposition temperature, the Si-precursor mass flow and the dopant gas flow.

We showed that the sensitivity of the carrier concentration on the dopant gas flow with trisilane is much higher than with DCS and that no saturation occurs in the region between 0 sccm and 200 sccm. Moreover, a linear-dependence of the carrier concentration on the flow was observed. These properties could be due to the fact that, within the temperature range of 500-600 °C, the epitaxial layer grows under a regime that is a mixture of the mass transport regime and the kinetically controlled regime.

A process for heavily doped epilayers was therefore demonstrated at 600 °C with growth rates as high as 55 nm/ min. In a next step, it will be applied to the epitaxy of monocrystalline emitter layers for BiCMOS applications.

In our work, the total pressure was a constant parameter of the process, with a value of 15 Torr. It is known that gas depletion effects can occur at atmospheric pressure during the growth of undoped Si layers. Thus, it would be interesting to investigate such effects in the case of highly doped epitaxial films.

Acknowledgments

The supply of Silcore[®] by Voltaix, Inc. is gratefully acknowledged. The authors wish to thank Matthew Stephens and Michael Pikulin from Voltaix for helpful discussions. N.D. Nguyen would like to thank Eddy Kunnen and Emma Vecchio for performing the weight measurements. The financial support by Fonds Wetenschappelijk Onderzoek (FWO) is gratefully acknowledged.

References

[1] M.R. Caymax, W. Leong, Low thermal budget chemical vapour deposition techniques for Si and SiGe, in: J.F. Nijs (Ed.), Advanced Silicon and Semiconducting Silicon-Alloy Based Materials and Devices, Institute of Physics Publishing, Bristol, 1994.

[2] R. Loo, et al. ECS Transactions 3 (2006) 453.

- [3] Bauer M, ICSI-5 Book of Abstracts 2007 9
- [4] L.J. Choi, et al. IEEE Trans. Electron Devices 28 (2007) 270.
- [5] J.C. Sturm, K. Chung, E. Sanchez, K.K.K. Singh, S. Kuppurao, ECS Meet. Abstr. 701 (2007) 606.

[6] P. Agnello, T.O. Sedgwick, J. Cotte, J. Electrochem. Soc. 140 (1993) 2703.

- [7] C. Ygartua, M. Liaw, Thin Solid Films 313-314 (1998) 237.
- [8] R. Loo, M. Caymax, G. Blavier, S. Kremer, in: G. Kissinger, L.H. Weiland, Proc. SPIE 4406 (2001) 131.
- [9] S.M. Sze, Physics of Semiconductor Devices, J. Wiley and Sons, 1981, p. 32.
- [10] R. Loo, et al. ECS Proceedings Volume 2004-07, 2004, p. 1123.
- [11] D.C. Mueller, W. Fichtner, Phys. Rev. B 70 (2004) 245207.