ECS Transactions, 27 (1) 959-964 (2010)
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Selective Epitaxial Growth of InP in STI Trenches on Off-axis Si (001) Substrates

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We report high quality InP layers selectively grown in shallow trench isolation structures on 6º offcut Si (001) substrates capped with a thin Ge buffer layer. The Ge layer was used to reduce the thermal budget for surface clean and double step formation. The atomic steps on the Ge surface were recovered after a bake at 680 ºC. Smooth nucleation layer was obtained at 420 ºC on the Ge surface. Baking the Ge surface in As ambient facilitates the InP nucleation and improves the InP crystalline quality. This improvement is attributed to the effective As adsorption on the Ge surface and the polar Ge:As surface prevents the islanding of InP seed layer. Stacking faults were found in the InP layers as a result of threading dislocation dissociation and high quality InP layers were obtained in trenches with aspect ratios greater than 2.

Introduction

High mobility channel materials, such as III-V compound semiconductors, are considered as the candidates for further boosting CMOS device performance. However, the poor thermal and mechanical properties and high cost of III-V materials prevent the use of III-V substrates. Epitaxial growth provides a promising solution for using non-Si channel materials while maintaining a relatively low cost (1, 2). With epitaxial growth III-V materials can be integrated on Si substrates to extend the Si processing technology into III-V based device processing. Selective epitaxial growth (SEG) in shallow trench isolation (STI) structures on Si (001) provides the versatility of integrating different materials on one Si substrate, such as Ge for pMOS devices and III-V for nMOS devices, since Ge has high hole mobility and zincblende III-V compound semiconductor materials generally have high electron mobilities. The combination of Ge and III-V materials on one Si substrate is essential to make high performance CMOS devices. Another advantage of SEG in submicron STI trenches is the extended defect necking effect (1), which makes it feasible to obtain extended defect free materials in device regions despite the large lattice mismatch between the epitaxial layers and the Si substrates. The extended defect necking effect is a benefit from the scaling of CMOS devices which keeps shrinking the STI dimensions and no extra effort is required to obtain the necking effect.

Previous reports have demonstrated that the necking effect is limited to trenches with aspect ratio greater than 2 (1, 2). pMOS device performance boost on Ge selectively grown in STI trenches has been demonstrated recently (3). Tang, *et*. *al*. (4) and Li, *et*. *al*. (5), reported InP SEG on exact Si (001). However, for zincblende III-V compound semiconductor epitaxial layers grown on Si (001) or Ge (001) substrates, the reduced symmetry of III-V compounds induces antiphase boundaries (APBs). These APBs are either in {111} or in {110} planes. The APBs in {110} cannot be trapped by the STI side walls and thus penetrate to the surface. Despite that APBs were found to annihilate in a few micrometer thick InP layer on Si (001) (6), it is not clear whether they can be effectively suppressed in shallow trenches, especially within a thickness of 300 nm. To avoid APBs, offcut Si (001) substrates have been widely used in previous studies (7, 8). In this work, SEG of InP in STI trenches on Si (001) substrates with 6º offcut toward (111) was studied in terms of the surface treatment, nucleation and optimization of extended defect free InP materials.

Experiment

The process flow for InP growth in STI trenches is shown in Fig. 1a. 200 mm Si (001) substrates with 6º offcut toward (111) were used. Trenches of width from 0.1 µm up to 100 µm were made with SiO_2 STI patterning and about 40% of the total Si wafer surface was exposed for Ge and III-V deposition. The trenches were aligned in the [110] and [$\bar{1}$10] directions. The thickness of the STI-SiO_2 is 300 nm. After a standard wet clean, HF dip and in-situ H_2 bake at 850 °C to remove the native oxide, the Si was recessed to a depth of ~300 nm by in-situ HCl vapor phase etching at 850 °C and 10 Torr, using an ASM-Epsilon^{TM} 2000 reactor. This was followed by 40-75 nm Ge deposition on the recessed Si surface at an atmospheric pressure. GeH_4 (1% in H_2) was used as the Ge precursor with H_2 carrier gas.

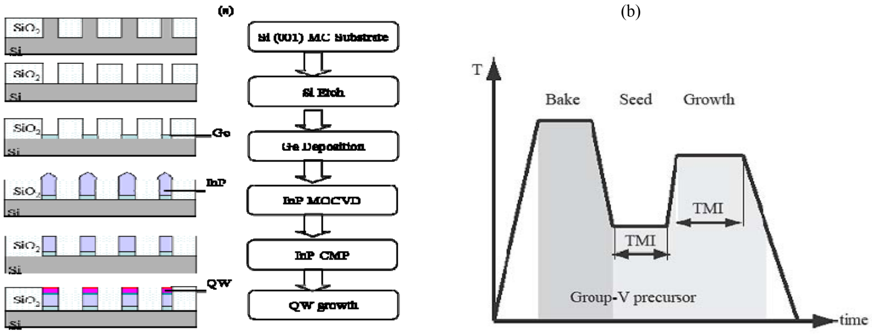

Fig. 1. Epitaxial growth flow for InP buffer layer in offcut Si (001) STI trenches and the subsequent $In_xGa_{1-x}As$ quantum well (QW) channel.

After Ge deposition, the Si substrates were cleaved into 2-inch pieces and loaded into a Thomas Swan metalorganic chemical vapor deposition (MOCVD) reactor. The InP growth procedure is shown in Fig. 1b. Before growth, a pre-epi bake at 680 °C was carried out to remove the native Ge oxide and carbon contamination at 450 Torr. Since Ge native oxide desorbs at about 430 °C (9), the use of thin Ge layers avoids high thermal budget otherwise to be used to remove the native oxide on Si surface. A group-V element precursor, either tertiarybutylarsine (TBA) or tertiarybutylphosphine (TBP) was introduced in the H_2 ambient during the bake. With this bake, Ge was confirmed completely strain relaxed by X-ray diffraction and this relaxed Ge layer mitigated the lattice mismatch between the InP layer and the Si substrate. After the bake, the temperature was ramped down to 420 °C to grow a InP seed layer. The bulk layer was grown at a higher temperature. Trimethylindum (TMI) and trimethylgallium (TMG) were used as the group-III element precursors. The surface morphologies were characterized with a scanning electron microscope (SEM) and an atomic force microscope (AFM). The crystalline defects were characterized with transmission electron microscopy (TEM).

Results and discussion

Ge surface morphology change during H_2 bake

As shown in Fig. 1, 40~75 nm Ge epitaxial layers were used to reduce the thermal budget during pre-epi bake and to reduce the lattice mismatch between the InP layers and the substrates. However, the Ge layer surface is not as smooth as Si substrate due to Stranski-Krastanov growth mode of Ge on Si. In addition, although the pre-epi bake at 680 °C is sufficient to remove the Ge native oxide, the Ge surface roughness may change at this temperature. Figure 2 shows the AFM images of a 75 nm Ge layer grown on an offcut Si (001) substrate. The as-grown Ge surface roughness is about 0.5 nm and there is no change in RMS roughness after a bake at 680 °C for 4 min. However, the feature of surface atomic steps are clear after the bake (Fig. 2b). These atomic steps facilitate the nucleation of InP and avoid antiphase domains.

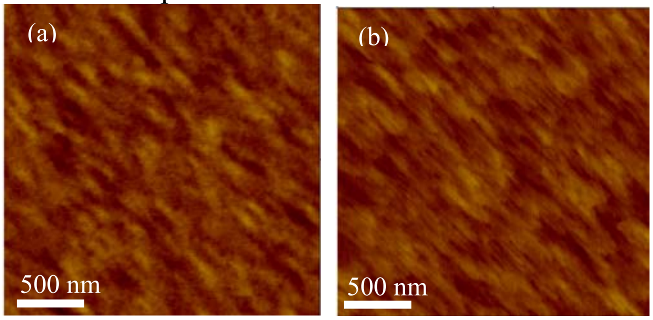

Fig. 2. AFM images of a 75 nm Ge layer on a 6º offcut Si (001) substrate before H_2 bake (a) and after H_2 bake at 680 °C for 4 min at 450 Torr (b). The RMS is 0.51 nm (a) and 0.49 nm (b), respectively. The atomic steps become more visible after the H_2 bake.

InP seed layer growth in STI trenches

The 8% lattice mismatch between InP and Si (001) substrates causes islanding at the beginning of growth. The direct growth of InP on Si (001) substrate has been found to cause high density of staking faults and poor crystalline quality (5). Consequently, a GaAs seed layer grown at 400 °C with a subsequent anneal at 600 °C has been used to improve the InP crystalline quality (5). However, in our experiments, poor growth selectivity of GaAs was observed at low temperatures. Therefore, we chose the strain relaxed Ge epitaxial buffer layer instead of the GaAs seed layer. With a strain relaxed Ge layer, the lattice mismatch reduces to 3.7% which is similar between Ge and Si. Accordingly, islanding can be mitigated by optimizing the seed layer growth conditions. However, different from Ge epitaxial growth on Si (001) substrates, InP bonds are partially ionic. The nucleation of InP on Ge surface requires a full monolayer coverage of P. If the Ge surface is not completely covered by P, then In droplets may form and lead to polycrystalline InP. At a low temperature, P desorption rate is limited at a high TBP partial pressure. In addition, the growth temperature must be higher than the cracking temperature of TBP, which is about 400 °C (10). Figure 3 shows the SEM images of InP seed layer grown at 450 °C, 420 °C, and 390 °C, respectively. All the seed layers were grown at 450 Torr, with a TBP partial pressure of 0.97 Torr and V/III ratio of 313. In Fig. 3a, the islands of a few hundred nanometers formed as a result of In migration. In contrast, by lowering the growth temperature (Fig. 3b), we obtained reduced island size and the surface roughness decreases. However, further lowering the growth temperature by 30 °C, we found the island sizes increased again as a result of In droplet formation (Fig. 3c). At 390 °C, the TBP precursor is not completely cracked while TMI is decomposed, resulting in a reduced equivalent V/III ratio. In addition, the reaction of In with P requires enough thermal budget to overcome the reaction activation energy barrier. At 390 °C or lower temperatures, the reaction rate of InP is limited while the catalytic reaction dominates on the In droplet surface (11). Consequently, islands are formed around the In droplet where TBP is catalytically decomposed to provide P reactant. As a result, InP nanowires were obtained in Fig. 3c. In such a temperature regime, no complete layer is obtained.

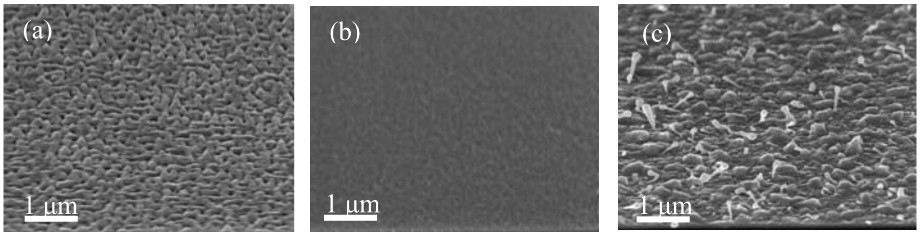

Fig. 3. SEM images of InP grown on 75 nm strain relaxed Ge epitaxial layer at 450 °C (a) and 420 °C (b), and 390 °C (c), respectively.

A rather narrow temperature window was found in Fig. 3 for the InP seed layer growth. To avoid islanding and to obtain a smooth seed layer, high TBP partial pressure and low growth temperature above the TBP cracking temperature are required. At low temperatures, In migration was suppressed and a continuous InP seed layer was obtained. This continuous seed layer ensures a smooth InP layer for the bulk layer growth at elevated temperatures.

After the seed layer growth at 420 °C and 450 Torr, the substrate temperature was ramped to a temperature above 550 °C, during which no TMI was introduced in the reactor while TBP flow was kept constant. This temperature ramp gives additional thermal budget to anneal out the point defects in the InP seed layer. In migration on the seed layer in the ambient of TBP allows smoothening of the seed layer surface. After the temperature stabilization, TMI partial pressure was ramped up to obtain a higher growth rate, 1µm/h.

Crystalline quality improvement by TBA

As described above, InP nucleation was done at a low temperature to avoid islanding. However, the nucleation also depends on the starting Ge surface conditions, such as the atomic step configurations. Step movement on vicinal Ge (001) surface at high temperatures has been well understood. McMahon *et. al.* studied vicinal Ge (001) surfaces annealed in both As and P ambient (12, 13). They reported that a high AsH_3 partial pressure led to Ge double steps while single steps were observed at a low AsH_3 partial pressure (13). In contrast, annealing in PH_3 ambient did not result in double steps (12). It has been reported that baking in As ambient resulted in improved crystalline quality for GaP on Si (001) because As is more easily adsorbed on Si surface compared with P (14). Similar mechanism applies to Ge surfaces. The adsorbed As monolayer changes the nonpolar Ge surface into polar surface which facilitates the subsequent InP nucleation. In addition, the As atoms on the Ge surface introduce surfactant effect to retard the diffusion of In adatoms. It is known that stacking faults and dislocations are formed at the boundary of two islands when they merge (14). The As terminated Ge surface reduces the InP island density and accordingly the stacking fault density. Although our Ge epilayer does not reproduce exactly the steps on the offcut Si (001) substrates due to the Ge surface roughness (RMS 0.5 nm), atomic steps still exist on the Ge layer surface as shown in Fig. 1b. Therefore, it is essential to choose the correct baking conditions.

The impact of group-V element precursors as used during the pre-epi treatment of the Ge surface on the InP surface morphology is shown in Fig. 4. A clear influence of the baking ambient on InP surface morphology was revealed. Baking the Ge epilayer at 680 °C in TBP (Fig. 4a) lead to irregular InP surface morphology. This distorted overgrowth was caused by the stacking faults or microtwins in the InP layer which prevent the growth in the vertical direction. By baking the Ge surface in TBA ambient, the vertical growth of InP was successfully obtained (Fig. 4b). This vertical growth indicates improved crystalline quality and reduced stacking fault density. This improvement in InP surface morphology is attributed to the As:Ge surface electronic properties. The polar As:Ge starting surface lowers the interface energy between the InP layer and Ge surface. However, there are still some trenches where distorted overgrowth was observed, suggesting that some stacking faults still exist in this InP layer. To further improve the InP layer quality, a 5 nm GaAs layer was grown at 420 °C after the bake in TBA ambient. The thin GaAs layer stabilizes the As terminated surface for the subsequent InP growth. Consequently, all the trenches show consistent vertical growth (Fig. 4c).

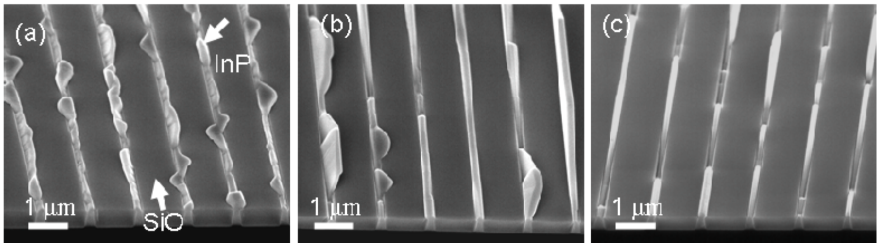

Fig. 4. Tilted-view SEM images of InP in 110 nm wide trenches along [110]. The InP was grown at 610 °C, 76 Torr with different pre-epi treatment conditions, (a) Ge epilayer baked in TBP, (b) Ge epilayer baked in TBA, and (c) Ge epilayer baked in TBA with subsequent ~5 nm GaAs at 420 °C.

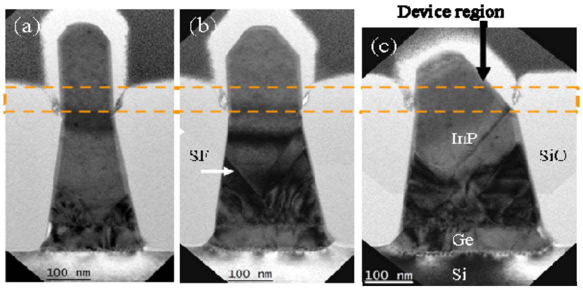

Fig. 5. Cross-section TEM images of InP in [110] oriented STI trenches grown at 610 ºC, 76 Torr. The trench widths from from (a) to (c) are, 110 nm, 150 nm, and 200 nm, respectively.

Since the stacking faults formed by the dissociation of dislocations can not be avoided due to the large lattice mismatch at the InP/Ge interface, the aspect ratio of a trench determines the quality of the InP material on top of the trench, as shown in Fig. 5. The aspect ratios in Fig. 5a, b, and c are 3, 2, and 1.5, respectively. It is clearly shown that an aspect ratio greater than 2 is required to obtain extended defect free InP materials in the device region.

Conclusions

We obtained high crystalline quality InP layers selectively grown in STI trenches on Si (001) substrates with 6º offcut toward (111). The InP layers were confirmed free of extended defects on top of the trenches with aspect ratio greater than 2. This provides the starting templates for fabricating high electron mobility channel devices on Si substrates. The strain relaxed Ge buffer layer reduces the thermal budget during the pre-epi bake and mitigates the lattice mismatch between InP and the underneath Si substrates. After baking at 680 °C, Ge surface roughness did not change while the atomic steps become clear. The nucleation of InP on the Ge buffer layer surface showed strong temperature dependence. Nucleation at a temperature right above the TBP decomposition ensured P covered Ge surface and retard InP surface diffusion so that islanding was suppressed. As terminated Ge surface resulted in a better InP surface morphology.

Acknowledgement

This work is funded by IMEC Ge and III-V program and European project DualLogic. The present authors would like to acknowledge IMEC core partners and the European commission for financial support.

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