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(54) **Method for manufacturing a junction**

Herstellungsverfahren für einen Übergang

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Description

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention relates to a semiconductor device comprising a homojunction or a heterojunction with a controlled dopant (concentration) profile and a method of making the same. For example, the present invention can be suitably applied in the manufacturing of a bipolar device for BiCMOS technology or of a photovoltaic device having a controlled dopant (concentration) profile at the emitter-base interface.

BACKGROUND OF THE INVENTION

[0002] In the npn (pnp) bipolar transistor, the emitter layer consists of n-type (p-type) semiconducting material that is deposited on top of the epitaxially-grown base structure. The emitter itself is either polycrystalline or monocrystalline. A monocrystalline emitter is preferred from the point of view of device integration because it allows for a reduction of parasitic resistance and enables band gap engineering of the emitter stack in the perspective of optimization of the transistor performances. In both cases, high dopant concentration (above 1E20 at/cm3) is required in order to achieve low-resistance emitter layer.

[0003] Nowadays the fabrication of a bipolar transistor is performed in a BiCMOS process flow, which means that the thermal anneal that drives the dopants from the emitter layer into the base layer also serves as a junction activation anneal for the CMOS part of the device. This step, which consists of a spike anneal occurring after the deposition of the emitter layer, is usually fixed by the optimization of the CMOS part of the process flow and provides a relatively high thermal budget which adversely impact on the bipolar device characteristics.

[0004] JP 2003 059936 describes a bipolar transistor on a semiconductor substrate and a method of manufacturing thereof. The method involves forming a base electrode from a polycrystalline silicon, forming an emitter region on the surface of an intrinsic base region by Atomic Layer Doping, and forming an emitter electrode on the emitter region.

[0005] Liu, W. C. et al. discloses in "Design consideration of emitter-base junction structure for InGaP/GaAs heterojunction bipolar transistor", in IEEE proceedings 1999 p246-248, a study of an InGaP/GaAs heterojunction bipolar transistor (HBT) with a 50Å undoped spacer and δ-doping sheet at base-emitter interface.

[0006] EP 1 178 537 relates to a bipolar transistor and semiconductor device. It discloses a bipolar transistor comprising an emitter layer containing an impurity of a first conductivity type, a base layer containing an impurity of a second conductivity type, and a collector layer containing the impurity of the first conductivity type, said bipolar transistor having, a high-concentration doped layer being provided in said emitter layer which is adjacent to a depletion layer and doped with the impurity of the first conductivity type at a higher concentration than in said emitter layer.

[0007] Shimamune, Y. et al. discloses in "Atomic-layer doping in Si by alternately supplied PH3 and SiH4", in Thin Solid Films 380(2000) 134-136, a study of Atomic-layer doping of P in Si epitaxial growth by alternately supplied PH_3 and SiH_4 using ultraclean low-pressure chemical vapor deposition.

[0008] Schubert, E. F. discloses in "Delta doping of semiconductors" 1996 (Cambridge University Press) p4, a definition of δ-doping.

[0009] Tillack, B. et al. demonstrates in "Atomic layer processing for doping of SiGe", in Thin Solid Films 508(2006) 279-283, atomic layer processing for doping SiGe during Reduced Pressure Chemical Vapour Deposition (RPCVD) in a commercial single wafer reactor.

SUMMARY OF THE INVENTION

[0010] The present invention provides a method for controlling the dopant concentration profile at the emitter-base interface of a bipolar transistor.

[0011] More particularly, the present invention provides a method for controlling a dopant overshoot (or a dopant concentration peak) at the emitter-base interface of a bipolar transistor.

[0012] Furthermore, the present invention provides a method for improving the control of the doping profile at the emitter-base interface of a bipolar transistor (when compared to methods described in the art).

[0013] The present invention provides a method for controlling the in-diffusion depth of the dopants at the emitter-base interface of a bipolar transistor upon a rapid thermal treatment.

[0014] More particularly, the present invention provides a method for improving the control of the in-diffusion depth of the dopants at the emitter-base interface of a bipolar complementary metal-oxide-semiconductor (BiCMOS), upon applying the activation anneal of the complementary metal-oxide-semiconductor (CMOS) flow (when compared to methods described in the art).

[0015] The present invention provides a method for forming a highly doped semiconductor layer in a bipolar transistor having a dopant concentration exceeding (or above) the dopant solid solubility.

[0016] According to one aspect of the present invention, a method is provided for manufacturing a junction with a controlled dopant (concentration) profile according to claim 1.

[0017] In the context of the present invention, a controlled dopant (concentration) profile refers to a steep (or abrupt or box-shaped or sharp) (concentration) profile of the second dopant at the junction in the as-deposited structures/layers.

[0018] More particularly, in a method of the present invention, the second concentration of the second dopant is increased locally (or an overshoot is created) at the

junction. Otherwise stated, the second dopant (concentration) profile at the junction is controlled by steepening the second dopant (concentration) profile at the emitter-base junction.

[0019] In a method of the invention, the first semiconductor material can be a monolayer (or a single layer), or can comprise multiple layers, each of them being epitaxially grown.

[0020] In a method of the invention, the first concentration of the first dopant in the first semiconductor material can be comprised between (about) 10^{18} atoms cm^{-3} and (about) 10^{19} atoms cm^{-3}, preferably lower than $1x10^{20}$ atoms cm^{-3}.

[0021] In the context of the present invention, a fraction of a monolayer of a precursor refers to the deposition of less than one monolayer of said precursor on the surface (of a semiconductor material), whereby said surface is not fully covered with said precursor (i.e. incomplete coverage of the surface). Furthermore, it is to be understood that clustering of said precursor does not occur in said fraction of said monolayer.

[0022] In the context of the present invention, one monolayer (or one ML, or one single atomic layer) of a precursor refers to the deposition of said precursor on the surface (of a semiconductor material), whereby said surface is fully covered with said precursor. Furthermore, it is to be understood that clustering of said precursor does not occur in said monolayer.

[0023] Preferably, in a method according to the invention, the first semiconductor material and the second semiconductor material have the same composition, thereby forming a homojunction.

[0024] Preferably, in a method according to the invention, the first semiconductor material and the second semiconductor material have different compositions, thereby forming a heterojunction.

[0025] Preferably, in a method according to the invention, forming the second semiconductor material comprises

- performing a sequence consisting of
- epitaxially growing a layer of a second semiconductor material and thereupon
- depositing by Atomic Layer Epitaxy a monolayer of a precursor suitable to form the second dopant
- repeating the sequence at least twice, thereby incorporating the second dopant in substitutional sites in the second semiconductor material.

[0026] Preferably, in a method according to the invention, the second concentration of the second dopant in the second semiconductor material is higher or equal to $1x10^{20}$ cm^{-3}.

[0027] Preferably, in a method according to the invention, the second dopant is a n-type dopant.

[0028] Preferably, the n-type dopant is arsenic (As) or phosphorus (P).

[0029] Preferably, the precursors suitable to form the n-type dopant are arsine (AsH_3) or phosphine (PH_3).

[0030] Preferably, in a method according to the invention, the first dopant is a p-type dopant.

[0031] Preferably, the p-type dopant is boron.

[0032] Preferably, in a method according to the invention, the second semiconductor material comprises Si, Ge or combinations thereof.

[0033] Preferably, in a method according to the invention, the second semiconductor material is an emitter region of a bipolar transistor.

[0034] Preferably, in a method according to the invention, the first semiconductor material comprises Si, Ge or combinations thereof.

[0035] Preferably, in a method according to the invention, the first semiconductor material is a base region of a bipolar transistor.

[0036] Preferably, a method according to the invention further comprises a rapid thermal treatment (or rapid thermal anneal (RTA) or spike anneal).

[0037] In a method of the invention, said rapid thermal treatment is performed after the step of forming a second semiconductor material.

[0038] According to one aspect of the invention, said rapid thermal treatment is performed after the step of forming a second semiconductor material, at the same time (or simultaneously) with the activation anneal of the CMOS device.

[0039] The present invention provides a method for controlling the in-diffusion depth of the dopants at the emitter-base interface of a bipolar transistor upon a rapid thermal treatment.

[0040] In the context of the present invention, the in-diffusion depth (or electrical junction depth or (in-)diffusion length) of the dopants refers to the depth to which said dopants are diffused into the base region upon performing a rapid thermal anneal.

[0041] In a method of the invention, said rapid thermal treatment is performed using any means known in the art, more preferably by rapid thermal anneal, by laser anneal, or by flash anneal.

[0042] Preferably, the temperature of said rapid thermal anneal (or spike anneal) is comprised between (about) 1050°C and (about) 1200°C for (about) 0 seconds (of soaking time), more preferably (about) 1100°C for (about) 0 seconds (of soaking time).

[0043] Preferably, when said rapid thermal treatment is performed by laser anneal or by flash anneal, the exposure time is of the order of sub-milliseconds.

[0044] Preferably, the rapid thermal treatment is a typical HDD (highly doped drain) activation anneal used in CMOS technology.

[0045] Preferably, an in-diffusion depth of Arsenic (As) into the first semiconductor material is lower or equal to 15nm upon (performing) the rapid thermal treatment.

[0046] According to another aspect, the present invention relates to the use of a method as above described for the manufacture of a bipolar CMOS (BiCMOS) device.

[0047] In still another aspect, the present invention re-

lates to the use of a method as above described for the manufacture of a photovoltaic device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0048]

Fig. 1a represents schematically the emitter-base heterojunction (Si/SiGe) of a bipolar transistor, wherein the emitter is n-type heavily doped and the base is p-type doped (before performing a rapid thermal anneal).

Fig. 1b represents schematically the emitter-base heterojunction (Si/SiGe) of a bipolar transistor, wherein the emitter is n-type heavily doped and the base is p-type doped, having an overshoot (or concentration peak magnitude) of the n-type dopant (As) present at the emitter-base metallurgical junction (before performing a rapid thermal anneal). Said overshoot of the n-type dopant (As) may then be used as a reservoir of n-type dopant (As) for adjusting the concentration profile of said dopant, during (or upon performing) a subsequent rapid thermal anneal (i.e. diffusion of said dopant into the base region).

Fig. 2a represents schematically the emitter-base heterojunction of Figure 1a, upon (performing or after having performed a) rapid thermal anneal, the junction being electrically activated (the transition region or the emitter-base interface region in fig. 2a represents the region from the metallurgical junction up to (and including) the SiGe2 region).

Fig. 2b represents schematically the emitter-base heterojunction of fig. 1b, upon (performing or after having performed a) rapid thermal anneal, the junction being electrically activated.

Fig. 3 represents the Arsenic (As) dose as measured by X-Ray photoelectron spectroscopy (XPS) on as-deposited material as function of the exposure time to the precursor gas (AsH_3) in the CVD reactor.

Fig. 4 represents schematically the process sequence comprising an Atomic Layer Epitaxy (ALE) step and an epitaxial (over)growth step repeated n-times (or n-cycles) to achieve a dopant dose exceeding the dopant solid solubility.

Fig. 5a shows the Arsenic (As), Germanium (Ge), Silicon (Si) concentration as measured by secondary ion mass spectrometry (SIMS) (the transition region between the emitter region and the (base cap of the) base region is indicated on top of said figure). The origin of the depth scale is at the top surface of the base region (or metallurgical junction): (curve 1) no anneal, without ALE; (curve 2) with anneal, without ALE; (curve 3) no anneal, with ALE; (curve 4) with anneal, with ALE. The (rapid) thermal anneal was performed at 1085 °C (spike anneal). In the right figure of fig. 5a (i.e. depicting a zoom of curve 1 and curve 3) the expected profile for reduced ALE dose (submonolayer) is simulated.

Fig. 5b shows only the Arsenic (As) concentration (as represented in fig. 5a) as measured by secondary ion mass spectrometry (SIMS).

Fig. 6a (and fig. 6b) represents the results of the Technology Computer Aided Design (TCAD) simulations of an emitter grown using ALE (i.e. depicting the Ge and As concentration (cm^{-3}) versus the depth of the substrate (μm) after mono-emitter growth and after performing a spike anneal, respectively).

DETAILED DESCRIPTION OF THE INVENTION

[0049] In the context of the present invention, a metallurgical (emitter-base) junction refers to the physical junction between the emitter region and the (base cap of the) base region of a bipolar transistor.

[0050] In the context of the present invention, the (emitter-base) interface (region) (or transition region), refers to the region from the metallurgical junction up to (and including) the SiGe2 layer, as shown e.g. in Fig. 5a and Fig. 5b.

[0051] In the context of the present invention, the top surface of the base region refers to the starting surface for depositing the emitter (region) onto the base (region).

[0052] In the context of the present invention, an electrical (emitter-base) junction refers to the intersection between the n-type dopant (e.g. As) concentration profile and p-type (e.g. B) dopant concentration profile upon rapid thermal anneal.

[0053] In the context of the present invention, an abrupt (or box-shaped, sharp, or steep) dopant (concentration) profile at the emitter-base interface refers to a dopant (concentration) profile represented by a curve of the dopant concentration versus the depth of the substrate, said curve having a steep slope (such as represented e.g. in fig. 1a, 1b, or in fig. 5a, 5b (curve 3)). More particularly, the slope of said curve (i.e. x nm/decade in doping concentration) should be as small as possible (e.g. 1.5 to 3 nm/decade in doping concentration). Upon performing the rapid thermal anneal said slope is less steep (or less abrupt) and shows a kink (such as represented e.g. in fig. 2a, 2b, or in fig. 5a, 5b (curve 4)) due to the diffusion of the dopant into the base region.

[0054] One inventive aspect relates to a semiconductor device comprising a homojunction or a heterojunction with a controlled dopant (concentration) profile and a method of making the same.

[0055] Another inventive aspect relates to a method for manufacturing a bipolar device (suitable for BiCMOS technology) having a controlled dopant (concentration) profile at the emitter-base interface and a controlled in-diffusion depth for a (pre-determined) rapid thermal treatment compatible with the conventional CMOS flow. Preferably, the dopant (concentration) profile at the (emitter-base) interface is steep (i.e. abrupt/box-shaped).

[0056] Another inventive aspect relates to a method for manufacturing a photovoltaic device having a control-

led dopant (concentration) profile at the emitter-base interface. Preferably, the dopant (concentration) profile at the interface is steep (i.e. abrupt/box-shaped).

[0057] Yet another inventive aspect relates to a method for forming a highly doped semiconductor layer for a photovoltaic device (e.g. an emitter layer) having a dopant concentration exceeding the dopant solid solubility.

[0058] Another aspect of the present invention relates to a method for forming for forming a highly doped semiconductor layer in a tunnel Field Effect Transistor (FET) having a dopant concentration exceeding the dopant solid solubility.

[0059] The present invention will be described with respect to particular embodiments and with reference to certain drawings but the invention is not limited thereto but only by the claims. Any reference signs in the claims shall not be construed as limiting the scope. The drawings described are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes.

[0060] In a bipolar transistor an electrical junction is (typically) formed between an emitter region and a base region.

[0061] In case of a *npn* bipolar transistor, the emitter region comprises a *n*-type heavily-doped semiconductor material and the base region comprises a *p*-type doped semiconductor material (the emitter layer being deposited on top of the surface of the epitaxially-grown base structure).

[0062] In case of a *pnp* bipolar transistor, the emitter region comprises a *p*-type heavily-doped semiconductor material and the base region comprises a *n*-type doped semiconductor material (the emitter layer being deposited on top of the surface of the epitaxially-grown base structure).

[0063] The base region can comprise multiple layers, each of them being epitaxially grown. For the purpose of illustration, the direction of growth is e.g. indicated by the arrow in the upper (right) corner of Figure 1a (and Figure 1b).

[0064] Different embodiments of the invention disclose a base region comprising Si and/or SiGe. Optionally, the concentration of Ge has a flat (constant) profile. Alternatively, the concentration of Ge has a ramped profile towards the top surface (of said base region), or a ramped profile towards the substrate.

[0065] In a particular embodiment of the invention a base region is disclosed having a 2-step Ge profile. More specifically the base region comprises a layer of SiGe with a first Ge concentration (SiGe1 in e.g. Figure 1a and Figure 1b), thereupon a second SiGe layer with a second Ge concentration (SiGe2 in e.g. Figure 1a and Figure 1b) and a base cap layer of Si. Preferably, the second Ge concentration is lower than the first Ge concentration

[0066] The emitter region comprises a heavily-doped semiconductor material which can be either polycrystalline or monocrystalline. A monocrystalline emitter is preferred from device integration point of view since it allows a reduction of parasitic resistance and enables band gap engineering of the emitter stack. Throughout the description, a heavily doped semiconductor material is defined as a semiconductor material having a dopant concentration above (about) $1x10^{20}$ at/cm^3. The heavily doped emitter is required in order to achieve low-resistance emitter region.

[0067] Figure 1a (and figure 1b) shows schematically a Si/SiGe heterojunction bipolar transistor before applying (rapid) thermal treatment (or anneal). The optional (epitaxially grown) Ge peak in the emitter region is designed to improve the device operation by increasing the base current without degradation of the high-frequency performance.

[0068] Figure 2a (and figure 2b) represents schematically the Si/SiGe heterojunction of the bipolar transistor of Figure 1a (and figure 1b, respectively) after applying a rapid thermal treatment (or anneal). As shown in Figure 2a (and figure 2b), the junction is electrically activated (upon applying said rapid thermal treatment) and the emitter-base n-p (electrical) junction occurs in the layer SiGe2.

[0069] For a good performance of the heterojunction bipolar transistor, several requirements need to be fulfilled: (a) a high doping level in the emitter region (to reduce the emitter resistance), typically above $1x10^{20}cm^{-3}$; (b) a sharp (i.e. abrupt, or steep) doping (concentration) profile at the emitter-base interface (e.g. in figure 1a and figure 1b) ; (c) a good control over the location of the electrical emitter-base junction (i.e. control of the electrical junction depth, given by the quality of the deposition process control), preferably positioned in the SiGe layer with low Ge content (e.g. SiGe2 in figure 2a and figure 2b, i.e. the electrical emitter-base junction preferably not being spread over the whole base thickness). In case of a base region with a ramped Ge profile, the in-diffusion depth should be reproducible (i.e. electrical emitter-base junction positioned at a fixed Ge content). A typical thickness of the base Si cap layer is about 7-15nm, which means that the (electrical) junction depth should be lower than 15nm, preferably lower than 7nm, the depth being measured from the metallurgical junction.

[0070] When the fabrication of a bipolar transistor is performed in a BiCMOS process flow, the (rapid) thermal anneal that drives the dopants from the emitter layer into the base region also serves as a HDD (Highly Doped Drain) activation anneal for the CMOS part of the device. This step, which consists of a spike (i.e. rapid thermal) anneal occurring after the deposition of the emitter layer/region, is usually fixed by the optimization of the CMOS-process flow and provides a relatively high thermal budget. A typical spike anneal for CMOS flow is a rapid thermal treatment (or anneal) at a temperature higher than 1050 °C, e.g. at 1085 °C.

[0071] The thermal budget of the spike anneal determine the in-diffusion depth of the emitter dopants and the position of the electrical emitter-base junction, which

has a direct impact on the device characteristics. The method of the invention allows to control the effect of a high thermal budget activation anneal on dopant in-diffusion.

[0072] In general, forming a perfect sharp (i.e. box-shaped) dopant (concentration) profile at the emitter-base interface region is hampered by the lack of abruptness of the transition region between the emitter layer and the substrate (i.e. base cap), especially for highly-doped layers with e.g. arsenic introduced by an in-situ doping process in a chemical vapor deposition chamber.

[0073] The difficulty of realizing abrupt (i.e. steep) transitions (or (concentrations) profiles) originates both in the poor surface adhesion of the dopant (e.g. As, P, B) and the strong surface segregation of the dopant during growth. The segregation effect results in an incorporated bulk concentration lower than that the surface concentration by several orders of magnitude. These combined effects lead to a 'corner-rounded' (or a undershoot) of the concentration profile at the emitter-base interface in the as-deposited structures (illustrated in Fig 1a), instead of the intended box-shape (i.e. steep) profile (as illustrated in Fig. 2a).

[0074] The invention discloses a method for manufacturing a junction with a controlled dopant (concentration) profile comprising:

- forming a first semiconductor material comprising a first dopant having a first concentration and thereupon
- forming a second semiconductor material comprising a second dopant having a second concentration, thereby forming a (physical/metallurgical) junction, and
- depositing by Atomic Layer Epitaxy or Vapor Phase Doping at least a fraction of a monolayer of a precursor suitable to form the second dopant on the first semiconductor material, prior to forming the second semiconductor material, thereby increasing locally the second concentration of the second dopant at the (physical/metallurgical) junction.

[0075] In various embodiments of the invention the term 'controlled dopant (concentration) profile' refers to steep (i.e. abrupt/ box-shaped) (concentration) profile of the second dopant at the junction in the as-deposited structures/layers. This can be achieved by increasing locally the second concentration (or creating an overshoot) of the second dopant at the junction. In line with the above, steepening the second dopant (concentration) profile at the emitter-base junction means controlling (or creating an overshoot in) the second dopant (concentration) profile at the junction (i.e. at the metallurgical junction, before the step of performing the rapid thermal anneal, and subsequently, at the electrical junction, after having performed the rapid thermal anneal).

[0076] In different embodiment of the invention, the first semiconductor material and the second semiconductor material are made of the same material and have the same composition, thereby forming a homojunction.

[0077] In other embodiments of the invention the first semiconductor material and the second semiconductor material are made of different materials or have different compositions, thereby forming a heterojunction.

[0078] The method of the invention may comprise additional steps in between forming a first semiconductor material comprising a first dopant and forming a second semiconductor material comprising a second dopant. In case of a BiCMOS process flow, the emitter growth is not performed in the same process step as the base growth. The process flow may comprise at least a photolithographic step for emitter window definition. However, in all cases the emitter layer/region is overlying and in contact with the base region/stack.

[0079] The method of the invention allows the control of the dopant (concentration) profile at the emitter-base interface. Locally a dopant containing layer (of high dopant concentration) is provided that is used as a dopant reservoir for the in-diffusion during the subsequent (rapid) thermal treatment (or activation anneal).

[0080] Vapor Phase Doping (VPD) is a Chemical Vapor Deposition (CVD) process wherein species (i.e. precursors) suitable to form dopants are deposited directly from the gas phase onto a substrate (e.g. a semiconductor material) through pyrolysis of a precursor gas, such as e.g. diborane (B_2H_6) for p-type doping and phosphine (PH_3) or arsine (AsH_3) for n-type doping.

[0081] Preferably, the precursors are diluted in hydrogen gas (H_2), or in an inert gas, such as nitrogen gas (N_2) or argon (Ar).

[0082] The precursors used in manufacturing are mostly diluted in hydrogen (i.e. mixtures of the species suitable to form dopants and H_2).

[0083] Forming a dopant containing layer has to be performed at a temperature lower than the corresponding dopant desorption limit for the n-type dopants (As, P) and, respectively, lower than the dopant in-diffusion limit for the p-type dopants (B). The dopant desorption limit is defined as the temperature at which the dopants start to desorb from the substrate. The dopant in-diffusion limit is defined as the temperature at which the dopants start to diffuse into the substrate.

[0084] Typical examples of n-type dopant precursors are arsine (AsH_3) and phosphine (PH_3). Advantageously, forming an arsine/phosphine containing layer is performed at a temperature lower or equal to the dopant desorption limit. In case of arsine, the dopant desorption limit is 600 °C. The dopant desorption limit put also a constraint on the deposition temperature of the epitaxial overgrowth of a semiconductor material as referred to elsewhere in the description.

[0085] A typical example of a p-type dopant precursor is diborane (B_2H_6). Advantageously, forming a diborane containing layer is performed at a temperature lower or equal to the dopant in-diffusion limit.

[0086] When the dopant deposition step from the gas

phase in the Vapor Phase Doping process occurs epitaxially on the substrate and when the amount of dopants (or dopant dose) can be atomically controlled (typically at lower temperatures then usual VPD), the technique is also known as Atomic Layer Epitaxy (ALE). Atomic Layer Epitaxy is a chemical vapour deposition (CVD) process wherein dopant atoms chemi-sorb on a heated substrate through the thermal decomposition from a gaseous precursor (e.g., AsH_3, PH_3, B_2H_6). In the case of *n*-type doping, the chemi-sorption mechanism is self-limiting resulting in one single atomic layer (i.e. one monolayer) of dopant atoms (illustrated in Fig. 3). In the case of *p*-type doping, the self-limitation can be observed only at very low temperature, of the order of 100°C.

[0087] In the case of n-type doping (e.g. with As) the deposition is self-limited to 1 monolayer (ML). Below 1 ML, the deposited dose is determined by the duration of the exposure to the gaseous precursor (AsH_3), as shown in Figure 3 in the region labeled with (1).

[0088] Atomic Layer Epitaxy can be applied for in-situ doping of a semiconductor material. In this case, a layer of a semiconductor material (e.g. Si, Ge or SiGe) is epitaxially grown on top of a dopant layer already formed as illustrated in Fig 4.

[0089] The self-limitation of ALE to 1 monolayer of dopant is an additional advantage, since the dopant atoms can all be incorporated in substitutional sites during the epitaxial (over)growth of the semiconductor material. The growth processes are non-equilibrium processes which can be performed below the surface diffusion temperature of the dopants (related to the kinetics of the deposition process). In this way, very high active levels of doping can be obtained, above the dopant solid solubility. When the chemi-sorption is done on a Si (100) surface, the saturation dose (i.e. the dose of one monolayer) corresponds to a surface concentration of about $6.8x10^{14}$ atoms/cm^2.

[0090] The basic sequence that combines a dopant deposition step followed by the epitaxial overgrowth of a semiconductor layer can be repeated several times (or cycles). Each time, the overgrown semiconductor layer provides a fresh surface which allows the formation of a new dopant layer. This process is represented schematically in Figure 4.

[0091] Embodiments of the invention disclose depositing at least a fraction of a monolayer of a precursor suitable to form a dopant at a pressure between about 0.1 Pa and about 1 atm (101 kPa). The reaction chamber can be, for example, an epitaxial reactor, a low pressure chemical vapor deposition (LPCVD) chamber, a reduced pressure chemical vapor deposition (RPCVD) chamber, an atmospheric pressure chemical vapor deposition (APCVD) chamber or a ultra high vacuum chemical vapor deposition (UHVCVD) chamber, or a gas source molecular beam epitaxy chamber (GSMBE).

[0092] In specific embodiments of the invention a method is disclosed to improve the steepness of the doping profile at the interface between the emitter and the base region of a bipolar transistor (when compared to methods described in the art). Secondly, the method allows a good (or improved) control of the in-diffusion depth of the dopants at the emitter-base interface of a bipolar CMOS, upon applying the conventional activation anneal of the CMOS flow (when compared to methods described in the art).

[0093] Since the as-deposited dose can be varied with continuous values between 0 and 1 ML, ALE can be tuned to fit the profile steepness at the (emitter-base) interface and, at the same time, the diffusion length in the base (upon rapid thermal anneal).

[0094] The bulk of the emitter can be grown either by conventional in-situ doping techniques (e.g. Chemical Vapour Deposition (CVD) or by performing multiple cycles of ALE.

[0095] The emitter region can comprise multiple layers, each of them being epitaxially grown.

[0096] The sequence of dopant deposition (ALE) and epitaxial overgrowth of a semiconductor material such as Si, Ge, SiGe is repeated several times (Fig. 4). Because the overgrown layer provides a fresh surface for the dopant atoms, the dopant dose can be increased to any arbitrary value, provided that a sufficient amount of cycles is performed. Due to the layer growth, the thickness of the structure increases with the number of cycles.

[0097] If the exposure time is short enough during the ALE step, the substrate surface is not saturated by dopants. By an adequate choice of the exposure time, it is possible to tune the as-deposited dose at the required value (see e.g. figure 3 in the region labeled with (1)).

[0098] If ALE is followed by a (rapid) thermal treatment (or anneal), the dopant atoms will be activated in the semiconductor material. The maximum active dopant level that can be achieved is determined by the solid solubility limit at the anneal temperature. In the case of *n*-type dopants, without the deposition of a capping layer (or overgrown semiconductor material) immediately after the ALE step, most of the adsorbed atoms will desorb during the anneal step at temperatures higher than 550 °C -600°C. Therefore the semiconductor material must be grown/deposited at a temperature lower than the desorption temperature, to act as a protective cap layer with minimal alteration of the as-deposited dopant dose.

[0099] In Fig. 5a (and fig. 5b), secondary ion mass spectrometry (SIMS) measurements of the As concentration in the emitter layer are shown for 4 samples in the neighborhood of the physical interface between the emitter region (left hand side of the figure) and the base region (right hand side of the figure) (said transition region between the emitter region and the (base cap of the) base region indicated on top of said figure and depicted with the dashed line rectangle on said figure). In the as-deposited sample with the ALE (curve 3), the problem of the corner-rounded profile (curve 1) is solved, obtaining even a dopant concentration peak, with a magnitude of 6.2E20 at/cm^3. This magnitude of the concentration peak corresponds to 1 ML of As, but can be tuned/controlled

towards lower values, upon the requirements of a particular device, by depositing a fraction of a monolayer of arsine. The possibility to control the dopant overshoot (or concentration peak magnitude) is a particular advantage of the invention.

[0100] As a positive effect of ALE, the As concentration in the region (between -5 nm to -10 nm in said figure) of the overgrown layer close to the ALE peak (curve 3) is more uniform, compared to the profile of the sample without ALE (curve 1). Without being bound to theory, it is believed that the small dip in dopant (As) concentration at -14 nm is most probably due to the presence of Ge in the emitter or to a calibration issue of the SIMS measurement due to the presence of Ge.

[0101] After a spike anneal at 1085°C, the dopant (concentration) profile of the sample using ALE (curve 4) shows deeper in-diffusion compared to that of the sample without ALE (curve 2). The difference is due to the high amount of dopant (1 ML) that is available from the ALE, that acts as a reservoir of dopant atoms during the drive-in anneal. As indicated above, this amount of dopant can be reduced to a fraction of a monolayer in order to adjust the in-diffusion depth upon needs.

[0102] Fig. 6a (and fig. 6b) represents the results of TCAD simulations of an emitter grown using the (multiple) ALE.

[0103] Figure 6a shows the ALE peaks (1) (grey) to (5) (dashed black) with increasing magnitude. Figure 6b shows the corresponding in-diffusion depth after a spike anneal at 1085°C for the ALE peaks (1) to (5).

[0104] The simulations show that a proper tuning of the magnitude of the ALE peak close to the emitter/base interface allow to control the in-diffusion length after (or upon) the (rapid) thermal anneal.

[0105] The higher the ALE peak magnitude (i.e. the distance measured from the top of the (grey) peak (1) to the top of the (black-dashed) peak (5) in Fig 6a the higher is the in-diffusion depth (measured in microns on the x-scale) in the direction indicated by the arrow in Fig 6b (i.e. from the grey curve (1) to the black-dashed curve (5)). Upon anneal, the other ALE peaks in the bulk emitter region are leveled off at the same bulk concentration in the emitter.

[0106] The present invention can be applied in different areas of semiconductor device manufacturing. While the invention is described in conjunction with a bipolar transistor and more particularly to a bipolar CMOS (BiCMOS) device, it will be apparent to those ordinary skilled in the art that the benefits of this invention can be applied to other applications. Another possible application is growing thin highly doped semiconductor layers on a substrate. The method of the invention can be used e.g. to form thin n+ Si layer for photovoltaic applications or to control the dopant (concentration) profile at the emitter-base junction in a photovoltaic device.

[0107] It is to be understood that although preferred embodiments, specific constructions and configurations, as well as materials, have been discussed herein for devices according to the present invention, various changes or modifications in form and detail may be made without departing from the scope of this invention as defined by the appended claims.

Claims

1. A method for manufacturing a junction with a controlled dopant profile comprising the steps of:

   - forming a first semiconductor material comprising a first dopant having a first concentration and thereupon
   - forming a second semiconductor material comprising a second dopant, having a second concentration thereby forming a junction, wherein the second dopant is a n-type dopant, and wherein the second semiconductor material is formed at a temperature lower than the second dopant desorption temperature, and
   - depositing by Atomic Layer Epitaxy or Vapor Phase Doping at least a fraction of a monolayer of a precursor suitable to form the second dopant on the first semiconductor material, prior to forming the second semiconductor material, thereby increasing the second concentration of the second dopant at the junction between the first and the second semiconductor material.

2. The method according to claim 1, wherein the first semiconductor material and the second semiconductor material have the same composition, thereby forming a homojunction.

3. The method according to claim 1, wherein the first semiconductor material and the second semiconductor material have different compositions, thereby forming a heterojunction.

4. The method according to any of claims 1 to 3, wherein forming the second semiconductor material comprises

   - performing a sequence consisting of

     - epitaxially growing a layer of a second semiconductor material and thereupon
     - depositing by Atomic Layer Epitaxy a monolayer of a precursor suitable to form the second dopant

   - repeating the sequence at least twice, thereby incorporating the second dopant in substitutional sites in the second semiconductor material.

5. The method according to any of claims 1 to 4, wherein the second concentration of the second dopant in

the second semiconductor material is higher or equal to $1x10^{20}$ cm^{-3}.

6. The method according to claim 1, wherein the n-type dopant is arsenic (As) or phosphorus (P).

7. The method according to any of claims 1 to 6, wherein the first dopant is a p-type dopant.

8. The method according to claim 7, wherein the p-type dopant is boron.

9. The method according to any of claims 1 to 8, wherein the second semiconductor material comprises Si, Ge or combinations thereof.

10. The method according to any of claims 1 to 9, wherein the second semiconductor material is an emitter region of a bipolar transistor.

11. The method according to any of claims 1 to 10, wherein the first semiconductor material comprises Si, Ge or combinations thereof.

12. The method according to any of claims 1 to 11, wherein the first semiconductor material is a base region of a bipolar transistor.

13. The method according to any of claims 1 to 12, further comprising a rapid thermal treatment.

Patentansprüche

1. Verfahren zum Herstellen eines Übergangs mit einem kontrollierten Dotiermittelprofil, das die Schritte umfasst:

   - Bilden eines ersten Halbleitermaterials, das ein erstes Dotiermittel mit einer ersten Konzentration umfasst und darauf
   - Bilden eines zweiten Halbleitermaterials, das ein zweites Dotiermittel umfasst, mit einer zweiten Konzentration, wodurch ein Übergang gebildet wird, wobei das zweite Dotiermittel ein n-Typ-Dotiermittel ist, und wobei das zweite Halbleitermaterial bei einer Temperatur geringer als die Desorptionstemperatur des zweiten Dotiermittels gebildet wird, und
   - Abscheiden zumindest einer Fraktion einer Monolage eines Vorläufers, dazu geeignet, das zweite Dotiermittel auf dem ersten Halbleitermaterial zu bilden, durch Atomlagenepitaxie oder Dampfphasendotierung, bevor das zweite Halbleitermaterial gebildet wird, wodurch die zweite Konzentration des zweiten Dotiermittels am Übergang zwischen dem ersten und dem zweiten Halbleitermaterial erhöht wird.

2. Verfahren nach Anspruch 1, wobei das erste Halbleitermaterial und das zweite Halbleitermaterial die gleiche Zusammensetzung aufweisen, wodurch ein Homoübergang gebildet wird.

3. Verfahren nach Anspruch 1, wobei das erste Halbleitermaterial und das zweite Halbleitermaterial unterschiedliche Zusammensetzungen aufweisen, wodurch ein Heteroübergang gebildet wird.

4. Verfahren nach einem der Ansprüche 1 bis 3, wobei das Bilden des zweiten Halbleitermaterials umfasst

   - Durchführen einer Sequenz, bestehend aus

     - epitaktischem Züchten einer Lage eines zweiten Halbleitermaterials und darauf
     - Abscheiden einer Monolage eines Vorläufers, dazu geeignet, das zweite Dotiermittel zu bilden, durch Atomlagenepitaxie

   - Wiederholen der Sequenz zumindest zweimal, wodurch das zweite Dotiermittel in Substitutionsstellen im zweiten Halbleitermaterial integriert wird.

5. Verfahren nach einem der Ansprüche 1 bis 4, wobei die zweite Konzentration des zweiten Dotiermittels im zweiten Halbleitermaterial größer gleich 1×10^{20} cm^{-3} ist.

6. Verfahren nach Anspruch 1, wobei das n-Typ-Dotiermittel Arsen (As) oder Phosphor (P) ist.

7. Verfahren nach einem der Ansprüche 1 bis 6, wobei das erste Dotiermittel ein p-Typ-Dotiermittel ist.

8. Verfahren nach Anspruch 7, wobei das p-Typ-Dotiermittel Bor ist.

9. Verfahren nach einem der Ansprüche 1 bis 8, wobei das zweite Halbleitermaterial Si, Ge oder Kombinationen davon umfasst.

10. Verfahren nach einem der Ansprüche 1 bis 9, wobei das zweite Halbleitermaterial ein Emitterbereich eines bipolaren Transistors ist.

11. Verfahren nach einem der Ansprüche 1 bis 10, wobei das erste Halbleitermaterial Si, Ge oder Kombinationen davon umfasst.

12. Verfahren nach einem der Ansprüche 1 bis 11, wobei das erste Halbleitermaterial ein Basisbereich eines bipolaren Transistors ist.

13. Verfahren nach einem der Ansprüche 1 bis 12, das ferner eine schnelle Wärmebehandlung umfasst.

Revendications

1. Procédé de fabrication d'une jonction avec un profil de dopant contrôlé comprenant les étapes suivantes :

   - formation d'un premier matériau semi-conducteur comprenant un premier dopant ayant une première concentration puis, sur celui-ci,
   - formation d'un deuxième matériau semi-conducteur comprenant un deuxième dopant, ayant une deuxième concentration, formant ainsi une jonction, le deuxième dopant étant un dopant de type n et le deuxième matériau semi-conducteur étant formé à une température inférieure à la température de désorption du deuxième dopant et
   - dépôt, par épitaxie par couche atomique ou dopage en phase vapeur d'au moins une fraction d'une monocouche d'un précurseur convenant à la formation d'un deuxième dopant sur le premier matériau semi-conducteur, avant la formation du deuxième matériau semi-conducteur, augmentant ainsi la deuxième concentration du deuxième dopant au niveau de la jonction entre le premier et le deuxième matériau semi-conducteur.

2. Procédé selon la revendication 1, dans lequel le premier matériau semi-conducteur et le deuxième matériau semi-conducteur présentent la même composition, formant ainsi une homo-jonction.

3. Procédé selon la revendication 1, dans lequel le premier matériau semi-conducteur et le deuxième matériau semi-conducteur présentent des compositions différentes, formant ainsi une hétéro-jonction.

4. Procédé selon l'une des revendications 1 à 3, dans lequel la formation du deuxième matériau semi-conducteur comprend

   - la réalisation d'une séquence consistant en

     - la croissance épitaxiale d'une couche d'un deuxième matériau semi-conducteur puis, sur celle-ci,
     - le dépôt par épitaxie par couche atomique ou dopage en phase vapeur d'une monocouche d'un précurseur conçu pour former le deuxième dopant
     - la répétition de la séquence au moins deux fois, ce qui permet d'incorporer le deuxième dopant dans des sites de substitution dans le deuxième matériau semi-conducteur.

5. Procédé selon l'une des revendications 1 à 4, dans lequel la deuxième concentration du deuxième dopant dans le deuxième matériau semi-conducteur est supérieur ou égal à $1x10^{20}$ cm^{-3}.

6. Procédé selon la revendication 1, dans lequel le dopant de type n est de l'arsenic (As) ou du phosphore (P).

7. Procédé selon l'une des revendications 1 à 6, dans lequel le premier dopant est un dopant de type p.

8. Procédé selon la revendication 7, dans lequel le dopant de type p est le bore.

9. Procédé selon l'une des revendications 1 à 8, dans lequel le deuxième matériau semi-conducteur comprend du Si, du Ge ou des combinaisons de ceux-ci.

10. Procédé selon l'une des revendications 1 à 9, dans lequel le deuxième matériau semi-conducteur est une région d'émetteur d'un transistor bipolaire.

11. Procédé selon l'une des revendications 1 à 10, dans lequel le premier matériau semi-conducteur comprend du Si, du Ge ou des combinaisons de ceux-ci.

12. Procédé selon l'une des revendications 1 à 11, dans lequel le premier matériau semi-conducteur est une région de base d'un transistor bipolaire.

13. Procédé selon l'une des revendications 1 à 12, comprenant en outre un traitement thermique rapide.

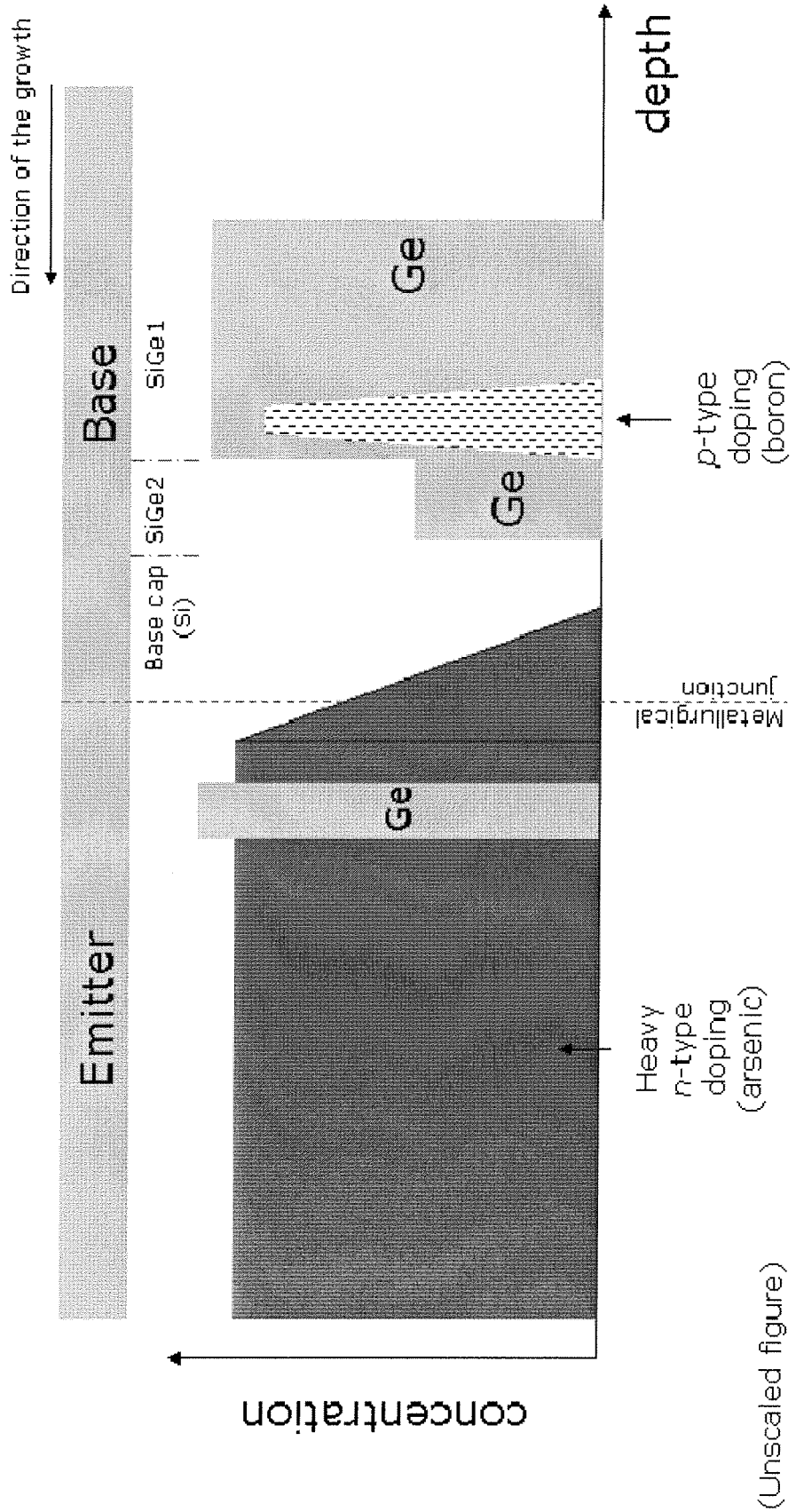
Direction of the growth
Emitter
Base
SiGe1
Base cap (Si)
SiGe2
Ge
Ge
Ge
depth
p-type doping (boron)
Metallurgical junction
Heavy n-type doping (arsenic)
concentration
(Unscaled figure)

FIG. 1a

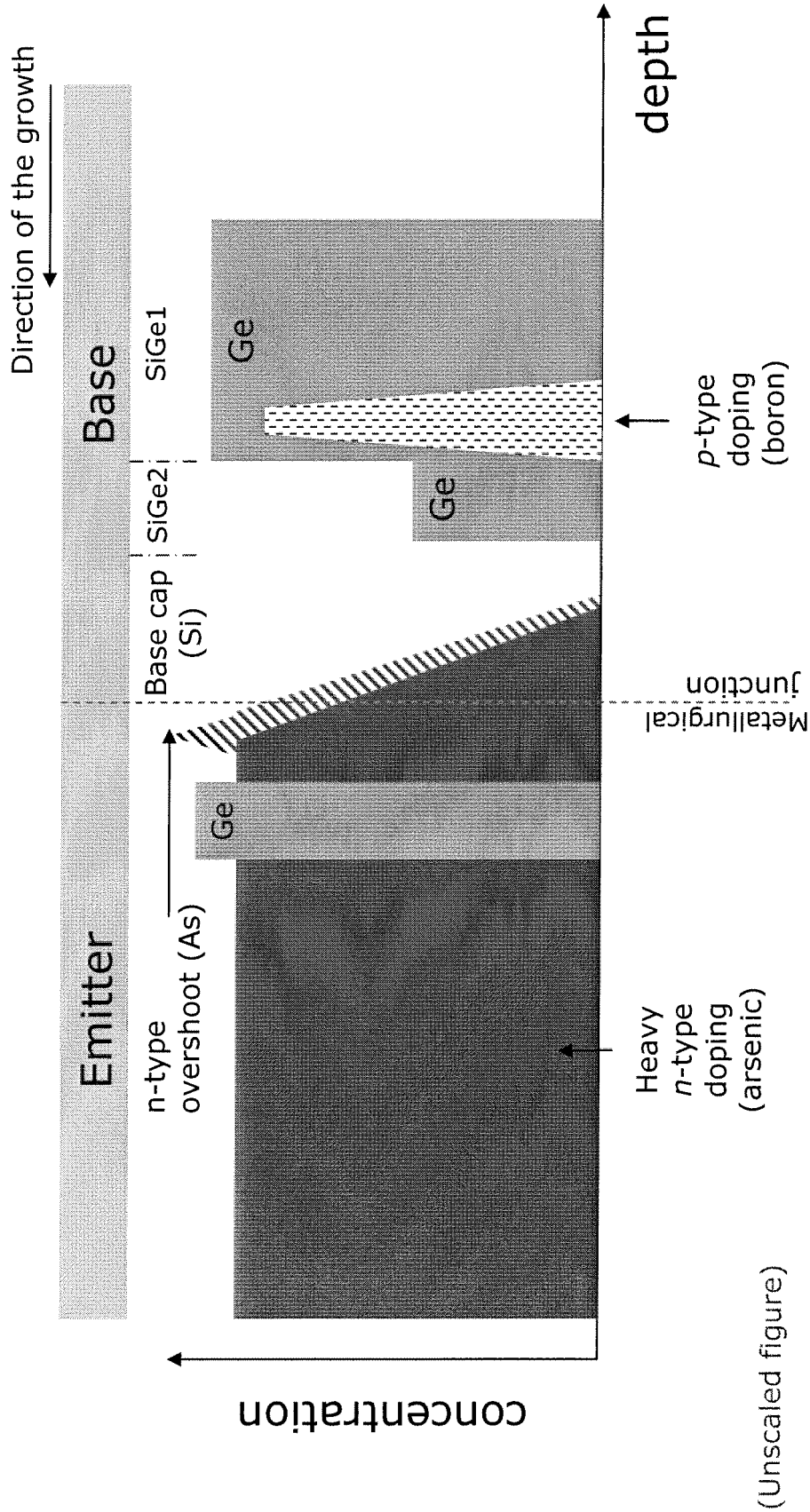
Direction of the growth
Emitter
Base
SiGe1
SiGe2
Base cap (Si)
Ge
Ge
Ge
n-type overshoot (As)
Metallurgical junction
p-type doping (boron)
Heavy n-type doping (arsenic)
concentration
depth
(Unscaled figure)

FIG. 1b

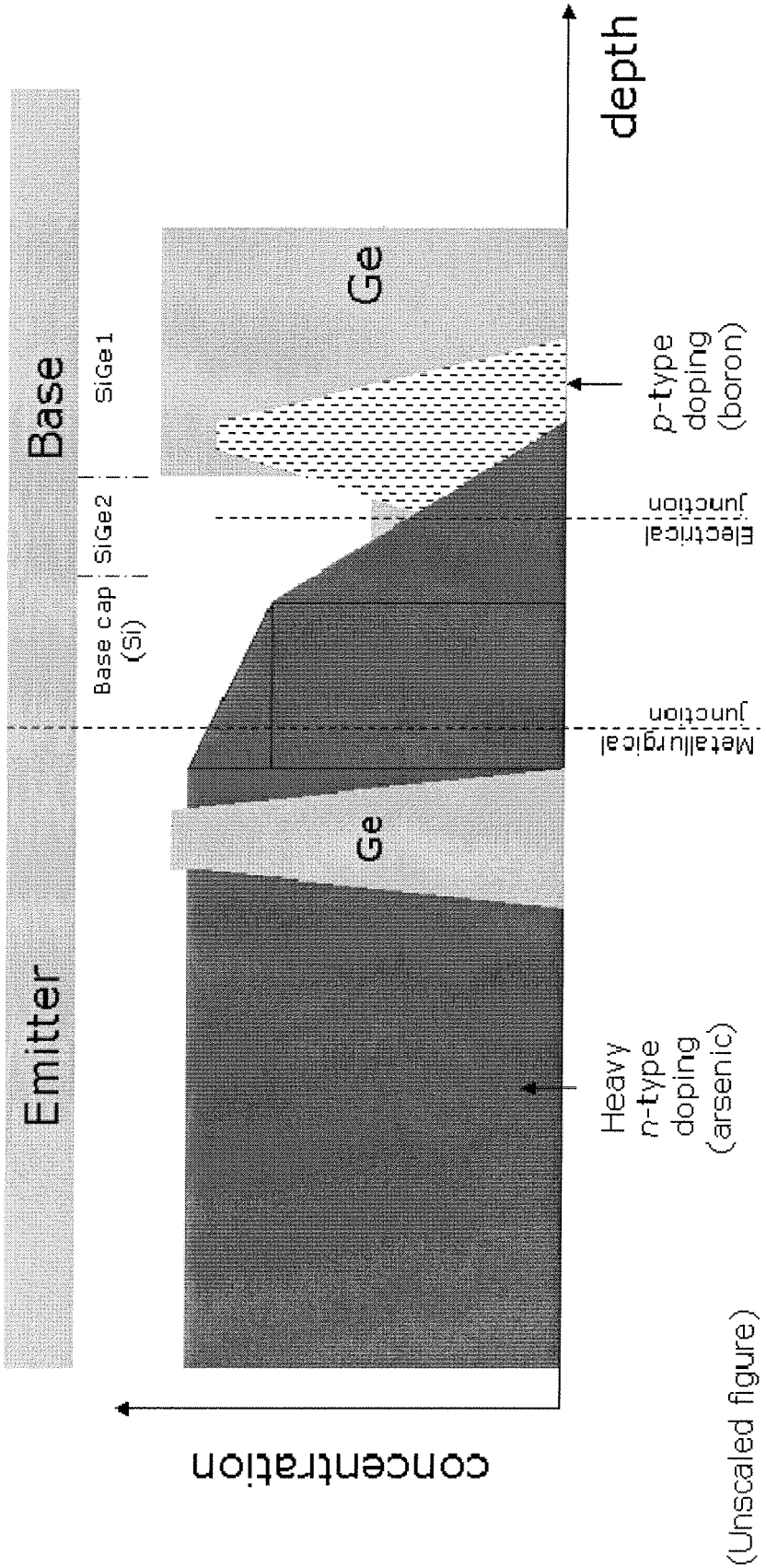
depth
Ge
Base
SiGe1
SiGe2
Base cap (Si)
p-type doping (boron)
Electrical junction
Metallurgical junction
Ge
Emitter
Heavy n-type doping (arsenic)
concentration
(Unscaled figure)

FIG. 2a

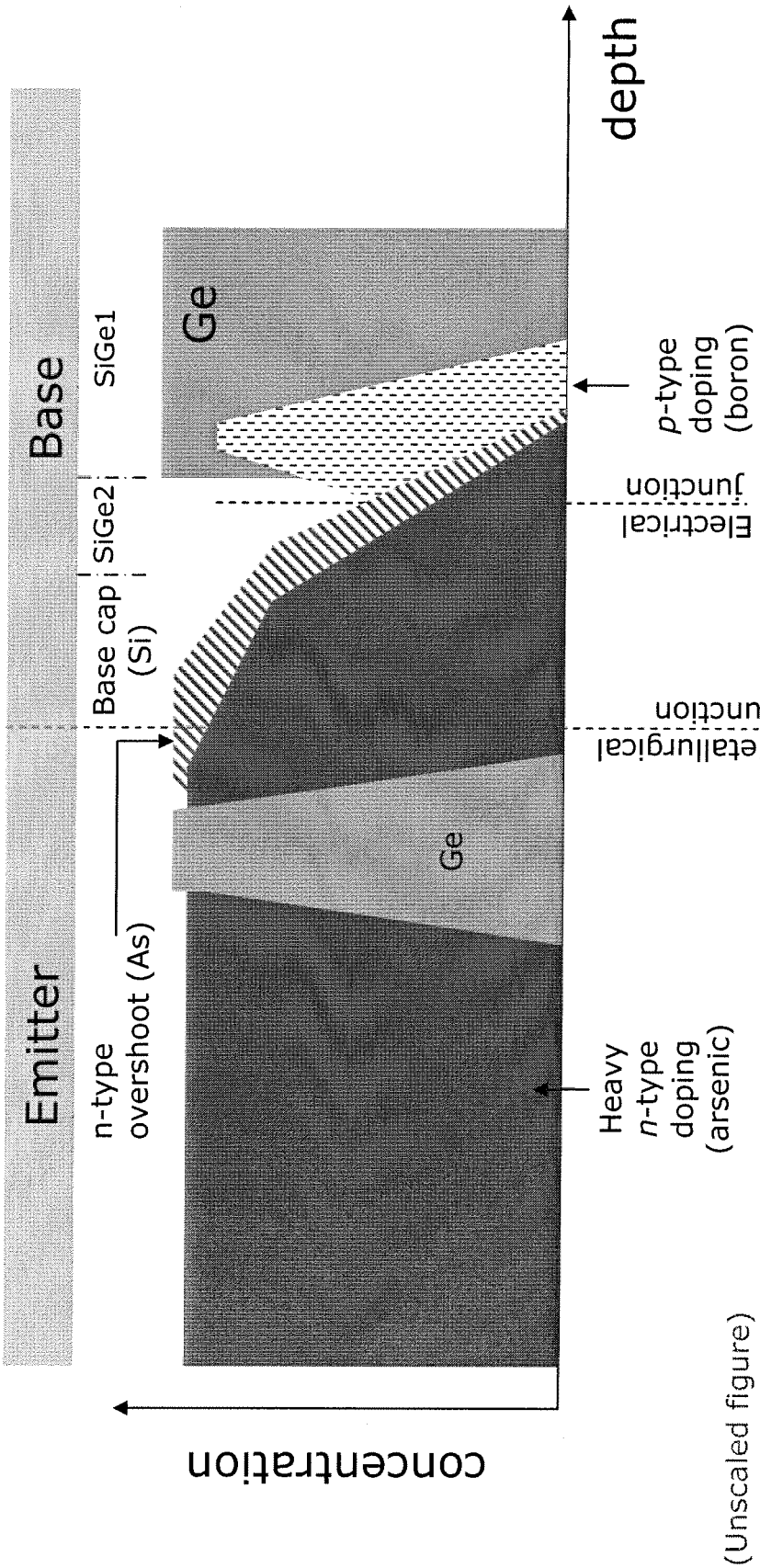
depth
Emitter
Base
SiGe1
Ge
Base cap (Si)
SiGe2
n-type overshoot (As)
Ge
p-type doping (boron)
Electrical junction
Metallurgical junction
Heavy n-type doping (arsenic)
concentration
(Unscaled figure)

FIG. 2b

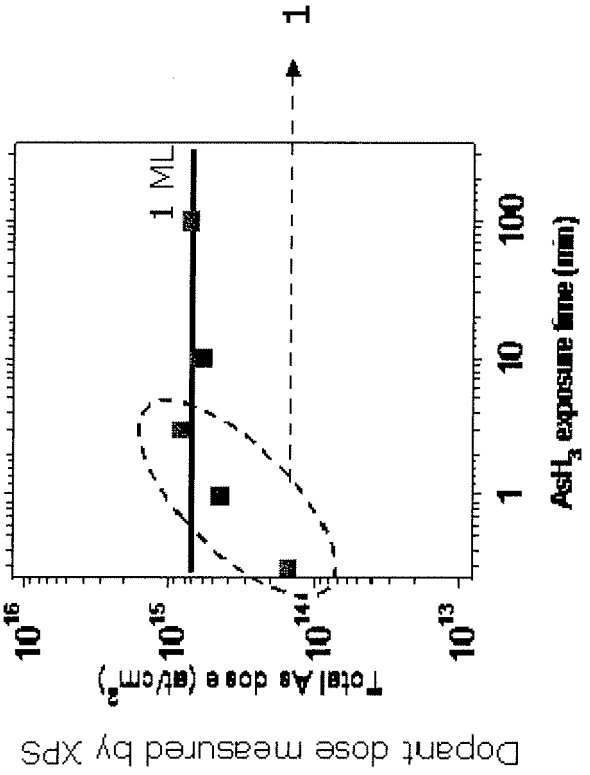
1
1 ML
10^{16}
10^{15}
10^{14}
10^{13}
1
10
100
AsH_3 exposure time (min)
Total As dose (at/cm^2)
Dopant dose measured by XPS

FIG. 3

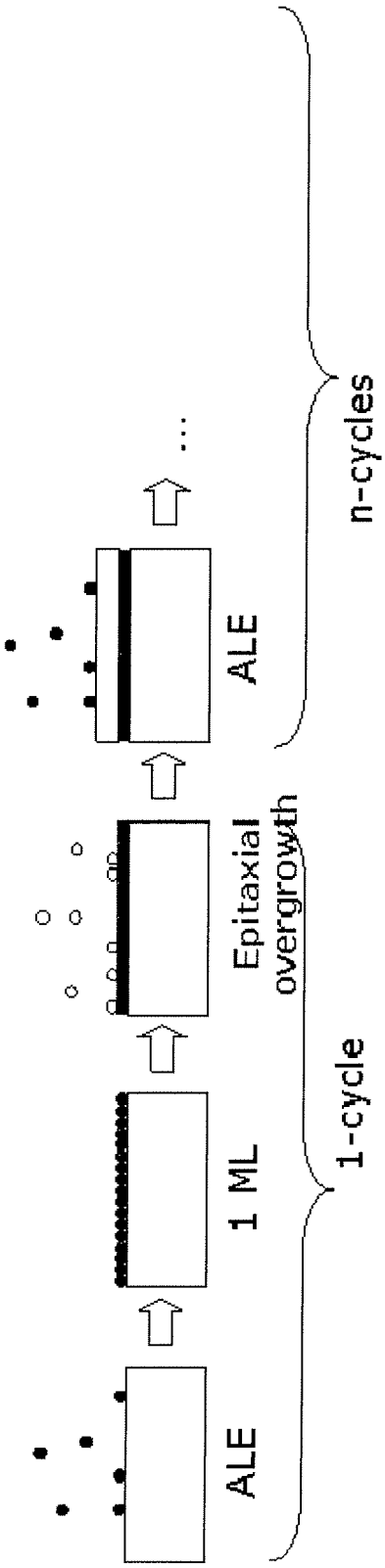

FIG. 4

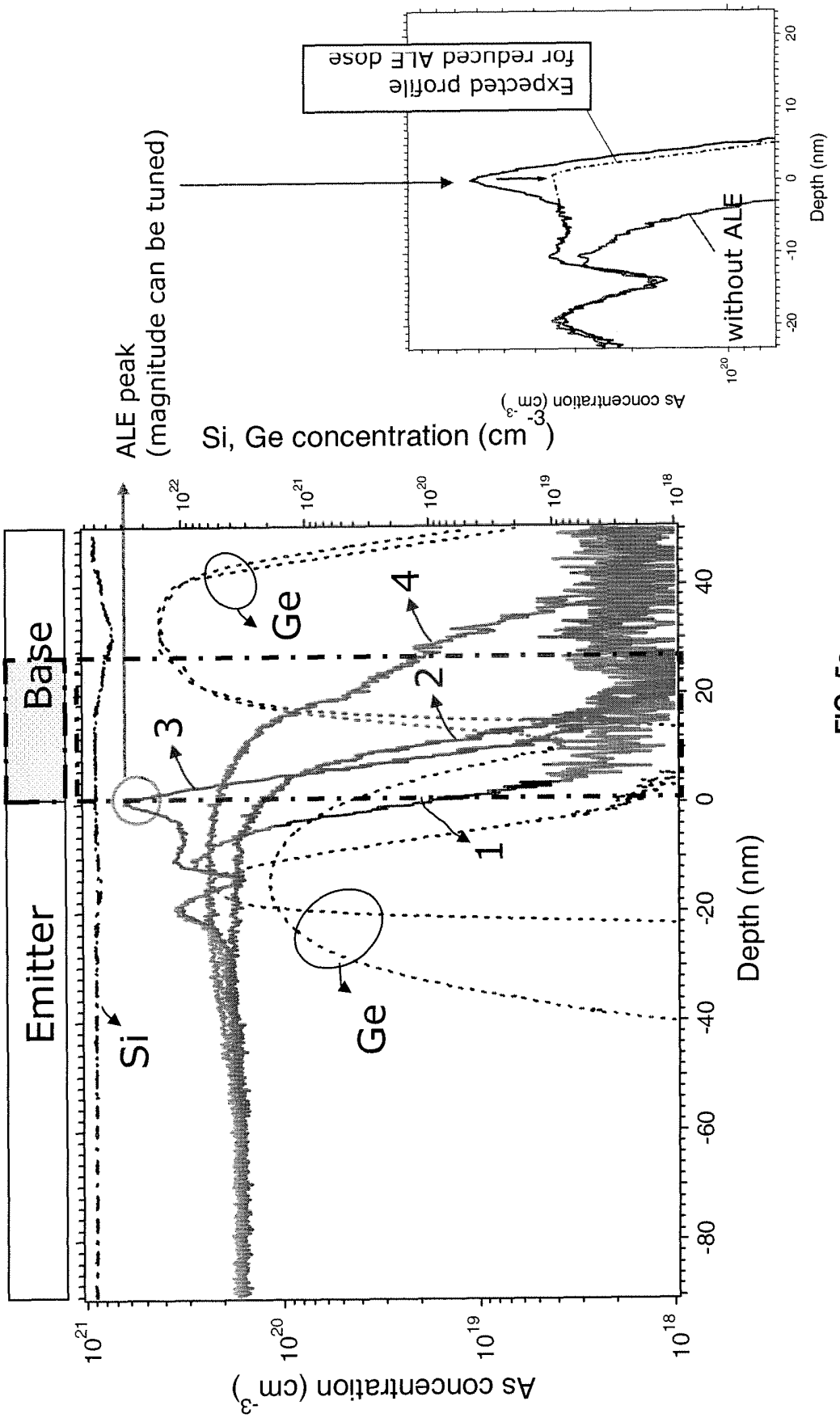
Expected profile
for reduced ALE dose
without ALE
Depth (nm)
As concentration (cm-3)
ALE peak
(magnitude can be tuned)
Si, Ge concentration (cm-3)
Base
Emitter
Si
Ge
Ge
1
2
3
4
Depth (nm)
As concentration (cm-3)

FIG. 5a

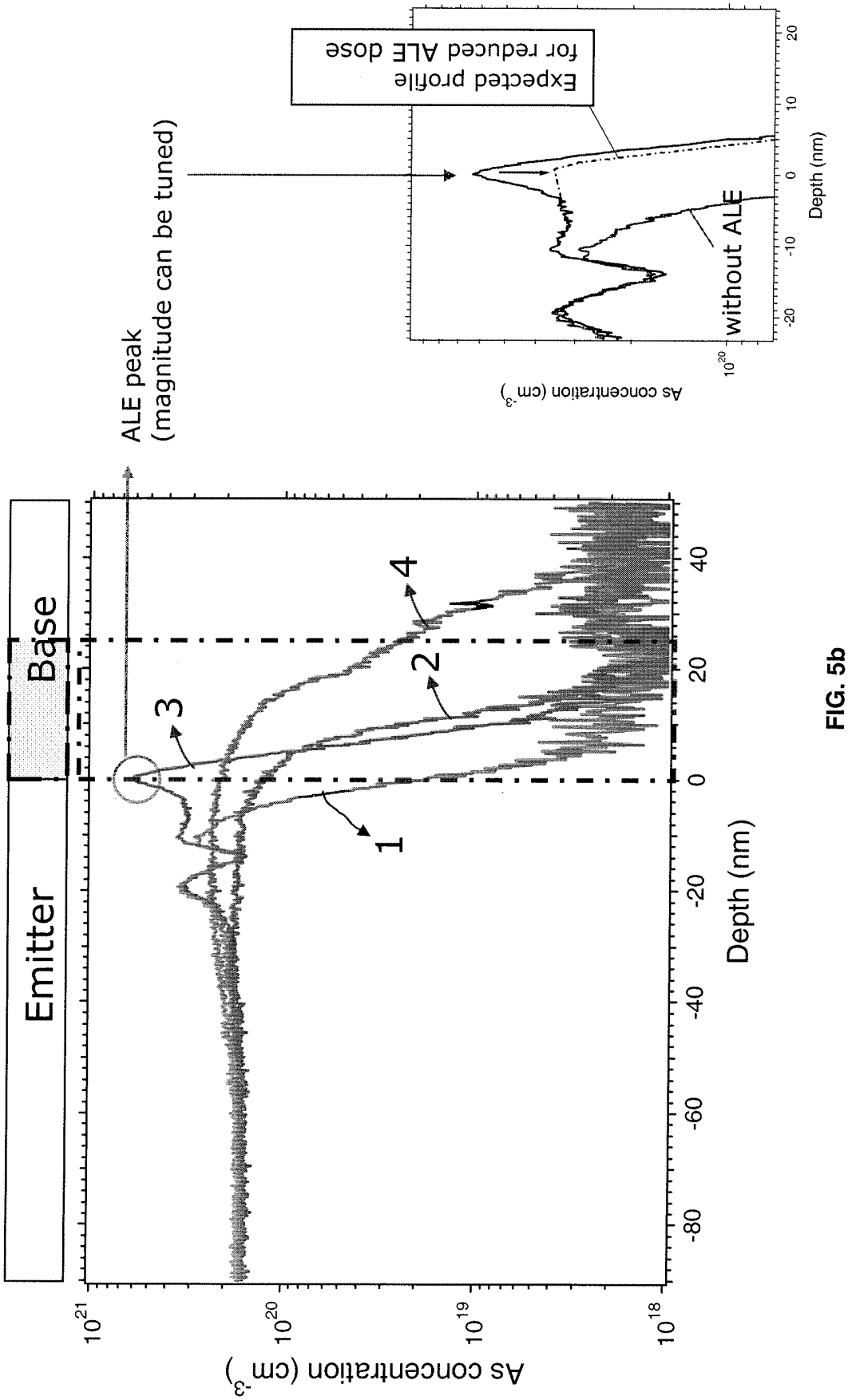
Emitter
Base
ALE peak
(magnitude can be tuned)
1
2
3
4
As concentration (cm-3)
Depth (nm)
Expected profile
for reduced ALE dose
without ALE

FIG. 5b

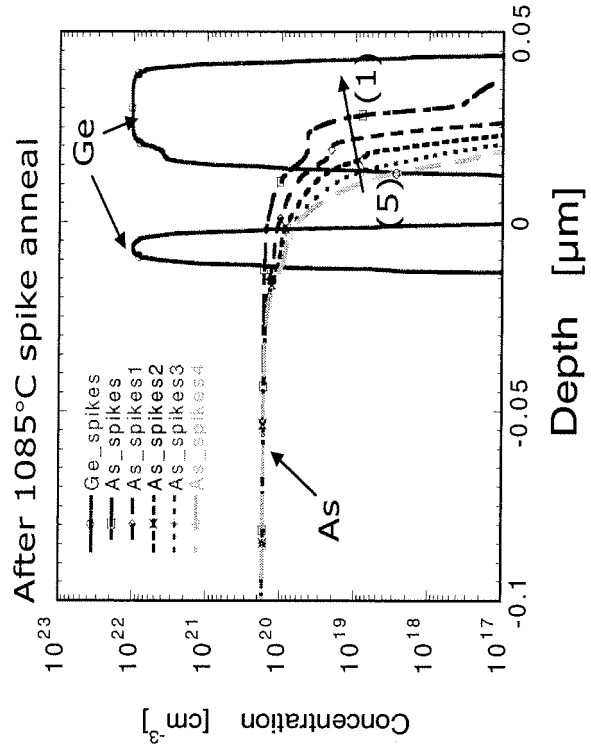
After 1085°C spike anneal
Ge
As
(1)
(5)
Ge_spikes
As_spikes
As_spikes1
As_spikes2
As_spikes3
As_spikes4
Concentration [cm-3]
Depth [µm]

FIG. 6b

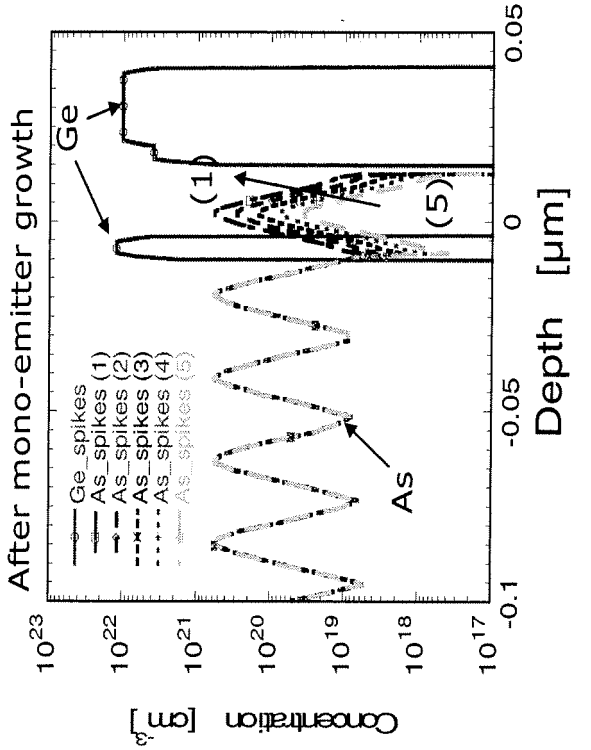
After mono-emitter growth
Ge
As
(1)
(5)
Ge_spikes
As_spikes (1)
As_spikes (2)
As_spikes (3)
As_spikes (4)
As_spikes (5)
Concentration [cm-3]
Depth [µm]

FIG. 6a

REFERENCES CITED IN THE DESCRIPTION

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- EP 1178537 A **[0006]**

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- **SHIMAMUNE, Y. et al.** Atomic-layer doping in Si by alternately supplied PH3 and SiH. *Thin Solid Films,* 2000, vol. 380, 134-136 **[0007]**
- **SCHUBERT, E. F.** Delta doping of semiconductors. Cambridge University Press, 1996, 4 **[0008]**
- **TILLACK, B. et al.** Atomic layer processing for doping of SiGe. *Thin Solid Films,* 2006, vol. 508, 279-283 **[0009]**