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Growth of III/V Materials On Large Area Silicon

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Continuous miniaturization has been at the heart of advances in modern semiconductor electronics. However, further scalability has seen its limits for conventional CMOS technology due to short channel effects. To further increase the performance for the 32 and 22 nm nodes, channel engineering introducing III-V materials may be necessary. Hence, epitaxial growth and processing strategies have to be developed which combine the high complexity of an MOCVD growth chamber with the requirements of the silicon industry.

Introduction

The compound semiconductor industry has seen tremendous progress in applications ranging from high-power electronics to optoelectronics. However, most of the devices being produced today are discrete due to the comparatively high cost of wafer area and the low level of integration experience compared to the silicon industry. Hence, co-integration with mainstream silicon manufacturing processes in which the compound semiconductor device is selectively deposited in areas where needed while the rest of the chip is kept in standard silicon VLSI technology is seen as one of the most promising ways to harvest the potential of III-V compounds.

Integration Strategies

One such potential device integration concept is the combination of CMOS logic circuitry with selectively grown laser and detector structures based on the GaNAsP-material system for inter- and intra-chip communication [1,2]. The suppression of anti-phase domains, the handling of the different thermal expansion coefficients and the provision of charge neutrality at the interface are of paramount interest [3,4].

On the other hand, in the field of state-of-the-art conventional CMOS technology such as for logic applications, continuing the aggressive scaling as predicted by the ITRS roadmap will require new channel materials [5]. Its high hole carrier mobility makes Germanium the natural alternative material of choice, however, suffers from underperforming Ge n-MOSFET devices. Thus, the selective co-integration of Ge p-MOSFETs with III/V-based n-FETs to form a complementary logic in areas of the chip which require high clock rates is seen as one possible solution to the problem [6].

To pave these future roads, III-V equipment manufacturers are faced with the challenge of adapting their specialized (and usually stand-alone) tools to the requirements of the silicon industry. Most notably automation, cross-contamination of the Si processing line with III-V elements which act as dopants and particle specifications are among the toughest challenges to be met.

Growth Chamber Design

We report on the successful adaptation of the Crius® Close-Coupled Showerhead (CCS) technology for the Metal-Organic Chemical Vapor Deposition (MOCVD) of nitride and arsenide/phosphide III-V devices to the requirements of growth on 200 mm to 300 mm Si wafers (see Figure 1).

Figure 1: Photo of an industry compatible cluster with two AIXTRON CCS MOCVD tools attached. Inset: view of the opened reactor with 300 mm Si wafer and shower-head.

Extensive numerical modeling was employed to assure the thermal uniformity of the tool during the heat-up and cool-down phases which are extremely critical due to the tendency of Si to form slip-lines. The model includes the heat transfer from the 3-zone resistive heater to the wafer carrier and the heat transfer through differently shaped wafer pockets to the wafer. Here, the wafer contact on the outer rim, the optimization of the geometry of the outer rim and the curvature of the wafer pocket to compensate for spherical bow due to strain were at the center of the investigation.

Figure 2 shows numerical modeling results for the temperature optimization on the wafer with the heater zones kept constant at $T_A = 1423°C$, $T_B = 1477°C$, and $T_C = 1677°C$ from center to edge. It becomes imminently clear that the careful design of the wafer bearing and the curvature of the wafer pocket allows a reduction of the influence of the thermal contact at the edge of the wafer, hereby reducing the rise in temperature at the edge from almost $\Delta T = 22$ K down to 9.2 K. Further reduction can now be achieved by fine tuning the heating power to the heater zones.

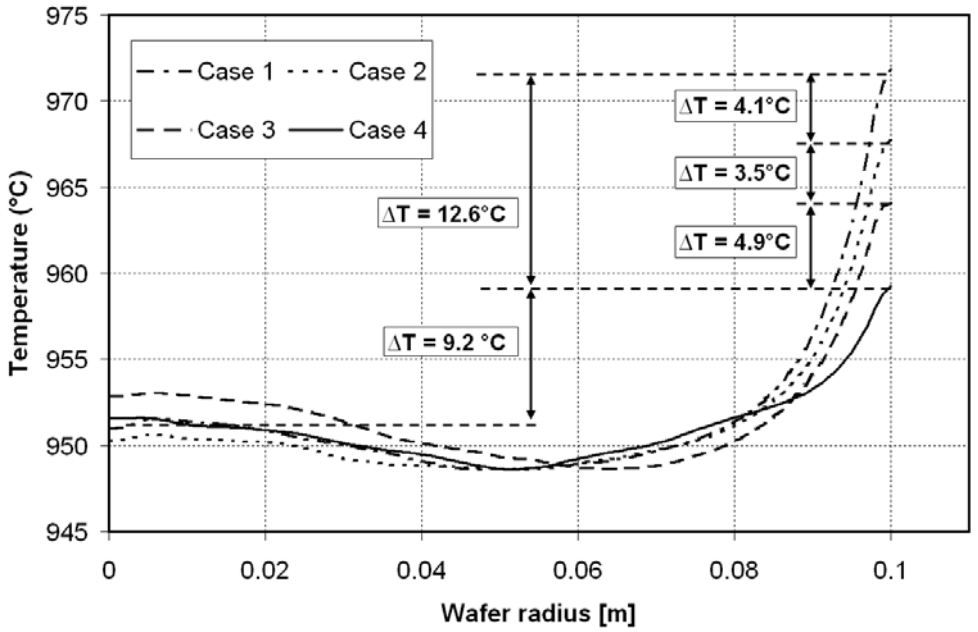

Figure 2: Temperature traces along the wafer radius from center to outer edge for 4 different cases of wafer carrier design.

Experimental Results

One concept to co-integrate Si-, Ge- and GaAs-based devices on the same chip is to employ Ge-on-Si (GOS) substrates and overgrowing a highly uniform GaAs-layer. We studied the growth of such GaAs-layers on 200 mm diameter Si-substrates using the newly developed growth machine.

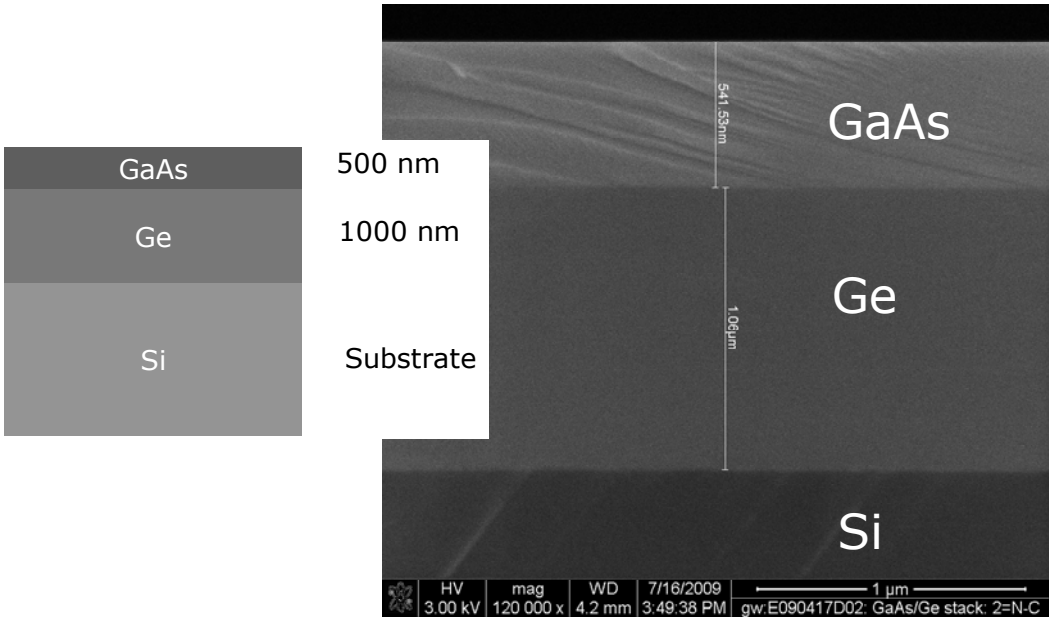

Figure 3: Cross-sectional SEM micrograph of a GaAs-layer overgrown on a GOS-substrate. Inset: sketch of the targeted layer thicknesses.

Figure 3 shows a cross-sectional scanning electron micrograph (SEM) of the GaAs layer on a GOS substrate. As can be seen the GaAs layer is of high quality without observable disturbances at the Ge/GaAs interface. The GaAs layer thickness was determined to be 541 nm on average across the wafer with a standard deviation of the thickness of 0.2% (based on 5 measurement points across the wafer diameter).

Conclusion and Outlook

The demand for the convergence of III-V technologies with the CMOS silicon industry has led to the development of cluster MOCVD tools which can be integrated into standard silicon processing lines. First growth experiments of GaAs on GOS substrates show good results in terms of uniformity across the wafer diameter and the general layer properties. This renders the III-V on Si approach a promising strategy to overcome the challenges faced by the Si-industry for further scalability of Si-chips.

Further experiments are focused on n- and p-type doping, the growth of ternary and quaternary compounds and the selective growth of such materials using masking of the wafer surface.

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