Growth of high quality InP layers in STI trenches on miscut Si (0 0 1) substrates

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Abstract

In this work, we report the selective area epitaxial growth of high quality InP in shallow trench isolation (STI) structures on Si (0 0 1) substrates 61 miscut toward (1 1 1) using a thin Ge buffer layer. We studied the impact of growth rates and steric hindrance effects on the nano-twin formation at the STI side walls. It was found that a too high growth rate induces more nano-twins in the layer and results in InP crystal distortion. The STI side wall tapering angle and the substrate miscut angle induced streric hindrance between the InP facets and the STI side walls also contribute to defect formation. In the [$\bar{1}$ 1 0] orientated trenches, when the STI side wall tapering angle is larger than 10°, crystal distortion was observed while the substrate miscut angle has no significant impact on the InP defect formation. In the [$\bar{1}$ 1 0] trenches, both the increased STI tapering angle and the substrate miscut angle induce high density of defects. With a small STI tapering angle and a thin Ge layer, we obtained extended defect free InP in the top region of the [1 1 0] trenches with aspect ratio larger than 2.

Keywords : A3. Metalorganic vapor phase epitaxy ; B1. Phosphides ; B2. Semiconducting III–V materials

1. INTRODUCTION

InP epitaxial layers are extensively used in high frequency and optoelectronic devices due to their high electron mobility and more often they are used as the buffer layer for InGaAs active layers [1,2]. Selective area growth (SAG) is widely used in III-V heterojunction bipolar transistor devices and photonic integrated circuits [3,4]. To extend the advantage of the high electron mobility of III-V zincblende compound semiconductor materials to complementary metal oxide semiconductor (CMOS) logic devices, there is a great interest in integrating InP and other high mobility materials like InGaAs on Si substrates. One approach to integrate these materials on Si substrates is SAG in shallow trench isolated (STI) structures [5,6]. Using this approach, it should be possible to obtain extended defect free areas by the so-called defect necking effect [7]. This would enable an alternative route for making III-V channel nMOS devices. SAG also provides the possibility of making Ge channel based pMOS in the vicinity of III-V channel based nMOS devices so that high performance CMOS devices can be realized on a single Si substrate [8]. In addition, the integration of optoelectronic devices on a Si chip likely needs SAG of III-V materials on dedicated Si areas.

Previous reports have demonstrated that the defect necking effect is limited to trenches with aspect ratio (depth to width) greater than 2 [7,9,10]. pMOS device performance boost on Ge selectively grown in STI trenches has been demonstrated recently [11]. Tang et al. [12] and Li et al. [5] reported InP SAG on exact Si (0 0 1). However, for zincblende III-V compound semiconductor epitaxial layers grown on Si (0 0 1) or Ge (0 0 1) substrates, the reduced symmetry of III-V compounds induces antiphase (domain) boundaries (APBs). These APBs are either in {1 1 1} or in {1 1 0} planes. The APBs in {1 1 0} will penetrate to the surface. Although APBs in {1 1 1} were found to annihilate in a few micrometer thick InP layer on exact Si (0 0 1) [12], it is not clear whether they can be effectively suppressed in shallow trenches, especially within a thickness of 300 nm, a typical STI depth. To avoid APBs, miscut Si (0 0 1) or Ge (0 0 1) substrates have been used in previous studies [13-15].

In this work, we report SAG of high quality InP in STI trenches on miscut Si (0 0 1) substrates. On Si (0 0 1) substrates with 61 miscut toward (1 1 1), we studied the impact of local growth rates and trench orientation on defect formation and a model is proposed to explain the preferential occurrence of planar defects like stacking faults (SFs) and nano-twins in [$\bar{1}$ 1 0] oriented trenches. With optimized growth conditions, we obtained extended defect free InP in the top region of [1 1 0] trenches with aspect ratio larger than 2.

2. EXPERIMENTAL

200 mm Si (0 0 1) substrates with 61 miscut toward (1 1 1) were used. A standard STI process, widely used in Si-CMOS technologies, was employed to make the trenches for InP SAG. The trench formation is described in more detail in Refs. [6,16]. The result is that our starting STI wafers have 300 nm thick embedded SiO_2 and, by selective etch of Si with HCl vapor, trenches are formed. The wafers expose Si (0 0 1) trenches of width from 0.1 to 100 mm (trench lengths are one order larger than the widths), separated by SiO_2 sidewalls. The trenches

were aligned in [1 1 0] and [$\bar{1}$ 1 0] directions. About 40% of the total Si wafer surface was exposed for the InP deposition. In an ASM-Epsilon 2000 reactor [16], following the Si etch, a thin (40 nm) Ge layer was grown at 450 °C and atmospheric pressure using GeH_4 (1% in H_2) in H_2 carrier gas. From Ref. [5], it is known that a very high density of twins is present in InP grown directly on Si. Thus an intermediate layer is required. A thin Ge layer is considered to be a suitable intermediate layer between Si and the III-V material for a number of reasons. First of all, this thin Ge layer mitigates the lattice mismatch between the InP and Si substrates. Secondly, although a GaAs intermediate layer has also been proposed for a similar reason [5], we found the selectivity of GaAs is much worse compared with that of Ge. Thirdly, the highest possible susceptor temperature in our Thomas Swan MOVPE tool is 750 °C, which is not enough to clean the native SiO_2 on Si substrates while the Ge surface can be oxygen-free above 600 °C.

After unloading the 200 mm wafers, they were cleaved into 50• 50 mm^2 pieces and loaded into an Aixtron/ Thomas Swan close coupled showerhead metalorganic vapor phase epitaxy (MOVPE) reactor. Trimethylindum (TMIn) was used as the group-Ill element precursor. For the group V element, tertiarybutylarsine (TBAs) and tertiarybutylphosphine (TBP) were available. Before the growth, a pre-epi bake at 680 °C and 450 Torr with TBAs and H_2 carrier gas was carried out to remove the Ge native oxide and to promote double step formation. Following this bake, the temperature was ramped down to 420 °C to grow ~30 nm InP seed layers at 450 Torr with V/III=300. Optimization of the seed layer has been reported in Ref. [6]. In agreement with previous work [17], we found the As-terminated Ge surface the most suitable for subsequent III-V growth. After the growth of the InP seed layer, the temperature was ramped to 640 °C for the bulk InP layer growth at 76 Torr with V/ III=100. Surface morphologies were characterized with a scanning electron microscope (SEM). Crystalline defects were characterized with transmission electron microscopy (TEM).

3. RESULTS AND DISCUSSION

To obtain high crystalline quality InP layers in STI trenches, we studied the defect formation mechanism in terms of local growth rates, the impact of substrate miscut angle and the STI side wall tapering angle. Fig. 1 shows the SEM images of InP grown at different growth rates. With a growth rate of 15 nm/min in the trench (measured by cross-section SEM), high crystalline quality InP was obtained as indicated by the undisturbed vertical growth. In contrast, by increasing the TMIn flow to achieve 1.5 times higher growth rate while keeping the other growth parameters unchanged, we obtained drastically different surface morphology (Fig. 1b). The distorted overgrowth in Fig. 1b is caused by the high density of nano-twins as confirmed by TEM analysis. These extended planar defects originate from the STI side walls. We have consistently found in many experiments that a too high growth rate leads to enhanced twin formation in the trenches. Consequently, the layer quality is very sensitive to growth rates. It is well known that in III-V SAG the filling factor (the opening area vs. the total surface area) causes significant variation in growth rates [18,19]. Therefore, the loading effect causes a concern about layer quality dependence on local filling factors. It is a great challenge to obtain uniform layer quality on a patterned wafer with various filling factors unless ultra-high vacuum is used as in the case of chemical beam epitaxy (CBE) [20,21].

In addition to the impact of local growth rates, trench orientation on a miscut Si (0 0 1) substrate has a strong impact on layer quality. We first look at the InP surface morphology in trenches along [1 1 0] and [$\bar{1}$ 1 0], as shown in Fig. 2. With the same filling factor and trench width, the surface morphologies are strikingly different. Vertical InP overgrowth and macrosteps are observed in [1 1 0] trenches (Fig. 2a) due to the substrate miscut, which creates atomic steps perpendicular to the trenches. During growth, InP follows step flow growth mode. When step bunching occurs, the growth rate of wide terraces decreases significantly [21-23], resulting in macrosteps. We also found that the InP surface between two neighboring macrosteps has a slope of 61, the substrate miscut angle. The distance between two adjacent macrosteps is about 1 mm on average. In contrast, the [$\bar{1}$ 1 0] trenches show slightly tilted growth toward the miscut direction, [1 1 1]. No macrosteps are found in these trenches.

The different InP surface morphologies are linked to both miscut angle of the substrate and the planar defects in the layer. Fig. 3 shows cross-sectional TEM images of [1 1 0] and [$\bar{1}$ 1 0] oriented trenches. These two trenches are from the same sample. The layer thicknesses in both trenches are similar. More nano-twins are found in the [$\bar{1}$ 1 0] trenches. A series of cross-section TEM images confirmed the consistent formation of nano-twins originating from the STI side walls in the [$\bar{1}$ 1 0] trenches. Furthermore, these nano-twins occur preferentially on the same side of the trenches. Note that the Si surface is not flat in Fig. 3b, which is attributed to the miscut Si substrates. During the Si recess etch with HCl vapor, the formation of the facets follows the symmetry of the Si crystal. Asymmetric facets are formed as a result of 6l substrate miscut. Despite the difference in the etched Si surface, the Ge surface becomes flat in both trenches. Therefore, there is no impact of Si surface geometry on InP growth.

The nano-twins in the [$\bar{1}$ 1 0] trenches (Fig. 3b) come from the streric hindrance effect during the growth, as schematically shown in Fig. 4. On the miscut substrate, [0 0 1] is titled from the surface normal by $\varphi \approx 6°$, the miscut angle. The facet formation follows the symmetry with respect to [0 0 1] and thus the two angles between the facets and the STI side walls on both sides, α, β, differ by 2φ ($\beta - \alpha = 2\varphi$), introducing enhanced steric hindrance effect on the side with the smaller angle. In addition to the impact of miscut angle, the STI shape also plays a role in changing the angle between the facets and the STI side walls. We first investigated the steric hindrance in [$\bar{1}$ 1 0] trenches with STI side walls, which have an inward tapering angle, $\delta \approx 6°$. In the case of {1 1 1} facets at the STI side walls, a simple calculation gives, $\alpha_{[\bar{1} 1 0]} = 35.3° - \varphi - \delta = 23.3°$, while $\beta_{[\bar{1} 1 0]} = 35.3° - \varphi - \delta = 35.3°$, This means the steric hindrance effect on the left side is substantially enhanced. As a result, the probability of forming SFs and nano-twins increases on the left side while, and on the right side, there is less chance to form these defects. This explains the preferential occurrence and consistent orientation of nano-twins in the [$\bar{1}$ 1 0] trenches on the Si (0 0 1) substrates miscut toward (1 1 1). The formation of SFs and nano-twins from the STI side walls due to the steric hindrance effect prevents the growth of high quality InP materials in the [$\bar{1}$ 1 0] trenches because these defects will propagate to the top region of the trenches (Fig. 3b).

In the [1 1 0] oriented trenches, since the atomic steps are perpendicular to the trenches, the miscut angle induces macro-steps as shown in Fig. 2a but it does not change the angle between the facets and the STI side walls. Therefore, for a STI side wall tapering angle of 6°, $\alpha_{[1 1 0]} = \beta_{[1 1 0]} = 35.3° - 6° = 27.3°$. This angle is larger than the previous $\alpha_{[\bar{1} 1 0]} (\approx 23.3°)$ and now no nano-twins are observed at the STI side walls. However, by further increasing the STI tapering angle from 6° to 10°, we found a complete disrupted growth, see Fig. 5. With increased STI tapering angle, $\delta' \approx 10°$, we recalculate that $\alpha'_{[1 1 0]} = \beta'_{[1 1 0]} = 35.3° - 10° = 25.3°$. With this angle, both the [110] (Fig. 5a) and [$\bar{1}$ 1 0] (Fig. 5b) trenches show distorted InP crystal growth. With a decrease in angle between the {1 1 1} facets and the STI side walls, steric hindrance becomes more pronounced and thus nano-twins occur on both sides of the trenches. The high density of nano-twins interrupts the crystal growth in the [0 0 1] direction. The presence of these planar defects also ruins the step flow growth and thus no macrosteps are observed in the [1 1 0] trenches. In our case, the critical angle for nano-twin formation seems to be around 27°. Too small angles result in nano-twin formation. Furthermore, we found the distorted InP crystal growth could not be solved by lowering the growth rates.

Fig. 1. *Tilted-view SEM images of [1 1 0] oriented trenches with different InP growth rates, 15 and 22.5 nm/min for (a) and (b), respectively. The trench widths in both cases are 110 nm.*
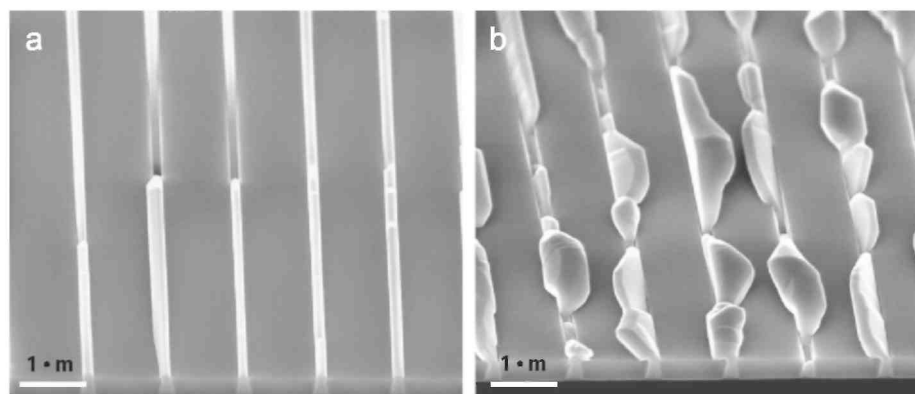
Fig. 2. *Top-view SEM images of InP surface morphology in [1 10] (a) and [̄1 1 0] (b) trenches. The InP growth rate is 15 nm/min. The trench widths are 150 nm and the STI side wall tapering angle is ~ 6°.*
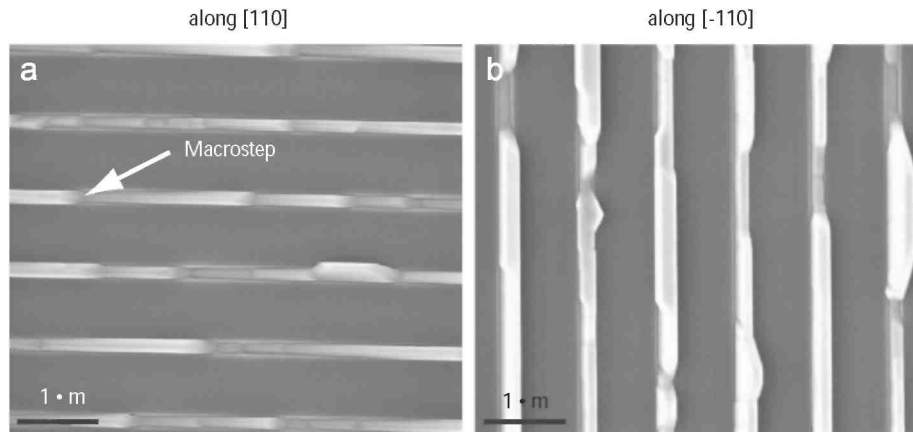
**Fig. 3**. *Bright field cross-section TEM images (g= [0 0 4]) of InP in [1 1 0] (a) and [̄1 1 0] (b) trenches. The nano-twins in [̄1 1 0] trenches are indicated by the arrow. The miscut orientation is schematically shown in (b).*
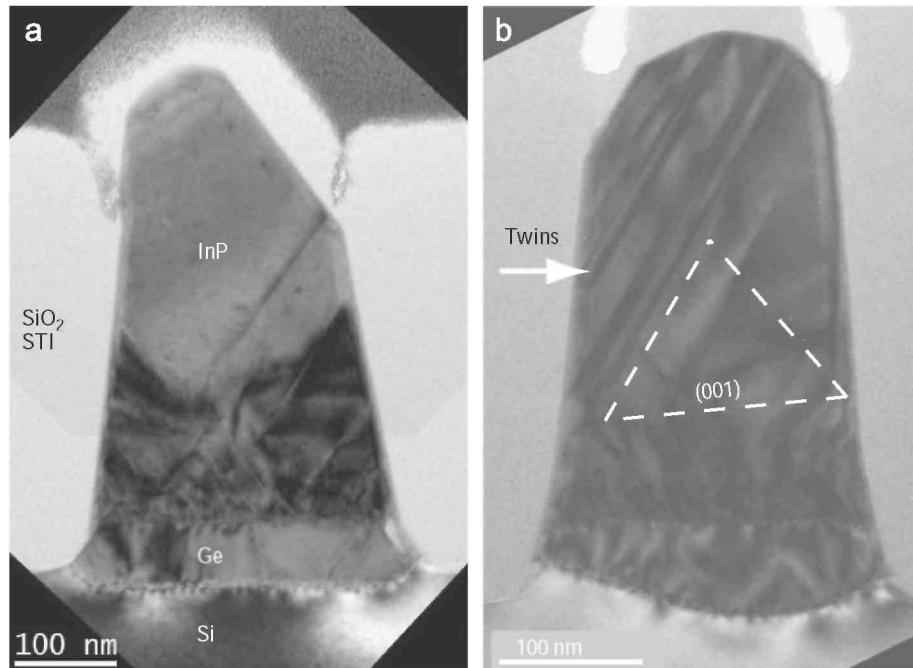

In addition to the growth-induced planar defects mentioned above, low SF energy of InP favors the dissociation of threading dislocations into SFs [24]. The 3.7% lattice mismatch between InP and Ge introduces high density of threading dislocations. Some of them dissociate into pairs of partial threading dislocations bounded by SFs [24]. The dissociation of threading dislocations into SFs is determined by thermodynamics and occurs in trenches of both orientations. The typical feature of these SFs is that they originate from the InP/Ge interface, propagate in {1 1 1} and terminate at the STI side walls. Their origin is distinctly different from the nano-twins. Therefore, these SFs can be effectively trapped at the bottom of the trenches provided that the aspect ratio is greater than 2. The cross-section TEM images of InP grown in trenches with different aspect ratios are shown in Fig. 6. All the trenches are along [1 1 0] and the STI side wall tapering angle is ~ 6°. In the absence of nano-twins originating from the STI side walls, we obtained extended defect free InP in the top 50 nm regions in trenches of 100-150 nm wide with a STI thickness of 300 nm.

Fig. 4. *Schematics of steric hindrance at the STI side walls on a miscut Si (0 0 1) substrate with {1 1 1} facet formation. The angles, α and β, are the angles between the {1 1 1} facets and the STI side walls on the left and right side, respectively. The substrate miscut angle is φ and the STI side walls have an inward tapering angle δ.*
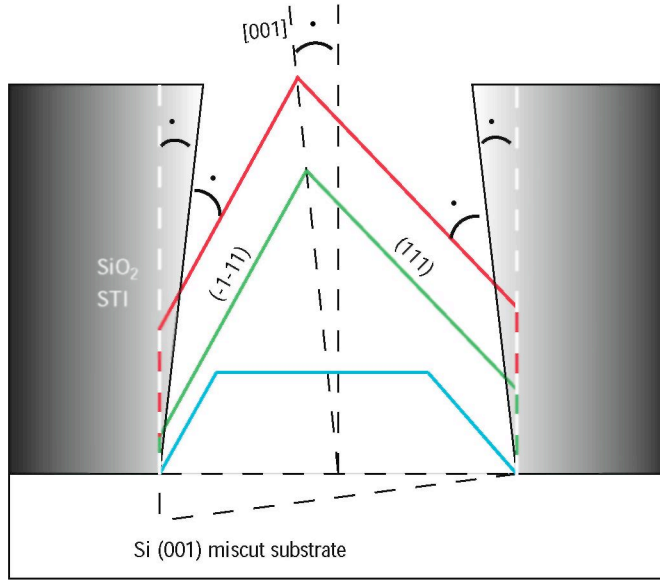

Fig. 5. *Top-view SEM images InP in both [1 1 0] (a) and [$\bar{1}$ 1 0] (b) oriented trenches with STI tapering angle of ~ 10°. At a growth rate of 15 nm/min, distorted InP growth is observed in both trenches.*
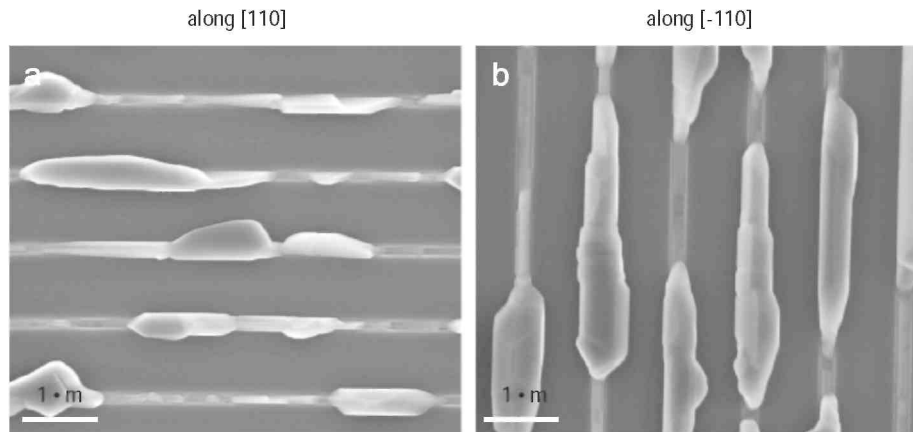
From the various TEM images shown in this paper it can be seen that the misfit dislocations at the Ge/Si interface are regularly spaced with about 10 nm separation. In the Ge layers, threading dislocations can be seen but no SFs. This is what can be expected from a fully strain-relaxed system. The threading dislocation density in these Ge layers is about 10^{10}cm^{-2} [25]. On top of the Ge layers, a 30 nm defective InP seed layer can be observed. Since this seed layer is grown at 420 °C, a high density of point defects degrades the crystalline quality. At the InP/Ge interface, the misfit dislocation separation is similar to that at the Ge/Si interface. Due to the low SF energy in InP, most of the threading dislocations propagating from the Ge/InP interface are dissociated into SFs. With the continuation of growth, SFs are left out of the layer and crystalline quality improves from the bottom to the top. In the trenches with aspect ratio greater than 2 (Fig. 6a and b), the top region of the InP layers is free of extended defects. As a result, InP growth follows the [0 0 1] direction without disturbance. The overgrown InP is bounded by {1 1 0} and {1 1 1} facets.

Fig. 6. *Bright field cross-section TEM images (g= [0 0 4]) of InP in [1 1 0] oriented trenches with different trench widths, 110nm (a), 150 nm (b) and 200 nm (c). All the STI side walls have a tapering angle of ~ 6° and the growth rate is 15 nm/min. The SFs and threading dislocations (TDs) were effectively confined in the trenches with an aspect ratio greater than 2 (a and b) where high mobility channel materials could be grown for device fabrication.*
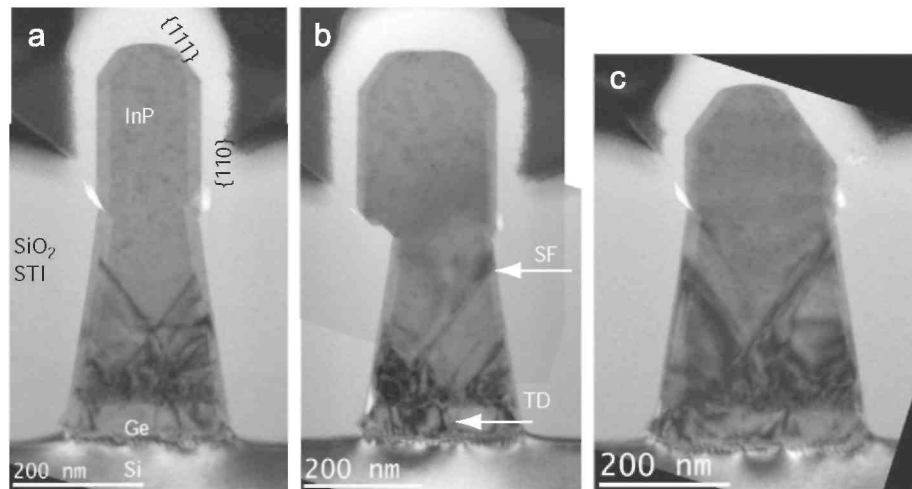
4. CONCLUSIONS

We obtained extended defect free InP in the top region of [1 1 0] STI trenches with aspect ratio greater than 2 on Si (0 0 1) substrates 6° miscut toward (1 1 1). This provides a virtual substrate for InGaAs channel based high mobility devices. We found InP layer quality is influenced by local growth rates and steric hindrance effects at the STI side walls. Too high growth rates induce a high density of nano-twins and result in distorted overgrowth.

In the [1 1 0] trenches, the miscut angle has no impact on the InP crystal defect formation. In the [1̄ 1 0] oriented trenches, the substrate miscut angle enhances the streric hindrance effects at one side of the trenches and thus increases the formation probability of planar defects. An increased STI side wall tapering angle can disrupt the crystal growth in both trench orientations. To obtain high quality InP layers in STI trenches, low growth rates and steep STI side walls are preferred.

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