ECS Transactions, 16 (8) 311-320 (2008)
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Strained Silicon on Wafer Level by Wafer Bonding: Materials Processing, Strain Measurements and Strain Relaxation

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Different methods to introduce strain in thin silicon device layers are presented. Uniaxial strain is introduced in CMOS devices by process-induced stressors allowing the local generation of tensile or compressive strain in the channel region of MOSFETs. Biaxial strain is introduced by growing thin silicon layer on SiGe buffer and transferring it to an oxidized silicon substrates. The latter forms strained silicon on insulator (SSOI) wafer characterized by tensile strain only. Future CMOS device technologies require the combination of the global strain of SSOI substrates with local stressors to increase the device performance.

Introduction

Conventional MOSFETs have proven to be remarkably scalable to gate lengths of about 60 nm, which are compatible with the 130 nm high-performance CMOS technology node. Intrinsic device performance up to this node has increased by about 17 % per year, following an inverse gate-length ($1/L_g$) dependence commensurate with channel length decrease. This performance increase has relied in part on the steady increase of channel carrier velocity due to gate-length scaling combined with innovations, such as retrograde channel doping and highly doped halos around very highly doped source and drain junctions. The intrinsic carrier transport properties in the channel material, however, have remained constant, i.e. those of the relaxed silicon lattice. From the 90 nm node onwards, additional innovations have been introduced to increase the channel carrier mobility, and hence allow continuation of velocity increase, by the imposition of strain in the silicon channel of otherwise conventional MOSFETs.

There are generally 2 different methods to introduce strain in the channel region: biaxial strain and uniaxial strain. Biaxial strain is also referred to as global strain and is introduced by epitaxial growth of Si and SiGe layers (substrate engineering). The strain is induced by the lattice mismatch between Si and SiGe. The advantages of SOI and biaxially strained silicon layers can be combined in a single substrate of strained silicon on insulator (SSOI). Its application is not limited by further scaling below 32 nm. On the

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other hand, uniaxial strain is generated by local structural elements near the channel region. Since these process modules that cause uniaxial strain are part of CMOS processes, uniaxial strain is also referred to as process-induced strain (PIS). Owing to the relative ease of integrating process-induced strain modules in conventional CMOS processes, strain enhanced scaling has relied on the development of new advanced methods of PIS. The application of local strain elements, however, is limited by further scaling to 32 nm and below making some of them ineffective or unfeasible. For instance, stressed nitride layers can furthermore not be applied by shortages of space (1, 2). Therefore new methods of strain generation in the transistor channel region are required. One possible option is the combination of global and local strain or, in other words, of biaxial and uniaxial strain.

Methods of Strain Generation

Local Strain (Process-Induced Strain)

Electron and hole mobilities respond to mechanical stresses in different ways. For MOSFETs with the [110] channel orientation on {001}-oriented silicon substrates, tensile strain along the [110] direction improves electron mobility but degrades hole mobility. Therefore, to improve both the electron mobility in n-channel MOSFETs (NMOS) and the hole mobility in p-channel MOSFETs (PMOS), the introduction of strain in the transistor channel needs to employ different approaches for NMOS and PMOS.

Advanced CMOS processes contain different process-induced stressors. These are mainly overlayers, embedded stressors, and stress memorization techniques (Fig. 1). Overlayers are typically stressed nitride layers deposited after salicidation of the source/drain and gate. Tensile overlayers are deposited over NMOS and compressive

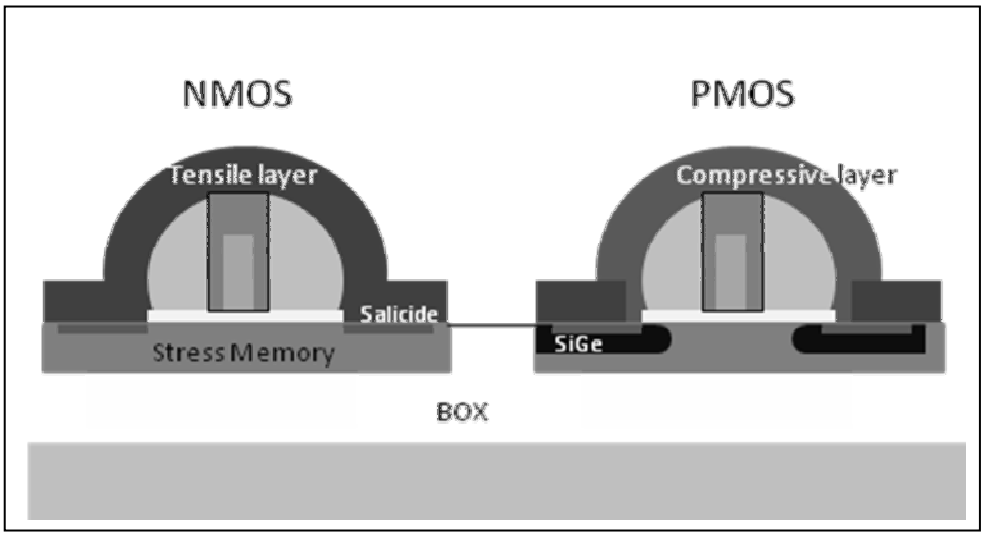


Figure 1: Schematic representation of local stressors (process-induced stressors) in SOI CMOS. Tensile strain in NMOS is obtained by tensile overlayers and various stress memorization techniques. Compressive strain in PMOS is induced by compressive overlayers and embedded SiGe.

overlayers are deposited for PMOS. The strain in the channel region depends on the intrinsic stress of the layer, thickness of the layer, and device dimensions. Using tensile and compressive layers (dual stress liner, DSL) a significant hole mobility enhancement of 60% was achieved (3). Furthermore, important parameters of SOI CMOS devices, such as effective drive current enhancement, were proved in different 45 nm technologies. Stress memorization techniques (SMT) typically involve a nitride capping layer and an additional annealing step. They increase NMOS drive current and degrade the PMOS transistor.

Embedded SiGe layers (eSiGe) are widely used in PMOS transistors. Caused by the larger lattice constant of SiGe, compressive strain is induced in the channel. Currently this technique is improved by combining SiGe and SiC layers and mixtures of both (4, 5).

The integration of the different stressors into advanced CMOS technologies results in increasing device performance required by the ITRI road map (6). Typical effects of local stressors on the carrier mobility and the drive current (saturation drive current I_{DSAT} and linear drive current I_{DLIN}) are summarized in table 1 for a SOI CMOS process (7). Similar results of performance improvements have been also reported for CMOS processes on conventional bulk substrates (8, 9).

Table 1: Mobility, I_{DSAT}, and I_{DLIN} improvements for different stressor techniques. Measurements on transistors prepared at the 65 nm technology node of a SOI CMOS process (7).

NMOS	Electron Mobility	I_{DSAT}	I_{DLIN}
SMT	35%	10%	11%
Tensile Liner	27%	11%	2%
PMOS	Hole Mobility	IDSAT	IDLIN
eSiGe	70%	23%	56%
Compressive Liner	90%	19%	39%

Global Strain

Global strain on wafer level is mostly induced by the epitaxial growth of Si_{1-x} Ge_x and Si layers. Because the lattice parameter of Si_{1-x} Ge_x ($0 \leq x \leq 1$) alloys varies between 0.5431 nm for silicon ($x = 0$) and 0.5657 nm for germanium ($x = 1$) tensile strain is induced in a silicon layer epitaxially grown on top of the SiGe. The strain is generally biaxial. Furthermore, uniaxial strained layers are also obtained by mechanical straining.

Biaxially strained layers. Figure 2 illustrates various heterostructure substrates that have been applied to biaxial strain and high-mobility channel materials. Epitaxially grown Si_{1-x} Ge_x layers on Si bulk wafers are generally applied acting as substrate for a strained silicon layer grown on top (bulk materials). In order to reduce the defect density in the strained silicon a relaxed Si_{1-x} Ge_x buffer is required grown on a graded Si_{1-x} Ge_x layer (Fig. 2a). Because the Ge concentration x increases continuously by about 10 % per µm, the thickness of the graded buffer is several micrometers (Fig. 3a) (10, 11). An alternative is the relaxation of a thin pseudomorphic SiGe layer (< 500nm) induced by

hydrogen or helium implantation and subsequent annealing (Fig. 2d, 3b) (12, 13). Thinner SiGe buffer makes the process costs effective. Variations of the basic structure (Fig. 2a) have been also published including dual channel structures incorporating an additional strained Si_{1-y} Ge_y layer with y > x (Fig. 2b) and heterostructures on bulk using a second strained silicon layer (Fig. 2c) (9). Layer stacks of the types a, c, and d have been applied as virtual substrates for the preparation of SSOI and SGOI wafers. The

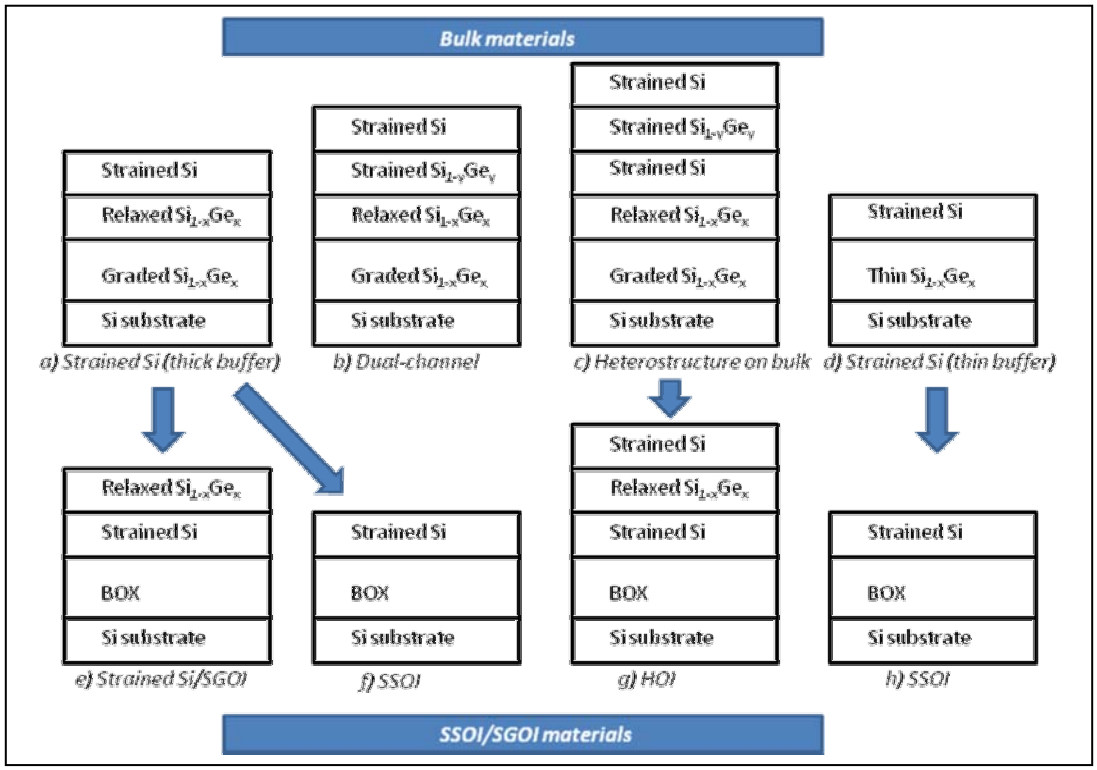
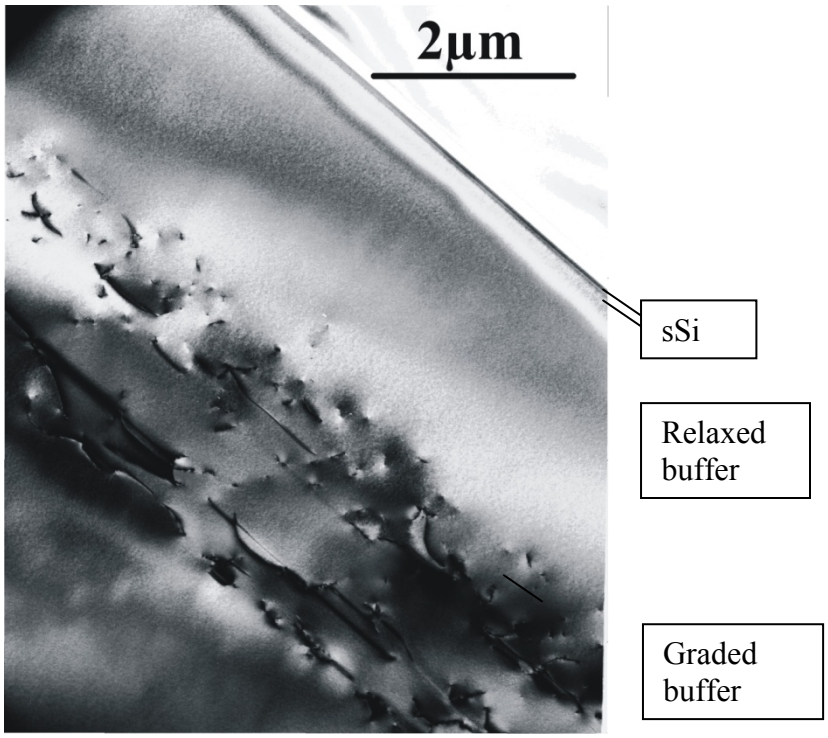


Figure 2: Schematic illustration of various heterostructure substrates produced by epitaxial growth on bulk substrates (bulk materials) and by transfer of the strained layers to oxidized substrates (strained silicon on insulator (SSOI), strained Si/SiGe on insulator (SGOI)) (9, 17).

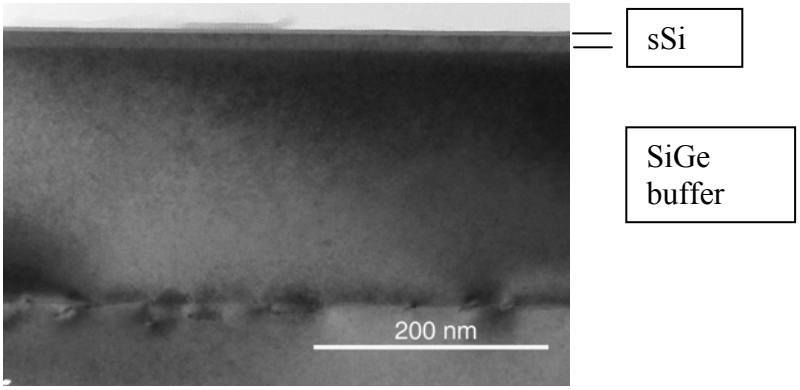
realization of SSOI wafers from bulk materials is a complex process combining wafer bonding, layer transfer, and etch-back methods. Processes using thick SiGe buffer layers were described, for instance, in references (14 – 16), while a process using thin buffer layers was published in ref. (17). The SSOI technologies provide a pathway to implementing mobility enhancement in partially or fully depleted devices, in ultrathin-body MOSFETs, or nonplanar (double-gate) MOSFETs. Mobility enhancement in SSOI was reported in (9) and (17) for the different SSOI configurations. Furthermore, long channel devices ($L_g \geq 1\mu m$) show clearly improvements of the device characteristics. For instance, drive current (I_{DSAT}) improvements of 80% at the same source-to-drain leakage (I_{OFF}) has been measured. Improvements in the same order of magnitude were not obtained for short channel devices. Here, an I_{DAST} improvement of only 10 – 20% was obtained up to now (17). The main reason was the interaction with process-induced stressors reducing the effect of the biaxial strain (18). This means that applications of SSOI wafers require modifications of existing CMOS processes. The combination of biaxially strained SSOI and optimized uniaxial stressors (dual-stress nitride capping layer and embedded SiGe) was already demonstrated resulting in I_{DSAT} improvements of 27%

and 36% for n-channel MOSFETs and p-channel MOSFETs, respectively, in sub- 40 nm devices (19). In addition, the gate leakage current was also reduced by 30%. All investigations suggest that the combination of biaxially strained SSOI and uniaxial strain by process-induced stressors is the optimum way for future requirements (2, 9, 18, 19).

Uniaxial strained layers: A concept to realize uniaxial strain on wafer level was published in ref. (20). Two wafers were bent over a cylinder thereby creating a curved or bowed wafer with a strained state induced. The bending direction was parallel to [110]. The curved wafers are brought into contact via direct wafer bonding and covalent bonds



a)



b)

Figure 3: Typical XTEM images of the strained Si/SiGe bulk heterostructures used as virtual substrates for SSOI fabrication.

a) a relaxed $Si_{0.83}Ge_{0.17}$ layer (about 2 µm thick) is grown on top of a compositional graded layer corresponding to the schema in Fig. 2a;
b) strained silicon layer on top of a pseudomorphically grown $Si_{0.77}Ge_{0.23}$ layer after relaxation by He implantation and subsequent annealing (corresponding to schema in Fig. 2d).

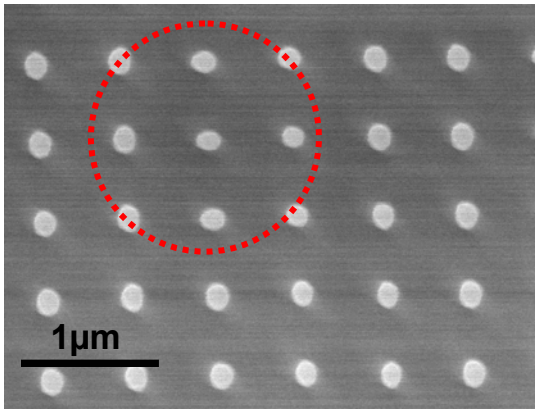
across the bonded interface form upon annealing in the bent state. By combining the process with hydrogen-induced layer splitting thin strained layers were transferred. The process can generally be used to realize strained layers of either tensile or compressive strain. The strain introduced by this technique is significantly lower as for biaxially strained layers. Depending on the radius of curvature strain values between about 0.08% and 0.04% were obtained for a radius of curvature ranging from 0,5 m up to 1 m.

Characterization of Strain

There is a large number of methods to measure the strain in thin layers but only a few are applied to strained silicon. For characterization of strain in non-patterned layers X-ray diffraction methods and UV- Raman spectroscopy are generally used. Especially UV-Raman spectroscopy is the method of choice because it is a non-destructive method, easy to handle, allows fast measurements, and can be applied in CMOS process lines. Because the penetration depth of the laser light mostly used for excitation (λ = 325nm) is about 10 nm in silicon, UV Raman spectroscopy is applicable also for very thin strained silicon layers required for fully depleted device fabrication. The application of the conventional UV-Raman technique, however, is limited to patterned device layers. For instance, Fig. 4a shows the SEM image of a patterned strained silicon layer on top of a SiGe buffer. Round strained silicon pillars having a diameter of 100nm were realized by electron beam lithography and dry etching. Using a μ-Raman setup and a He-Cd laser with λ = 325 nm, the diameter of the laser beam on the sample is about 1.5 μm. Since the dimension of the laser spot is larger than of the patterned pillars, a single Raman measurement contains contributions of more than one pillar and from the underlying SiGe buffer. The different positions of the Si-Si vibration modes in the strained silicon and SiGe allow the integral measurement only of a few pillars. The results show that patterning causes a distinct strain relaxation that is significantly increasing if the pillar diameter is reduced from 500 nm down to 100 nm (Fig. 4b). Numerical simulations of the strain relaxation are in agreement with the measured data. In addition, finite element simulation of the strain distribution in individual pillars were also carried out proving that the strain relaxes rather close to the free surfaces while remains concentrated at the interface between the strained silicon and the underlying SiGe buffer (21).

Analogous measurements on patterned strained silicon layers on an oxide (as for SSOI) cause that the strong Si-Si vibration mode of the silicon base wafer appears and the Si-Si vibration mode of the thin strained silicon structures cannot clearly be identified anymore. One possible solution to measure structures as shown in Figs. 4e, f is the reduction of the wavelength of the exciting laser. First measurements using a laser excitation at λ = 244 nm (frequency-doubled Ar ion laser) indicate that patterns having dimensions of 80 nm x 120 nm can be analyzed (22). The laser spot on the sample surface is about 500 nm and, using distances between individual structures in the same range, the measurement of single structures is possible.

Alternative techniques applicable to structures in strained silicon having feature sizes below 100 nm could be tip-enhanced (TERS) or surface-enhanced (SERS) Raman spectroscopy. Only first results exist up to now to their applicability for strained silicon on a SiGe buffer layer (23) and on SSOI (24). Besides Raman spectroscopy, also electron microscope methods were used either by analyzing the high-order Laue zone (HOLZ)



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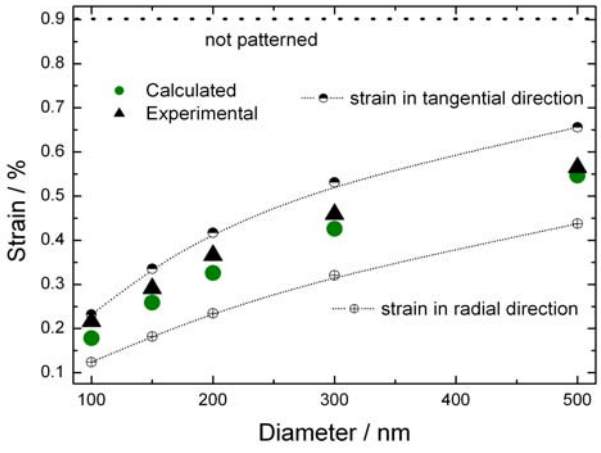

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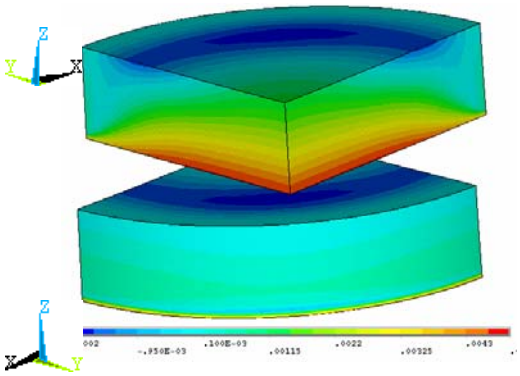

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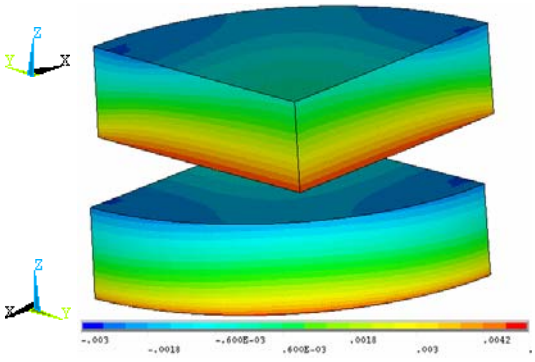

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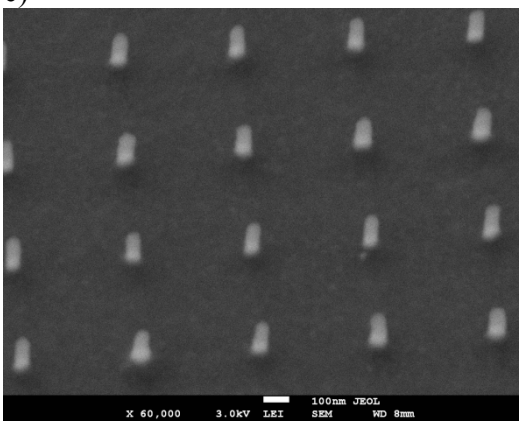

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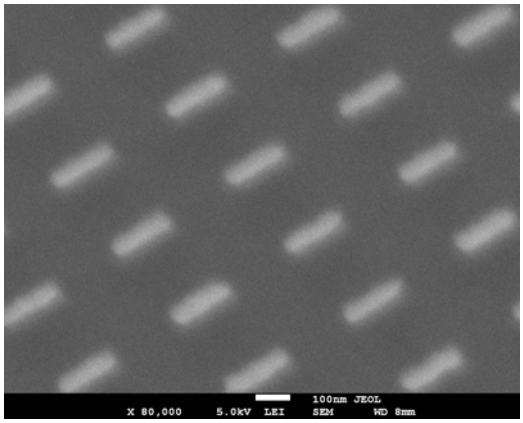

f)

Figure 4: SEM images of patterned round strained silicon pillars on a SiGe buffer (a). The dotted circle indicates the laser spot size. Comparison of strain values measured by µ-Raman spectroscopy (triangles) and calculated by finite element modeling for pillars having diameters ranging from 100 nm to 500 nm (b). Strain distribution obtained by finite element calculations within a round strained Si pillar with a diameter of 100 nm on the radial (c) and tangential (d) polar coordinates (21). SEM images of rectangular structures produced in a 20 nm thick strained silicon layer of a SSOI wafer. The dimensions of the structures are 50 nm x 100 nm (e) and 80 nm x 120 nm (f).

lines using convergent-beam electron diffraction (25) or nanoscale holographic interferometry (26). Both techniques are destructive and applied up to now only to devices.

Conclusions

Wafer bonding and layer transfer in combination with hydrogen-induced layer splitting is an effective approach to realize SSOI substrates using different virtual substrates. The strain in the silicon layer is tensile. The combination of the global strain of SSOI with local (process-induced) stressors is most important to improve important parameters of n-channel and p-channel MOSFETs simultaneously in future high-performance device technologies. The scalability of some of the process-induced stressors, on the one hand, is limited. This requires new techniques for stress generation on device level. On the other hand, band structure modeling proved that strong confinement cancels out some of the band splitting and effective mass reduction offered by biaxial tensile strain in ultrathin SOI (26). Consequently, higher levels of strain are required in order to get a band splitting similar to that observed in bulk strained silicon.

Acknowledgments

We are thankful to S. Hopfe and R. Scholz for the sample preparation and XTEM investigation. This work was financially supported by the German Federal Ministry of Education and Research in the framework of the TeSiN project (contract no. V03110).

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