Operating the power electronics of a superconducting system at low temperatures: mitigation of interface trap effects in a p-type MOS capacitor

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Keywords—p-Type MOS Capacitor, Cryogenic Temperatures, Interface Traps, Hysteresis, Bump Effect, Flat-Band Voltage, Memory Effect

Operating a transportation superconducting system with its power electronics at cryogenic temperatures is promising for increasing its efficiency, mainly by reducing the electronics power losses and increasing their power density. MOSFETs can show improved homogenized behavior such as higher switching speed and lower on-resistance when operated at cryogenic temperatures rather than at room temperature. In this study, we designed and fabricated our own MOS capacitor, with a full control of its architecture in order to understand its behavior at cryogenic temperatures. The MOS electrical and thermal homogenized behavior were characterized by means of a conventional C-V analysis. The MOS capacitors were fabricated by radio-frequency magnetron sputtering of a SiO2 target on (100) p-type silicon substrates at room temperature. Gate contacts were processed via the deposition of Al layers and electrical characterization was carried out using an impedance meter within a range of 293 K to 40 K. In comparison to the capacitance response at room temperature, a “bump” is observed in the C-V curve as temperature becomes sufficiently low (see Fig. 1). This response is a well known feature [1] and it is thought to be associated with charge trapping at interface states as the dynamics of the emission processes gets slower at reduced temperatures. As a result, the C-V curve is stretched out over the bias range required to fully interact with the trap states. The study also identified a strong electrical hysteresis influenced by prior thermal and electrical conditions, accompanied by capacitance dispersion. Such behaviors could impair the performance of these components as fundamental characteristics like threshold voltage and on-resistance can be impacted [2]. We show that applying a bias voltage during the cooling phase leads to an improved control over the flat-band and threshold voltages (see Fig. 2), thereby presenting a viable approach to mitigate the bump phenomenon and optimize device performance.

Ref:

[1] Goetzberger, A., & Irvin, J. C. (1968). Low-temperature hysteresis effects in metal-oxide-silicon capacitors caused by surface-state trapping. *IEEE Transactions on Electron Devices*, *15*(12), 1009-1014.

[2] Gui, H., Chen, R., Niu, J., Zhang, Z., Tolbert, L. M., Wang, F. F., ... & Choi, B. B. (2019). Review of power electronics components at cryogenic temperatures. *IEEE transactions on power electronics*, *35*(5), 5144-5156

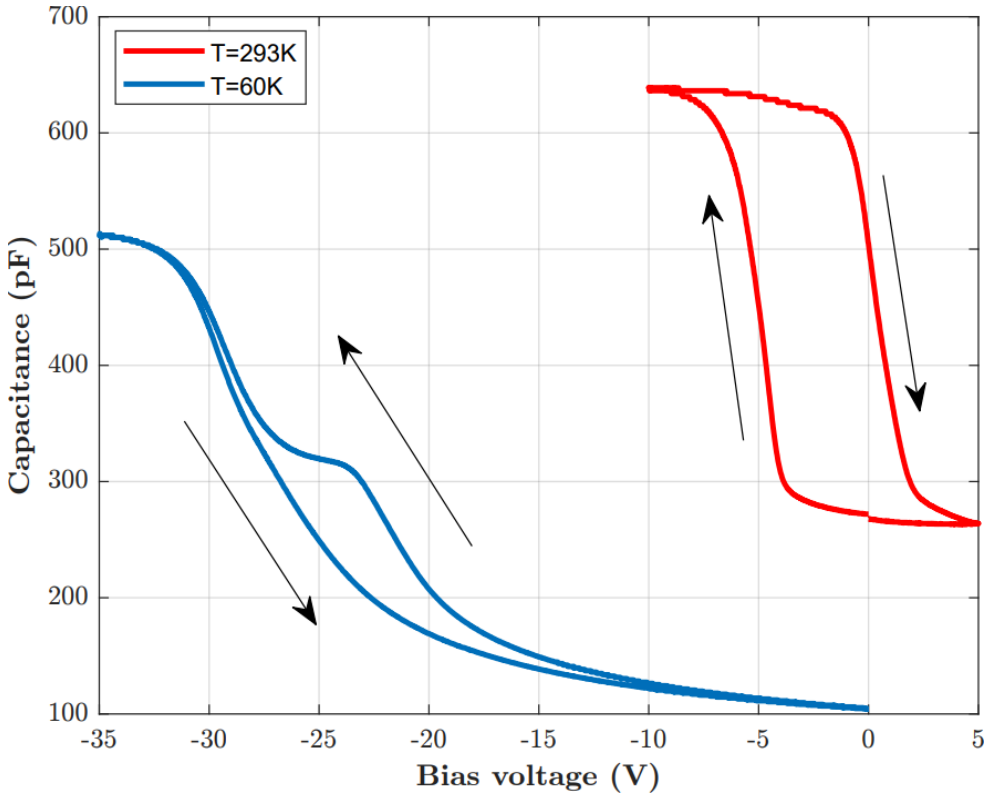

Figure 1 - Temperature influence on measured C-V curves at 100 kHz

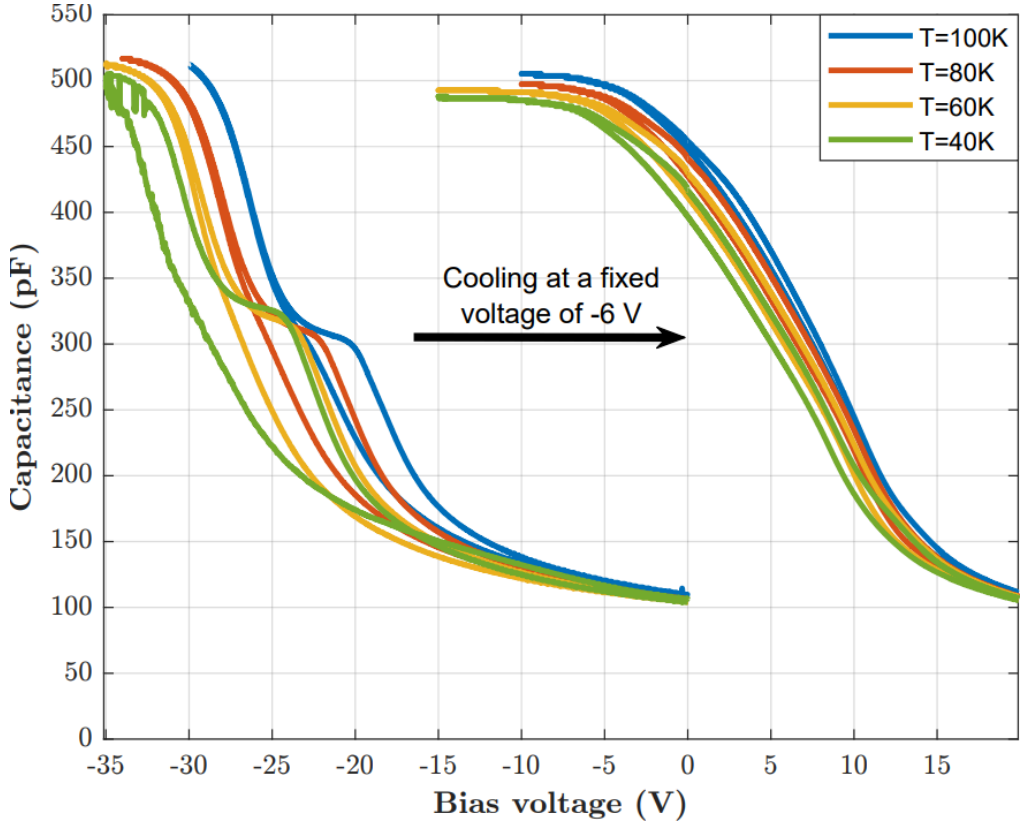

Figure 2 - C-V curves Before and after cooling at a fixed voltage