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Operating the power electronics of a superconducting system at low temperatures: mitigation of interface trap effects in a p-type MOS capacitor

Francisco Eleuterio^{1,2}, Benoît Vanderheyden¹, Stéphane Rael², Nguyen Ngoc Duy¹, Jean Leveque²

¹University of Liège, Belgium

²GREEN, BP 70239, 54506 Vandœuvre-lès-Nancy, France



Introduction: electronics for power applications in cryogenic environments

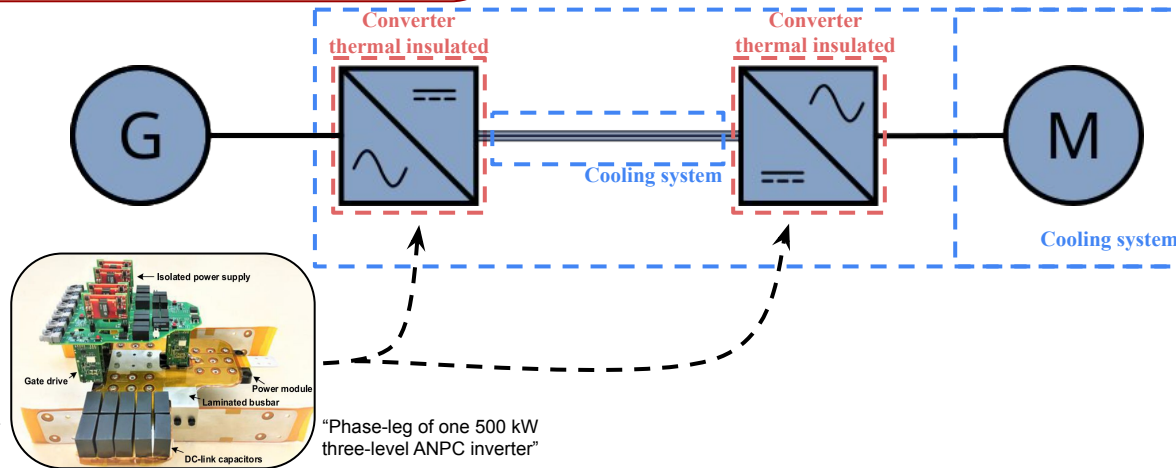
➤ Growing interest in **superconducting systems**

- Electrical machines
- Aerospace sector
- Fusion
- High-field magnets

➤ Need for **electronic control**

➤ Can we **cool down** the control electronics to gain in **efficiency**?

- Can contribute to lower power dissipation
 - Smaller volume and weight
- ## ➤ Challenge for application
- Important to understand the physical properties of power devices



[R. Chen, F. Wang. in *IEEE Open Journal of Power Electronics*, vol. 2, pp. 315-326, 2021.]

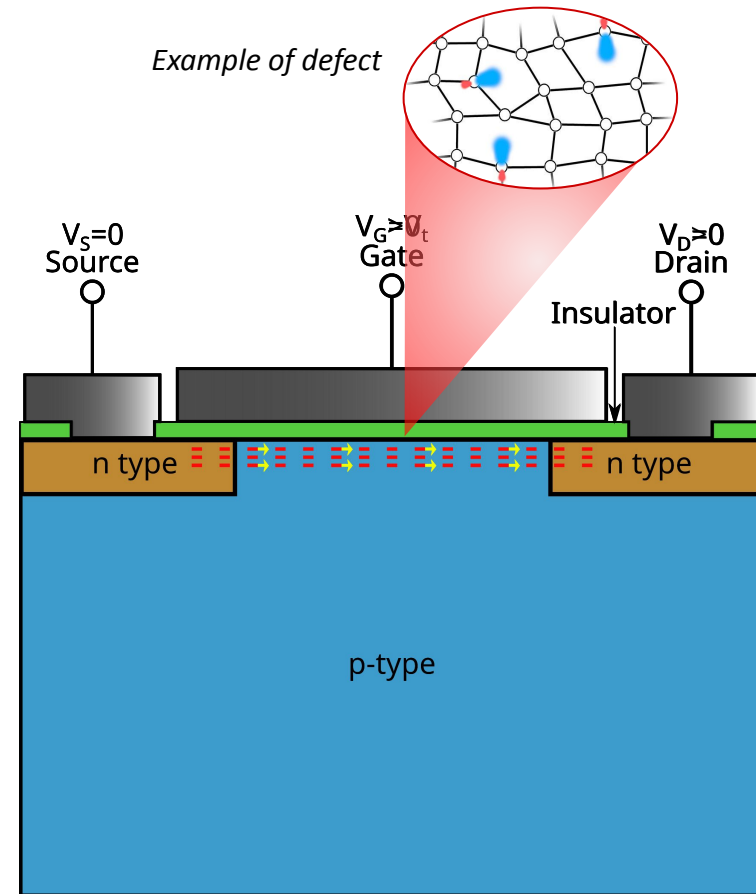


[Dorget, R., et al. in *IEEE Transactions on Applied Superconductivity*, vol. 35, no. 5, 2025.]

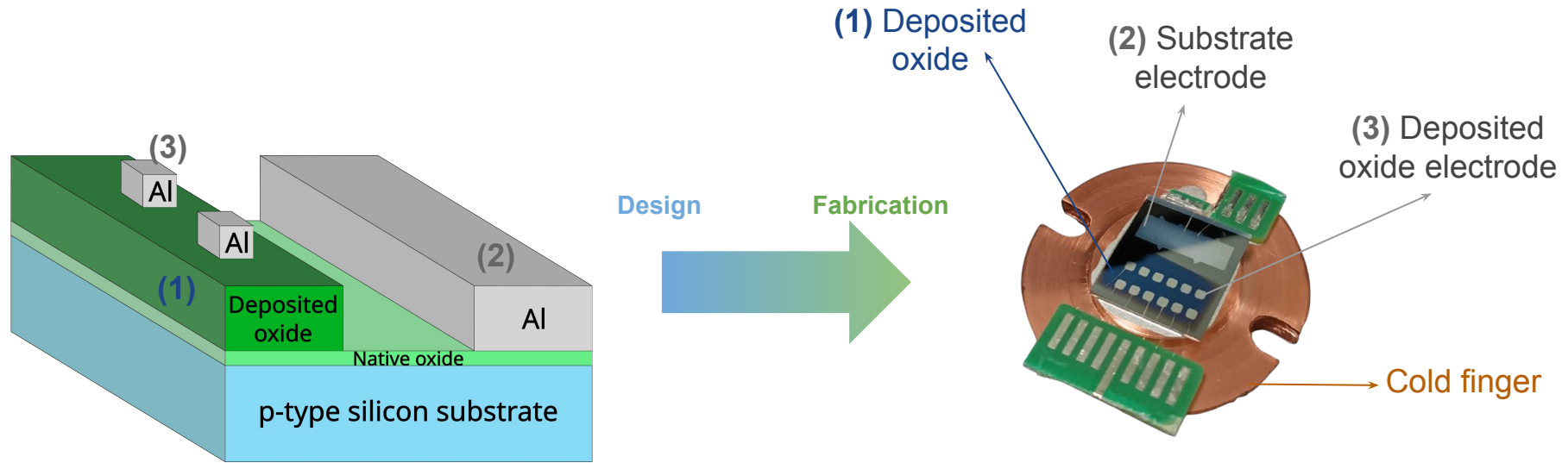
Fundamental concepts of MOSFET

- $V_G = 0$
Low conductivity between Source and Drain
- $V_G > V_t$
Formation of conductive channel between Source and Drain
 - Related to the electrostatics of the MOS stack
 - Impacted by defects in the MOS stack

p type = holes as majority charge carriers
n type = electrons as majority charge carriers



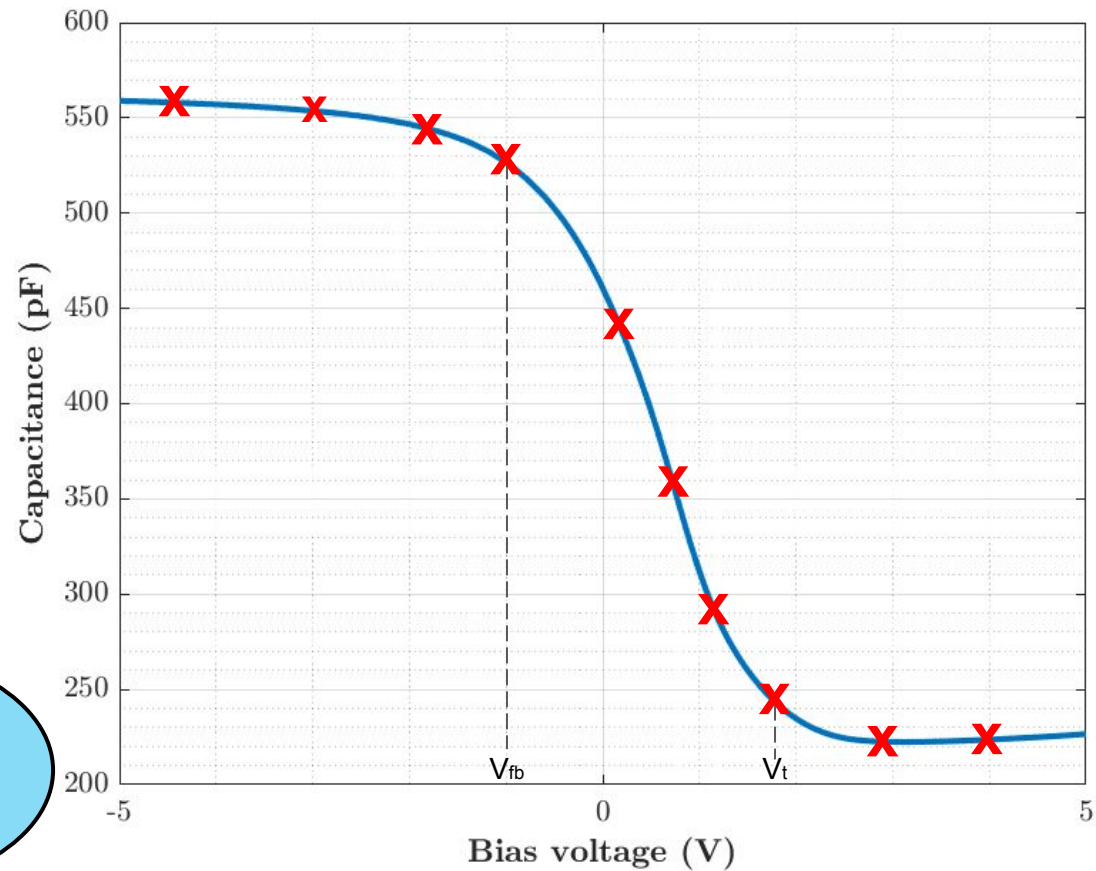
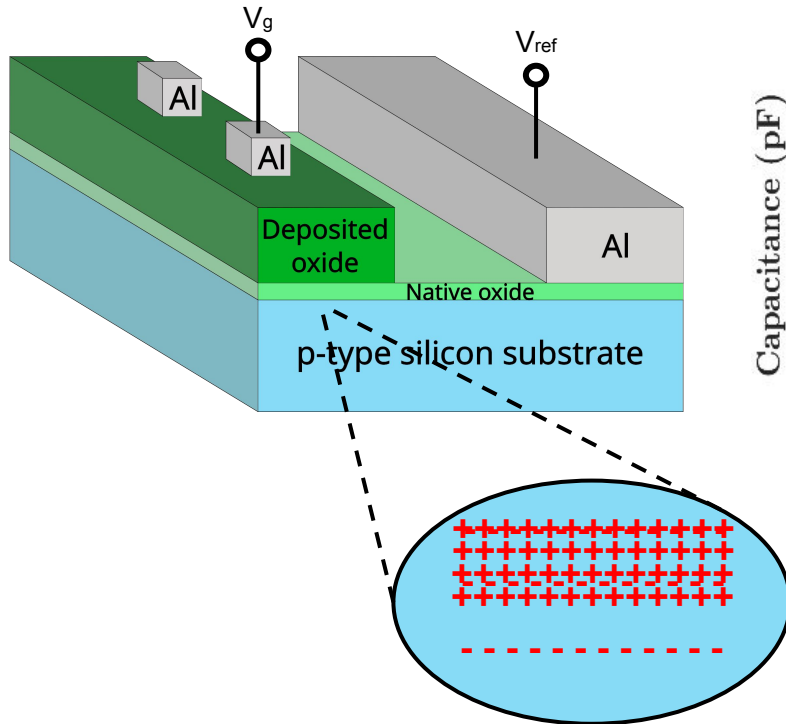
Fabricated MOS capacitor for experimental studies



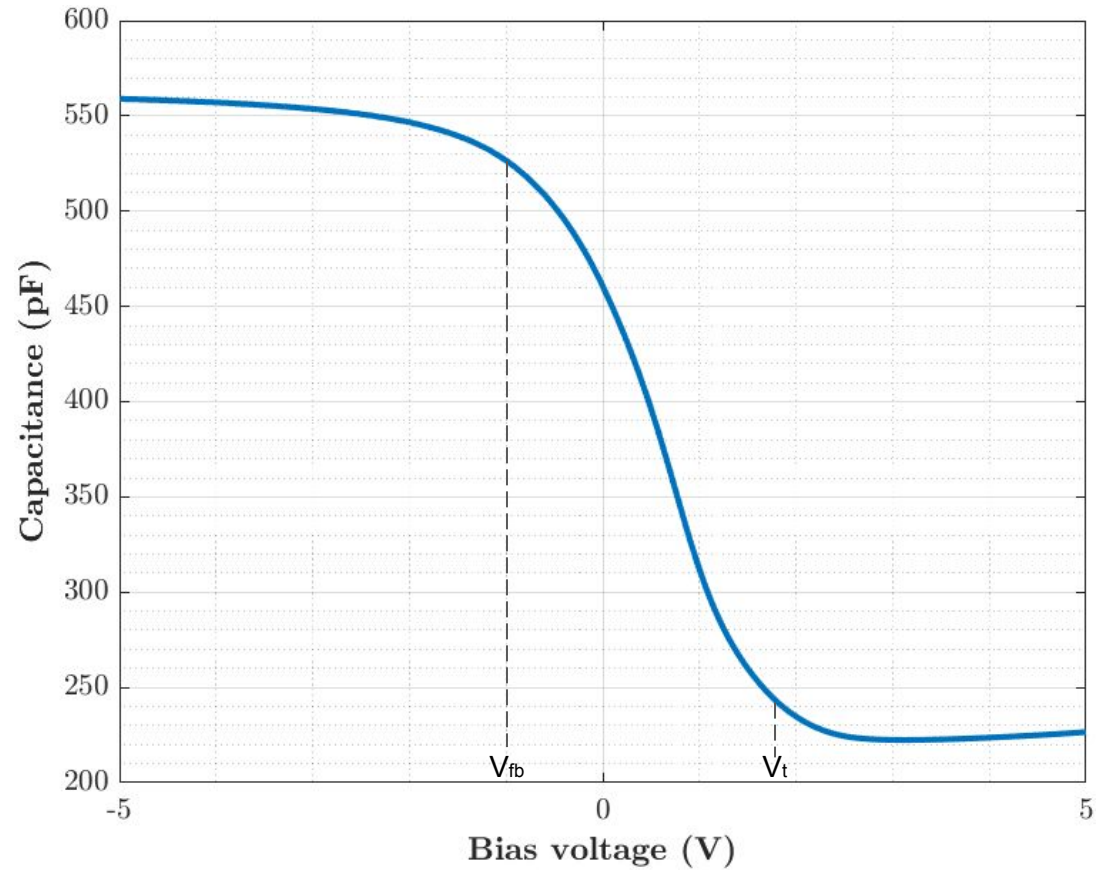
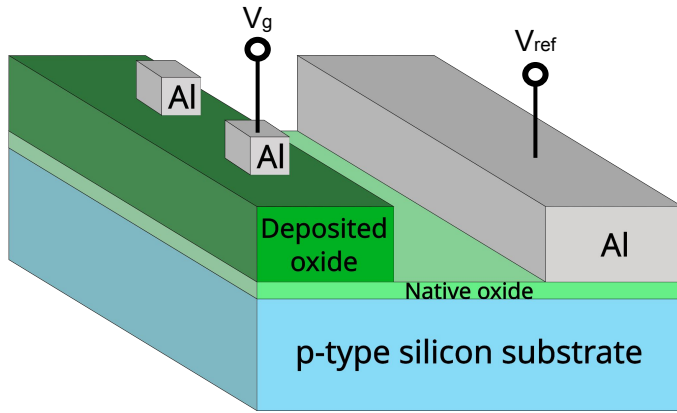
**RF sputtered SiO₂ MOS capacitor structure
designed on purpose with physical characteristics:**

- Thickness (100 nm)
- Roughness (RMS = 0,2 nm)
- Stoichiometry (SiO_x)

Characteristic C-V curves



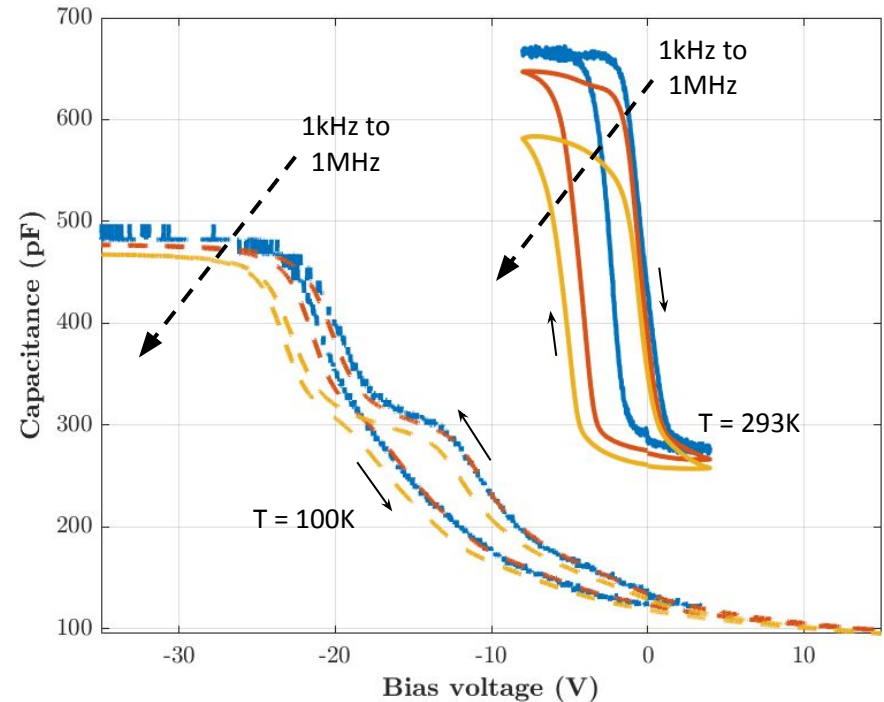
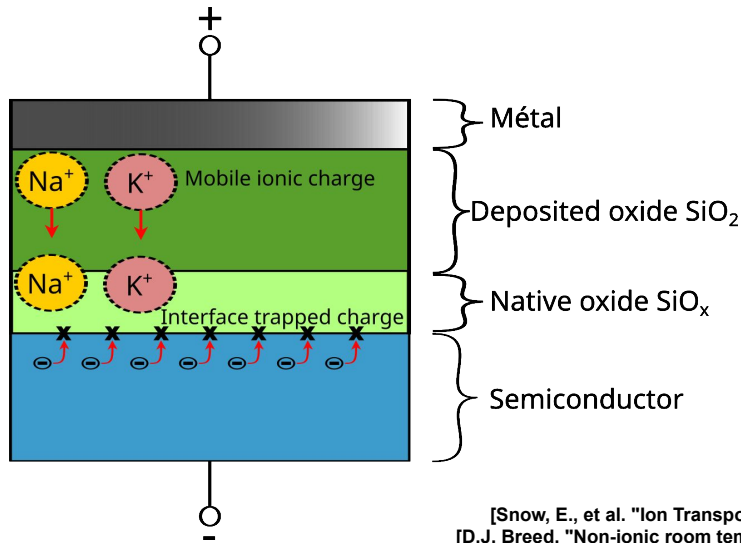
▶ Characteristic C-V curves



Results: C-V characteristics at room temperature and at 100K

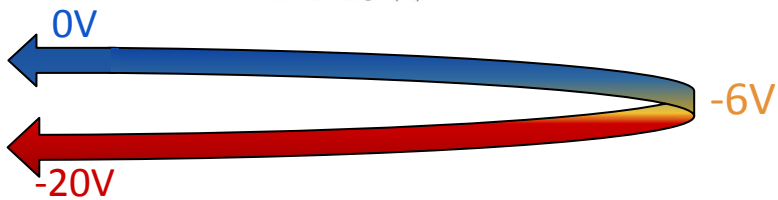
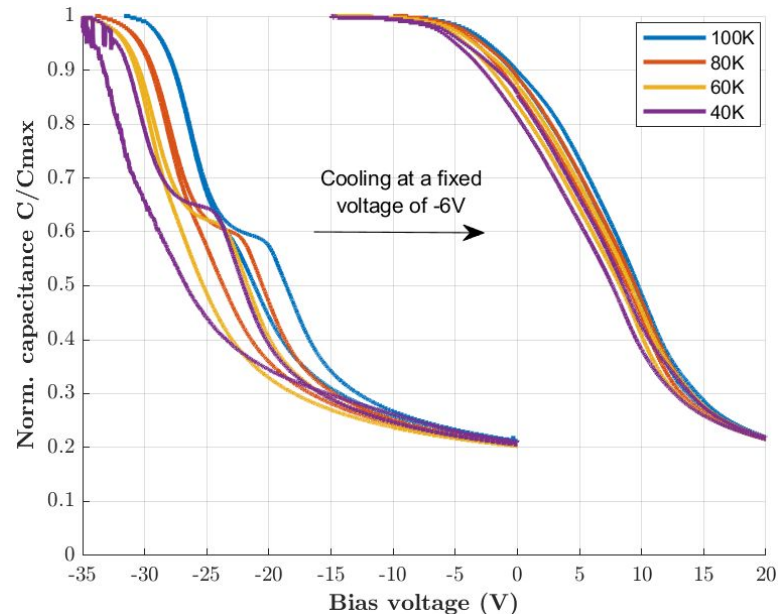
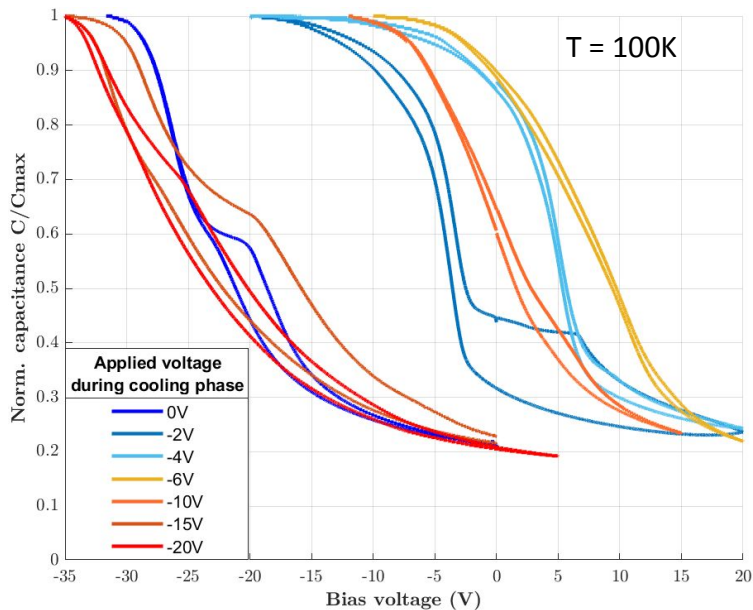
Trap-induced effects

- Hysteresis in Voltage Sweep
- C(f) dispersion
- Cryogenic behavior
 - C-V stretch-out effect
 - Bump effect

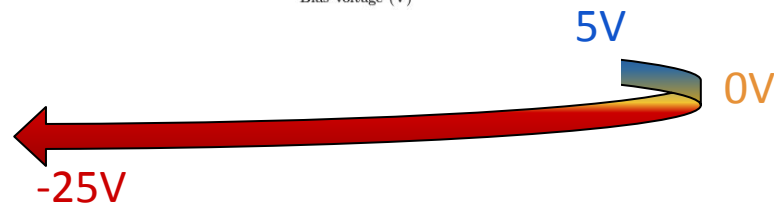
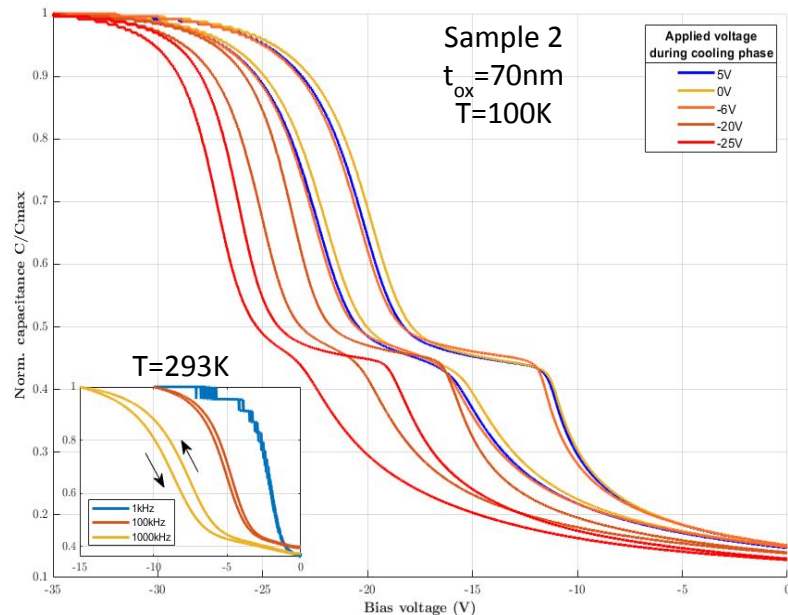
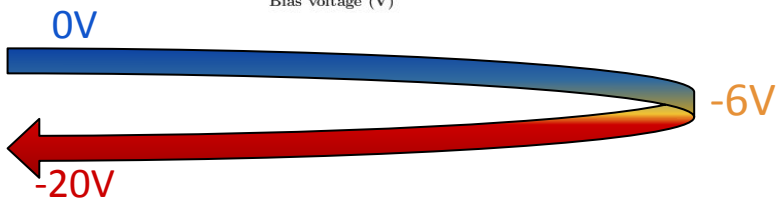
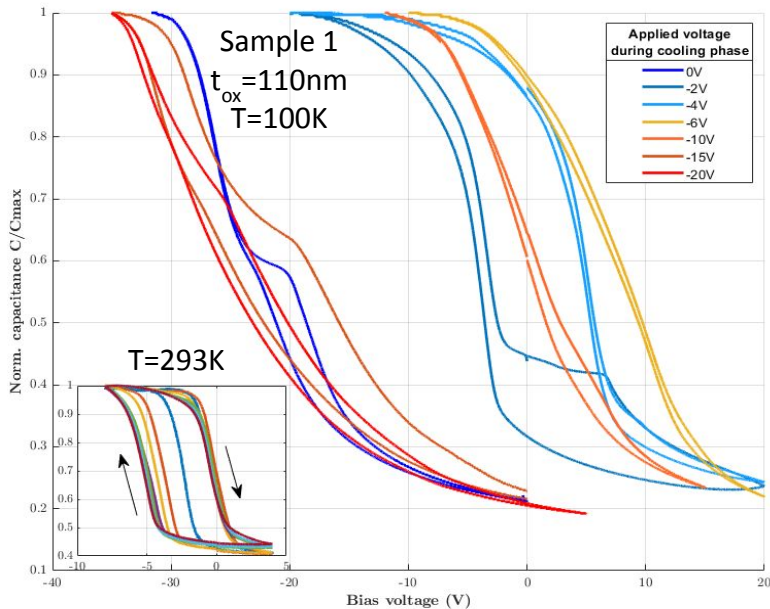


[Snow, E., et al. "Ion Transport Phenomena in Insulating Films," in *Journal of Applied Physics*, vol. 36, no. 5, pp. 1664-1673, 1965.]
[D.J. Breed. "Non-ionic room temperature instabilities in MOS devices," in *Solid-State Electronics*, vol. 17, no. 12, pp. 1229-1243, 1974.]

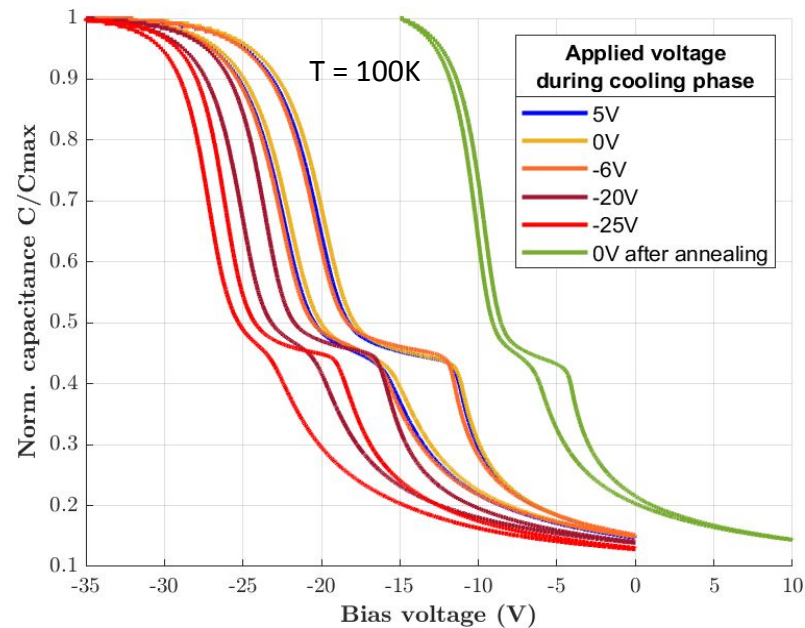
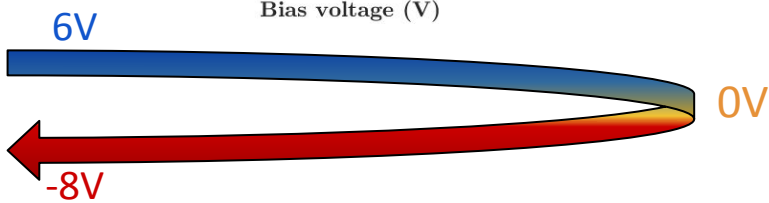
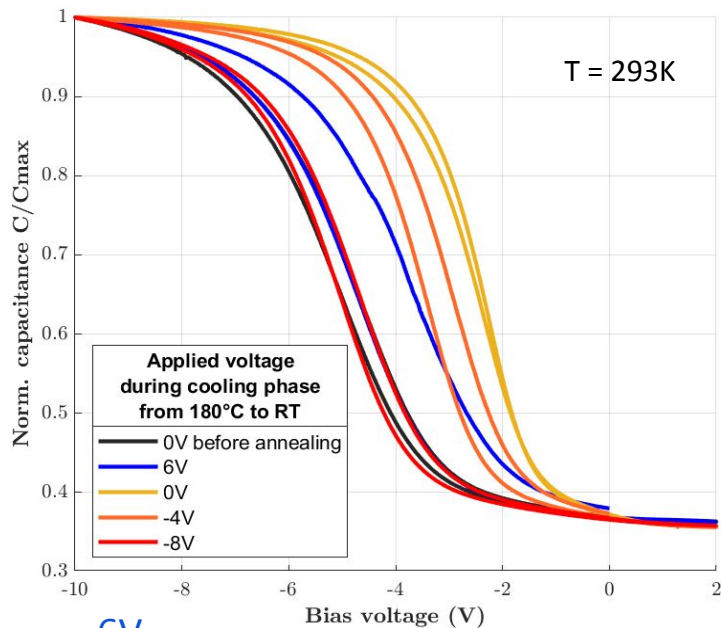
Results: impact of bias voltage while cooling the sample



Results: cryogenic behavior under the influence of low mobile ionic charge



Results: Sample 2, annealing treatment



▶ Conclusion

➤ To keep in mind

- Defects in MOS capacitors can greatly affect device performance, **especially at low temperatures!**
- Applying a voltage bias to the MOS during the cooling phase can help improve the device response

➤ Perspectives

- Annealing MOS devices before cooling
- Extended physical-chemical characterisation of the MOS stack

Thank you for your attention!

Francisco Eleuterio de Loredo
francisco.eleuterio-de-loredo@univ-lorraine.fr | PhD student at GREEN and ULiege



$$R_{en} = e_n N_t f_F(E_t) \quad (1)$$

$$R_{cn} = C_n N_t (1 - f_F(E_t)) n \quad (2)$$

R_{en} - Emission rate (#/cm3-s)

R_{cn} - Capture rate (#/cm3-s)

C_n - Constant proportional to electron-capture cross section

N_t - Total concentration of trapping centers

n - Electron concentration in the conduction band

$f_F(E_t)$ - Fermi function at the trap energy

e_n - Constant or **Emission Coefficient**: The probability per unit time that a trapped electron is thermally emitted

Thermal equilibrium:

$$R_{en} = R_{cn} \quad (3)$$

Using Boltzmann approximation $E_t - E_F \gg kT$ and consequently $f_F(E) \approx \exp\left(\frac{-(E-E_F)}{kT}\right)$:

$$e_n = n_0 C_n \quad (4)$$

E_F - Fermi level

n_0 - Electron concentration in the conduction band at thermal equilibrium

Where :

$$n_0 = N_c \exp\left(\frac{-(E_c - E_F)}{kT}\right) \quad (5)$$

Finally, emission time constant is the characteristic **time it takes for a single carrier to be emitted once it is trapped**, considering $1 - f_F(E_t) \approx 1$ from Boltzmann approximation:

$$\tau_{e,n} = \frac{1}{e_n} = (C_n N_t)^{-1} \exp\left(\frac{(E_c - E_t)}{kT}\right) \quad (6)$$

$$\tau_{e,n} = \frac{1}{e_n} = (\sigma_n \bar{v} N_c)^{-1} \exp\left(\frac{(E_c - E_t)}{kT}\right) \quad (7)$$

σ_n - Electron capture cross section

\bar{v} - Thermal velocity

$$R_{eh} = c_h N_t (1 - f_F(E_t)) \quad (1)$$

$$R_{ch} = C_p N_t f_F(E_t) p \quad (2)$$

R_{eh} - Emission rate (#/cm3-s)

R_{ch} - Capture rate (#/cm3-s)

C_p - Constant proportional to hole-capture cross section

N_t - Total concentration of trapping centers

p - Hole concentration in the valence band

$f_F(E_t)$ - Fermi function at the trap energy

c_h - Constant or **Emission Coefficient**: The probability per unit time that a trapped hole is thermally emitted

Thermal equilibrium:

$$R_{eh} = R_{ch} \quad (3)$$

Using Boltzmann approximation $E_t - E_F \gg kT$ and consequently $f_F(E) \approx \exp\left(\frac{-(E-E_F)}{kT}\right)$:

$$c_h = p_0 C_p \quad (4)$$

E_F - Fermi level

p_0 - Hole concentration in the valence band at thermal equilibrium

Where :

$$p_0 = N_v \exp\left(\frac{-(E_F - E_v)}{kT}\right) \quad (5)$$

Finally, emission time constant is the characteristic **time it takes for a single carrier to be emitted once it is trapped**, considering $1 - f_F(E_t) \approx 1$ from Boltzmann approximation:

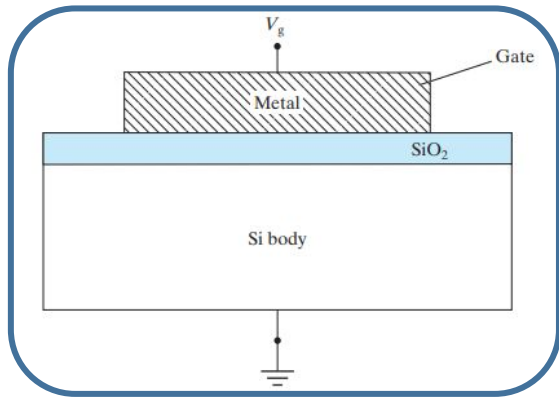
$$\tau_{e,h} = \frac{1}{c_h} = (C_p N_t)^{-1} \exp\left(\frac{(E_t - E_v)}{kT}\right) \quad (6)$$

$$\tau_{e,h} = \frac{1}{c_h} = (\sigma_h \bar{v} N_v)^{-1} \exp\left(\frac{(E_t - E_v)}{kT}\right) \quad (7)$$

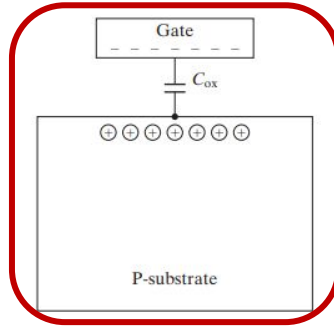
σ_h - Electron capture cross section

\bar{v} - Thermal velocity

$$\tau_c = \frac{1}{\sigma v_{th} N}$$

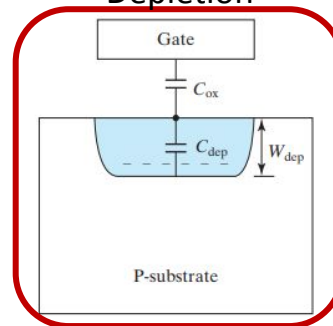


Accumulation



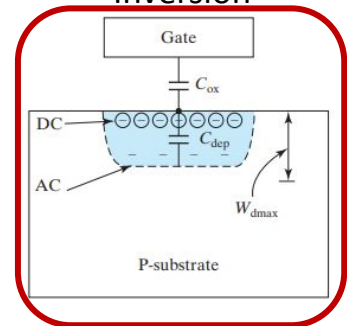
$$V_g < V_{fb}$$

Depletion

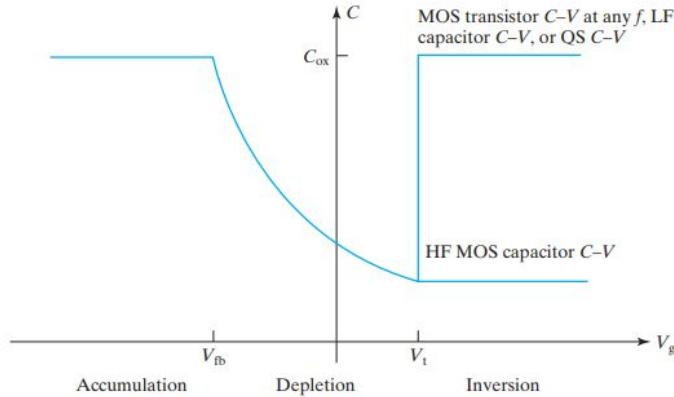


$$V_g > V_{fb}$$

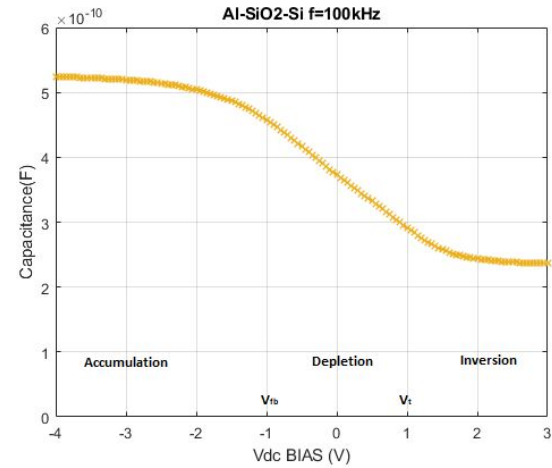
Inversion



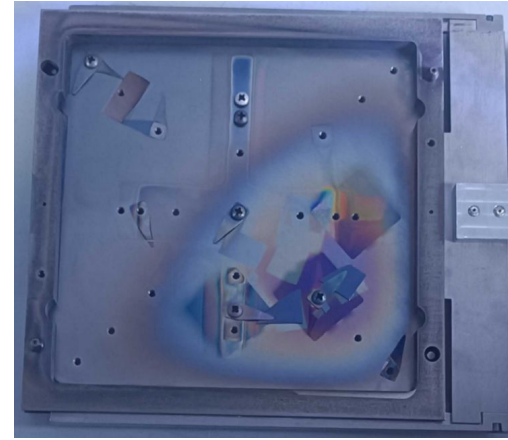
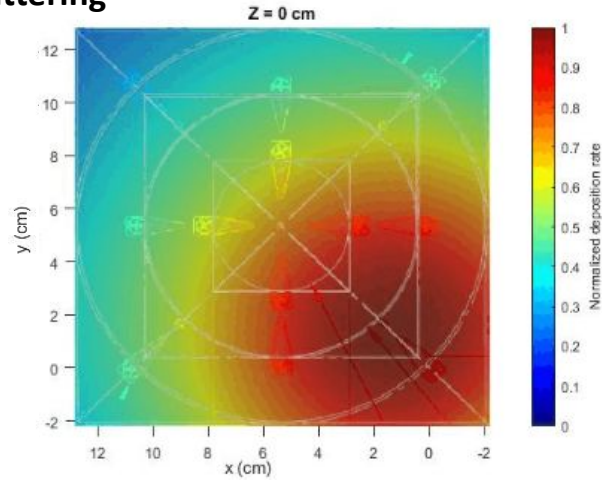
$$V_g > V_t$$



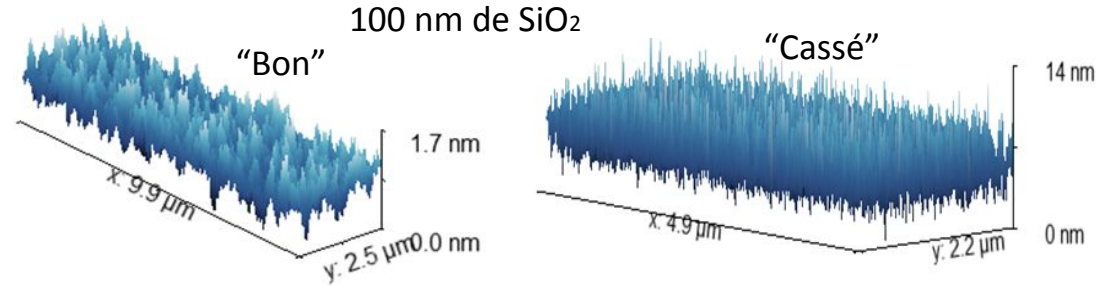
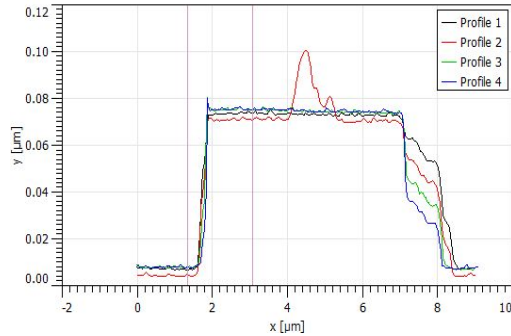
[Hu, C. (2010). *Modern semiconductor devices for integrated circuits* / Chenming Calvin Hu. Prentice Hall.]



RF sputtering

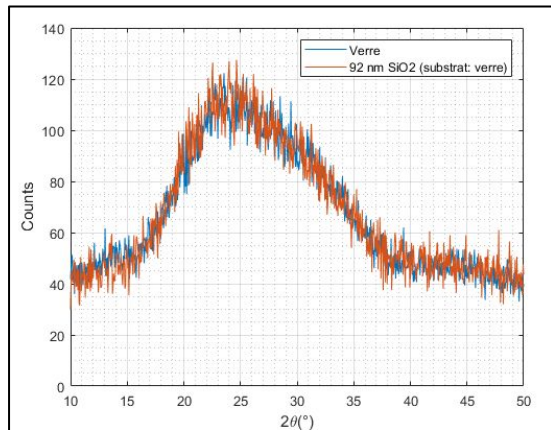


AFM (Atomic Force microscope)

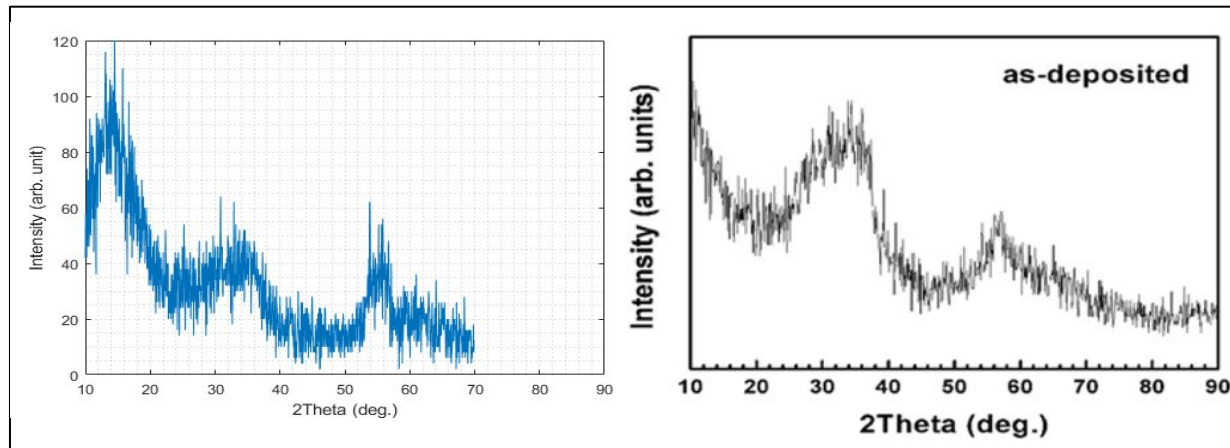


GIXRD (Grazing Incidence X-Ray Diffraction)

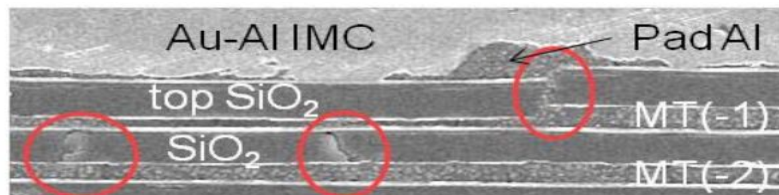
SiO₂



Ga₂O₃



Câblage (wirebonding)



[Hunter, Stevan & Rasmussen, Bryce & Ruud, Troy & Brizar, Guy & Vanderstraeten, Daniel & Martinez, Jose & Salas, Cesar & Salas, Marco & Sheffield, Steven & Schofield, Jason & Wilkins, Kyle. (2011). Use of harsh wire bonding to evaluate various bond pad structures.]