

A Preprint

ORIGINAL VERSION SUBMITTED ON JANUARY 30, 2026

A Fully Tunable Ultra-Low Power Current-Mode Memory Cell in Standard CMOS Technology

Arthur Fyon^{1,†}, Loris Mendolia^{1,†}, Jean-Michel Redouté¹, Alessio Franci^{1,2} and Guillaume Drion^{1,*}

¹Department of Electrical Engineering and Computer Science, University of Liège, Liège, Belgium

²WEL-T Department, WEL Research Institute, Wavre, Belgium

[†]These authors contributed equally to this work.

*Author to whom any correspondence should be addressed.

E-mail: gdrion@uliege.be

Keywords: Schmitt trigger, current-mode, spike-based logic, in-memory computing, subthreshold CMOS, neuromorphic computing, memory cell

Abstract

This work introduces a fully tunable, ultra-low power unipolar memory cell inspired by the Schmitt-trigger comparator and designed in Complementary Metal-Oxide-Semiconductor (CMOS) using only nine transistors. The proposed circuit operates entirely in the current domain and exploits a novel feedback configuration between two interdependent Heaviside-like thresholding elements to produce tunable bistable switching behavior. Its three key parameters—threshold current, hysteresis width, and output gain—are independently tunable via programmable bias currents, enabling flexibility across diverse analog computing applications. Unlike prior Schmitt-trigger designs, it simultaneously achieves current-mode operation, nanowatt-range power consumption, temperature stability, and full tunability, solely using standard MOSFET elements. Schematic-level simulations in a 180 nm CMOS process confirm robust hysteresis and resilience to device mismatch. Building on this circuit, we develop a complete family of spike-based logic gates using three-level current encoding, where the bistable memory retains the polarity of the last spike on each input indefinitely, enabling asynchronous logic operations without temporal windowing or refresh mechanisms. The same circuit also serves as the primitive for Bistable Memory Recurrent Units in analog neural networks, where the quantized hidden states provide inherent noise immunity. Together, these capabilities position the design as a versatile building block for next-generation neuromorphic processors integrating memory, logic, and recurrent computation.

1 Introduction

The rapid expansion of edge computing and Internet-of-Things applications has created an urgent demand for energy-efficient hardware capable of performing inference and signal processing directly at the sensor node [1]. In conventional von Neumann architectures, the physical separation between memory and processing units leads to significant energy and latency costs associated with data movement, a limitation commonly referred to as the memory wall [2, 3]. This bottleneck has become increasingly critical as the volume of data generated at the edge continues to grow, motivating the development of computing paradigms where processing occurs directly within or alongside memory [4, 5].

Two main in-memory computing approaches have emerged. Digital implementations based on static random-access memory (SRAM) arrays offer full compatibility with standard CMOS processes and reliable, deterministic operation [6, 7, 8]. However, ensuring read stability during computation requires augmented bitcells, and peripheral circuits (converters, sense amplifiers, adder trees) add substantial area and power overhead [9]. Memristive crossbar arrays offer an alternative with exceptional density and massive parallelism, enabling matrix-vector multiplication in a single step [3, 10, 11]. Yet these face fundamental challenges: device-to-device and cycle-to-cycle variability [12], programming nonlinearity, sneak path currents requiring selector devices [13], and fabrication steps beyond standard CMOS [5].

Table 1. Comparison with existing Schmitt trigger designs

Design	Mode	Resistorless	Power range	Tunable
[32]	Voltage	No (3)	1 mW to 10 mW	Yes
[34]	Voltage	Yes	1 μ W to 10 μ W	No
[35]	Voltage	No (2)	N/A	Yes
[36]	Voltage	No (3-4)	N/A	No
[37]	Voltage	No (4)	N/A	Partial
[38]	Voltage	No (1)	100 μ W to 1 mW	Yes
[42]	Current	Yes	10 μ W to 100 μ W	Partial
[43]	Current	Yes	10 μ W to 100 μ W	Yes
[44]	Current	Yes	100 mW to 1 W	Yes
[45]	Current	Yes	100 μ W to 1 mW	Yes
[46]	Current	No (2)	10 μ W to 100 μ W	No
[47]	Current	Yes	10 μ W to 100 μ W	Partial
Proposed	Current	Yes	1 nW to 10 nW	Yes

These limitations motivate compact bistable elements as alternative primitives combining CMOS reliability with ultra-low power operation. In neuromorphic architectures, bistable circuits provide noise-immune storage of binary states and quantized synaptic weights [14, 15, 16, 17, 18, 19]. Spike-based logic has also attracted interest, with existing approaches relying on memristive devices with inherent short-term temporal dynamics [20], conventional logic gates within spiking neural networks [21, 22], or emerging two-dimensional materials [23, 24]. However, a pure CMOS implementation capable of performing logic operations on spikes over an arbitrarily long time window without refresh or temporal constraints remains unexplored. More broadly, the growing demand for on-device machine learning at the edge, where power budgets are severely constrained and always-on operation is required, calls for circuit primitives that can support both logic and recurrent computation within nanowatt power envelopes and standard CMOS technology nodes.

Schmitt triggers are natural candidates for these applications, providing hysteresis and bistable switching [25, 26] while also serving in signal conditioning [27], threshold detection, and memory cells [28]. Recent work on the Bistable Memory Recurrent Unit (BMRU) has shown that Schmitt trigger activation functions enable direct analog implementation of recurrent neural networks with quantized hidden states and inherent noise immunity [29, 30, 31]. Voltage-mode implementations dominate the literature, including inverter-based positive feedback [32, 33], stacked inverters [34], operational transconductance amplifiers [35], current differencing buffered amplifiers [36], and current conveyors [37, 38]. These are often limited by fixed thresholds, reliance on external resistors, or high power. Current-mode designs [39, 40, 41, 42, 43, 44, 45, 46, 47] offer better compatibility with subthreshold operation, particularly in modern technology nodes [19], but typically lack full tunability of threshold and hysteresis width, or consume power above the μ W range. Table 1 summarizes key features of existing designs.

Motivated by the development of ultra-low power spike-based logic intelligence at the edge and by the limitations of existing designs, in this work we present a novel current-mode CMOS Schmitt trigger simultaneously achieving: (i) nW-range power consumption on standard CMOS technology; (ii) full tunability of thresholds and output current gain; (iii) compact nine-transistor implementation; and (iv) resistorless and capacitorless realization. The proposed circuit is intended for applications in ultra-low-power analog neuromorphic and event-driven systems rather than high-speed digital and mixed-signal logic. We build on this circuit to develop a complete family of spike-based elementary logic gates that operate in the nW range to compare the polarities of successive input spikes over an indefinite time window, demonstrating the potential of our tunable current-mode Schmitt trigger as a flexible primitive for asynchronous neuromorphic computation. The limitations of the current design are unipolar operation (positive currents only) and a trade-off between operating frequency, transistor count and size, and power consumption.

2 Method

The proposed circuit is based on a dual-Heaviside feedback structure, conceptually illustrated in Figure 1 (top left panel). It consists of two interdependent nonlinear thresholding elements:

- A primary Heaviside element that activates when the input current I_{in} exceeds a threshold I_{thresh} (the high threshold of the Schmitt trigger), producing an output current I_{gain} (the high output value).

- A secondary Heaviside element in feedback, triggered by the output of the first stage. It activates immediately to inject a feedback current I_{width} at the input of the circuit.

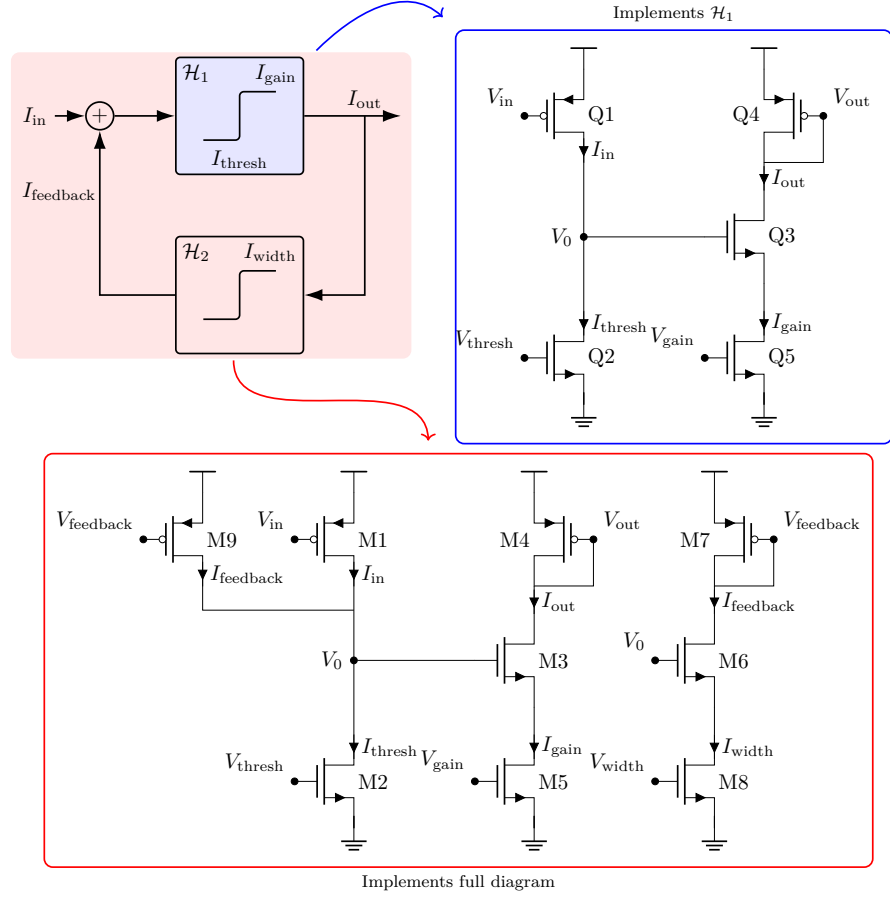


Figure 1. Conceptual architecture of the proposed dual-Heaviside feedback Schmitt trigger, along with the electronic schematics of the individual Heaviside circuit and the full Schmitt trigger.

The hysteresis behavior arises naturally from the feedback current I_{width} , which lowers the effective input threshold to $I_{\text{thresh}} - I_{\text{width}}$, thus enabling bistability. The three control parameters I_{thresh} , I_{gain} , and I_{width} are all independently adjustable via bias voltages, allowing straightforward tuning. Because the circuit operates only with positive currents, the constraint $I_{\text{thresh}} > I_{\text{width}}$ must be met to preserve bistability, ensuring that the positive feedback does not override the comparator threshold.

The top right panel (blue) of Figure 1 shows a minimal CMOS circuit that implements a fully tunable unipolar Heaviside function ($\mathcal{H}_1$) in current mode. The input current is provided through a voltage V_{in} at the output of a PMOS current mirror (Q1), while the threshold current I_{thresh} is set through a voltage V_{thresh} by an NMOS transistor (Q2). Together, Q1 and Q2 form a switching current comparator. If $I_{\text{in}} < I_{\text{thresh}}$, then $V_0 \approx 0$ and Q3 is off, resulting in a zero output current I_{out} . As soon as $I_{\text{in}} > I_{\text{thresh}}$, V_0 increases to the supply voltage and Q3 turns on, allowing current to flow in the output branch. At that point, the current flowing through this branch corresponds to the bias current I_{gain} , also set through a voltage V_{gain} by an NMOS transistor (Q5). The output current flows through the diode-connected transistor Q4 and can be mirrored to other stages via a PMOS transistor driven by V_{out} .

The bottom panel (red) of Figure 1 represents the feedback interconnection of the two Heaviside functions, forming a current-mode unipolar Schmitt trigger capable of operating with nW-level supply power. $\mathcal{H}_1$ (Q1–Q5) is implemented through transistors M1–M5. For $\mathcal{H}_2$ to switch concurrently with $\mathcal{H}_1$, they share the same switching voltage V_0 , removing the need for a separate comparator branch (like M1–M2). This means that if $I_{\text{in}} < I_{\text{thresh}}$, M6 is off and $I_{\text{feedback}} = I_{\text{out}} = 0$. Once $I_{\text{in}} > I_{\text{thresh}}$, M6 turns on and I_{feedback} reaches I_{width} , the bias current of the feedback branch set through V_{width} by an NMOS transistor (M8). This feedback current is mirrored through a PMOS current mirror (M7 and M9), and injected back into the comparator branch of $\mathcal{H}_1$ (M1, M2, and M9), thereby increasing the input current by I_{feedback} .

The resulting Schmitt trigger characteristics can be expressed as:

$$I_{th,high} = I_{thresh} \quad (1)$$

$$I_{th,low} = I_{thresh} - I_{width} \quad (2)$$

$$\Delta I_{hyst} = I_{width} \quad (3)$$

where $I_{th,high}$ and $I_{th,low}$ denote the upper and lower switching thresholds, respectively, and ΔI_{hyst} is the hysteresis width. The output current switches between approximately zero and I_{gain} . Beyond the listed metrics in Table 1, the proposed circuit achieves its performance with only nine transistors, hence improving on transistor count as compared to previous designs.

The circuit was simulated using the X-FAB 180 nm CMOS process. All NMOS transistors were sized with a width of 5 μm and a length of 5 μm , while PMOS transistors were sized with a width of 5.5 μm and a length of 5 μm . This conservative sizing reduces mismatch when properly laid out and mitigates undesired short-channel effects. The exceptions are transistors M3 and M6, which operate primarily as switches and were sized with a width of 2 μm and minimal length. While the relatively large transistor sizes mitigate mismatch, they also significantly increase parasitic capacitance, limiting the bandwidth to approximately 1 kHz. This bandwidth is well-suited to bio-medical and human-in-the-loop edge applications. In such contexts, ultra-low power consumption takes precedence over high-speed operation.

3 Results

All schematic-level simulations were conducted using SPICE with standard X-FAB 180 nm models, with a supply voltage of 1.8 V. Unless otherwise stated, the following baseline parameters were used: $I_{gain} = 486$ pA, $I_{thresh} = 368$ pA, and $I_{width} = 216$ pA. These values yield switching thresholds of 150 pA and 350 pA with a high output state of 500 pA. These values represent a representative operating point chosen to demonstrate the circuit functionality. In practice, bias currents are generated from a stable reference current via standard current mirrors, and the linear tunability demonstrated in subsequent sections allows straightforward adjustment to application-specific requirements.

The following analyses evaluate transient behavior, DC characteristics, robustness to mismatch and temperature, tunability, and spike-based logic operations.

3.1 Transient Response and DC Characteristics

To evaluate hysteresis, the input current I_{in} was swept linearly from 0 to 500 pA and then back to 0 using a triangular waveform. As shown in Figure 2A for different operating temperatures, the circuit exhibits clear bistable behavior with sharp transitions. The switching points align with the expected levels of $I_{thresh} - I_{width}$ and I_{thresh} , and the high-state output current closely follows I_{gain} . A small ($\sim 10\%$) overshoot is observed at transitions, attributed to the positive feedback inherent in the Heaviside interconnection.

DC simulations confirm the existence of two stable states and well-defined hysteresis (Figure 2B). Both the threshold currents and the high-state output level are independently tunable through their respective bias currents. In both cases, temperature mainly affects the upper switching point of the hysteresis, which is determined by the M1–M2 comparator. However, since the circuit operates in the ultra-low power regime, typical operating conditions remain well below 80 $^{\circ}\text{C}$, ensuring robust operation over temperature.

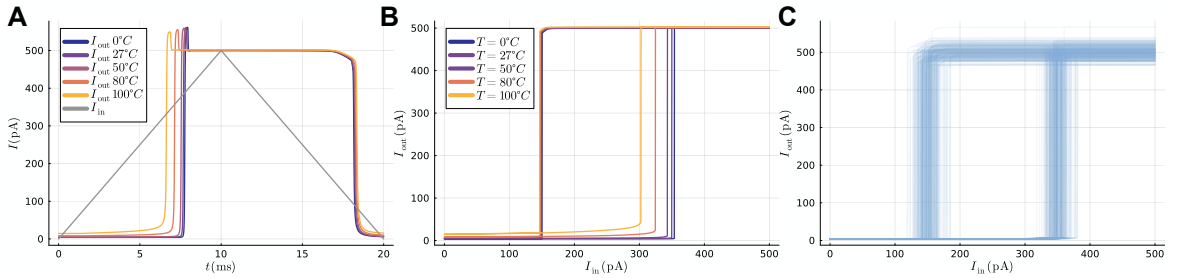


Figure 2. **A.** Transient simulation of the proposed Schmitt trigger under triangular input current for different operating temperatures. **B.** DC sweep demonstrating hysteretic behavior for different operating temperatures. **C.** Monte Carlo analysis of the proposed Schmitt trigger in DC input sweep analysis with 3σ process variation at room temperature. Baseline parameters: $I_{gain} = 486$ pA, $I_{thresh} = 368$ pA, and $I_{width} = 216$ pA.

3.2 Mismatch Analysis

Monte Carlo simulations were performed under a 3σ mismatch variation to evaluate the robustness of the design to device mismatch. The circuit consistently maintained correct bistable switching behavior, with only minor deviations, typically a few tens of pA, in the threshold currents, hysteresis width, and high output level (Figure 2C). These variations remain well within functional margins and do not compromise the qualitative operation of the Schmitt trigger.

3.3 Tuning Properties

We systematically swept each bias current to assess its effect on the output behavior. Results confirm that each parameter (I_{gain} , I_{thresh} , and I_{width}) controls its corresponding function (output level, threshold, and hysteresis width) in a linear and independent manner for different operating temperatures.

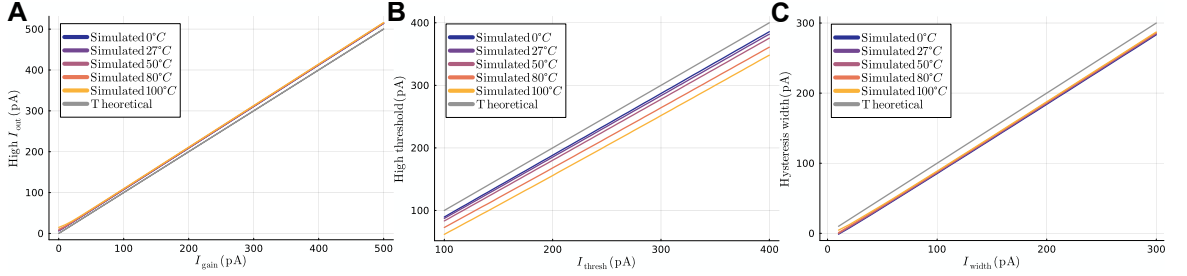


Figure 3. **A.** I_{gain} DC sweep analysis from 0 to 500 pA of the proposed Schmitt trigger for different operating temperatures. **B.** I_{thresh} DC sweep analysis from 100 pA to 400 pA of the proposed Schmitt trigger for different operating temperatures with $I_{\text{width}} = 50$ pA. **C.** I_{width} DC sweep analysis from 10 pA to 300 pA of the proposed Schmitt trigger for different operating temperatures. Baseline parameters: $I_{\text{gain}} = 486$ pA, $I_{\text{thresh}} = 368$ pA, and $I_{\text{width}} = 216$ pA.

Figure 3A shows the effect of sweeping I_{gain} from 0 to 500 pA. As expected, the high output level increases linearly, although a small offset is present due to subthreshold leakage currents (on the order of a few pA). As a result, the relative error between I_{gain} and the actual output current decreases with increasing current, reaching a low 2.8 % at 500 pA at room temperature.

Similar results were obtained for threshold and hysteresis width. For I_{thresh} , the sweep range was limited to 100 pA–400 pA to maintain bistability and avoid approaching either 0 or I_{gain} . For I_{width} , the range was 10 pA–300 pA to ensure $I_{\text{width}} < I_{\text{thresh}}$ throughout. Figures 3B and 3C show that the corresponding thresholds and hysteresis widths also follow a linear trend with minor offsets. The relative errors at room temperature were measured at 4.5 % and 5.25 %, respectively, for the highest tested currents. These analyses confirm that temperature mainly affects I_{thresh} , while lowering I_{width} to 50 pA did not change this effect compared with Figure 2B.

3.4 Spike-Based Logic Operations

The proposed Schmitt trigger can implement spike-based logic operations by exploiting its hysteretic response and bistable memory. The unipolar constraint naturally accommodates a three-level current encoding scheme: 0 pA represents logic 0 (negative spike), 500 pA represents logic 1 (positive spike), and the intermediate resting state at 250 pA indicates that no spike has yet been received, corresponding to an undefined logic value. This encoding enables bidirectional signaling within the strictly positive current domain.

The key property enabling spike-based logic operations is that the bistable nature of the circuit provides persistent memory of the polarity of the most recent received spike: once an input spikes positively or negatively, that state is retained until the next spike arrives. The logic operation is therefore determined solely by the polarity of the last spike received on each of the logic gate inputs, irrespective of the time elapsed since those spikes occurred. When configured with appropriate bias currents and input summation, the circuit responds selectively to specific polarity combinations: an AND gate activates only when both inputs last spiked positively; an OR gate activates when either input last spiked positively; NAND and NOR gates invert these responses; and an XOR gate activates only when the two inputs differ in their last spike polarity. This polarity-based encoding mirrors neuromorphic computing principles [21, 20, 22, 23, 17], while the persistent memory eliminates the need for temporal windowing or refresh circuits, a capability not demonstrated by prior memristive or conventional CMOS spike-based approaches.

Figure 4 shows the circuit implementation of the XOR gate, from which the other four logic gates are readily derived. Each input is fed into both a Schmitt trigger and an inverted Schmitt

trigger to detect spike polarity. These outputs are then summed depending on the desired logic operation. For instance, the NOR gate sums both inverted Schmitt trigger outputs and passes them through a thresholding element at 750 pA that outputs high when both inverted outputs are high, indicating that the last spikes on both input branches were negative. Similarly, the AND gate sums both non-inverted outputs with a threshold detecting when both last spikes were positive, while OR and NAND gates use analogous configurations. The XOR gate exploits asymmetric hysteresis to distinguish between matched polarities (both positive or both negative) and mismatched polarities (one positive, one negative).

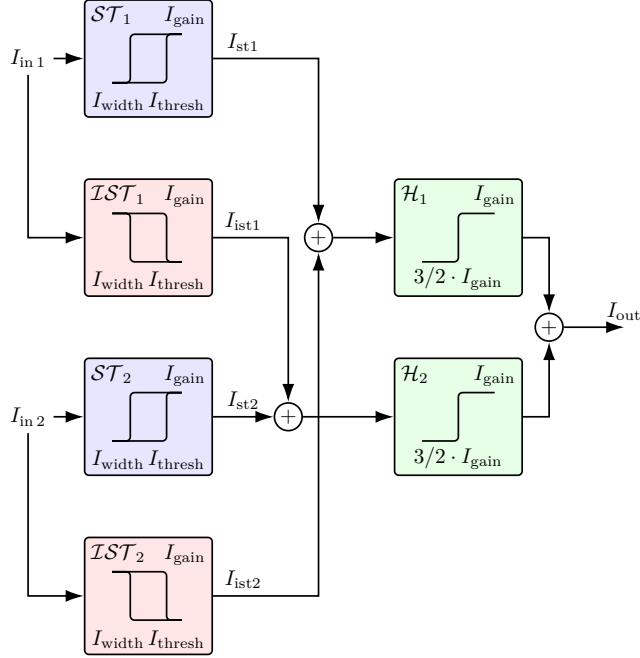


Figure 4. Circuit implementation of the XOR logic gate using the proposed Schmitt trigger. Each input is processed by both a standard and an inverted Schmitt trigger to detect spike polarity. The outputs are summed and thresholded to produce the XOR operation. The other four logic gates (AND, OR, NAND, NOR) follow analogous configurations with different summation and threshold arrangements. For the AND gate, I_{st1} and I_{st2} (both standard outputs) are summed; for the NOR gate, I_{ist1} and I_{ist2} (both inverted outputs) are summed; the OR and NAND gates use complementary summation configurations with appropriate threshold inversions.

Figure 5 presents simulation results for all five logic gates under different spike polarity combinations. The simulations confirm that the three-level encoding preserves the strictly positive current constraint while enabling full logic functionality with persistent memory.

These spike-based logic gates inherit the nanowatt-range power consumption of the base Schmitt trigger, making them suitable for massively parallel architectures. The hysteresis provides inherent noise immunity, as spurious fluctuations do not trigger state changes. The gates can be cascaded to build more complex computational primitives such as half-adders, full-adders, and sequential logic elements. Unlike purely digital implementations, these analog gates operate entirely within the positive current domain and preserve spike polarity for arbitrarily long time intervals, enabling asynchronous event-driven processing where logic operations occur only when new spikes arrive.

The ability to perform logic operations directly in the current domain based solely on spike polarity is particularly valuable for asynchronous neuromorphic processors and event-driven edge computing [16]. The persistent memory property enables ultra-sparse computation where power is consumed only during spike transitions. Combined with the BMRU recurrent processing capability described in the introduction, these logic gates enable compact neuromorphic processors integrating memory, computation, and decision-making in a unified current-mode architecture.

4 Discussion

The proposed Schmitt trigger and its derived logic gates address a gap in the neuromorphic computing landscape: the need for a pure CMOS primitive that combines bistable memory with ultra-low power operation, without the variability and fabrication complexity of memristive devices or the area overhead of augmented SRAM cells.

The observed mismatches in the Monte Carlo analysis arise primarily from variations in current mirrors and biasing transistors. Their impact could be further reduced by increasing device

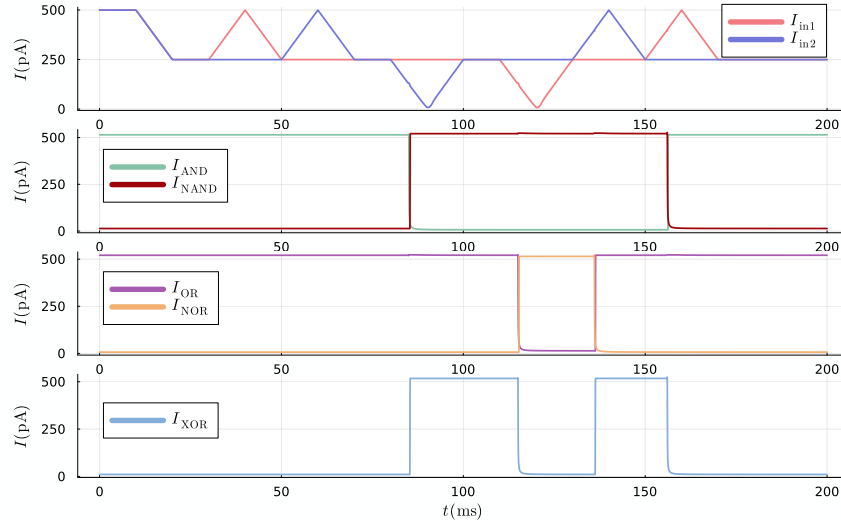


Figure 5. Simulation results of all five spike-based logic gates (AND, NAND, OR, NOR, XOR) for different input spike polarity combinations (top). The three-level current encoding (0 pA = logic 0 / negative spike, 250 pA = undefined / no spike received, 500 pA = logic 1 / positive spike) enables bidirectional logic operations while maintaining the unipolar current constraint. Each gate correctly responds to the polarity of the last spike on each input, with outputs persisting indefinitely until new spikes arrive. The power consumption of these gates remains in the tens of nW range.

dimensions, though this would increase the silicon footprint, a trade-off dependent on the intended application and area constraints. Conversely, decreasing transistor dimensions risks compromising the reliability of the hysteresis by causing undesirable overlaps between the low and high switching thresholds, which explains the relatively large transistor sizes selected for our simulations.

The predictable offsets observed in the tunability analysis do not impair functionality. The relationship between control currents and actual switching parameters remains monotonic and approximately linear despite minor offsets due to subthreshold leakage. These deviations can be compensated by simple calibration (*e.g.*, lookup table or linear correction), allowing accurate control of thresholds and hysteresis without additional circuitry.

For the spike-based logic gates, the three-level current encoding scheme introduces additional design considerations. The threshold placement for each gate must account for process variations to ensure correct discrimination between polarity combinations. However, the same tunability that enables flexible Schmitt trigger configuration also allows adjustment of the summing and thresholding stages, providing robustness against variability. The persistent memory property, where spike polarity is retained until explicitly updated, eliminates timing constraints that complicate conventional spike-based logic implementations, but requires that input spikes be sufficiently separated to avoid overlap during the transient response.

The tunability and consistent operation of this circuit allow it to retain functionality under higher bias currents, in the order of nA or μ A. This flexibility enables use in both power-critical scenarios and applications where signal integrity and low noise are paramount. Compared with memristive approaches that offer higher density but suffer from variability and nonstandard manufacturing processes, and SRAM-based approaches that provide reliability but at higher area and power cost, the proposed design occupies a distinct niche: pure CMOS implementation with nanowatt operation and persistent state retention.

5 Conclusion

This work introduces a compact, fully tunable, and ultra-low power Schmitt trigger operating in the current domain, implemented with nine transistors in standard CMOS technology in the subthreshold regime. Unlike previous designs, the proposed solution operates without resistors or capacitors, enabling monolithic integration while offering independent configurability of threshold current, hysteresis width, and output gain. The bistable behavior, achieved through a novel dual-Heaviside feedback architecture, yields robust transitions within nW power budgets. Schematic-level simulations confirm correct hysteretic behavior, independent tunability of circuit properties, and resilience to simulated device mismatch and temperature variations.

Building on this circuit, we developed a complete family of spike-based logic gates using a three-level current encoding scheme that represents positive spikes, negative spikes, and a resting

state within the strictly positive current domain. The key innovation is that the bistable memory retains the polarity of the last spike on each input indefinitely, enabling logic operations that compare spike polarities without temporal windowing or refresh mechanisms, a capability not reported in prior memristive spike-based logic implementations, which exhibit inherent temporal dynamics, or by conventional digital implementations. All fundamental Boolean operations (AND, OR, NAND, NOR, XOR) were demonstrated through SPICE simulations, with each gate inheriting the nanowatt-range power consumption and noise immunity of the base Schmitt trigger. These gates can be cascaded to construct more complex computational primitives, enabling complete neuromorphic processors operating in the current domain.

Beyond spike-based logic, the proposed Schmitt trigger directly implements the BMRU, a specific RNN whose input-output relationship corresponds one-to-one with the Schmitt trigger transfer function [29, 30]. Because the hidden states are quantized, noise and device variations do not accumulate across time steps, providing inherent robustness without explicit error correction [11, 3, 31]. This circuit has been employed in a hardware-software co-design demonstration achieving over 90% accuracy on keyword spotting tasks at approximately 100 nW power consumption [31], suggesting at least three orders of magnitude improvement over TinyML implementations achieving comparable accuracy [48, 49, 50, 51].

The dual functionality demonstrated in this work, spike-based logic and recurrent neural network primitive, positions the proposed Schmitt trigger as a versatile building block for next-generation neuromorphic hardware. The same circuit can serve as a memory element in recurrent layers and as a logic gate in combinatorial processing stages, enabling unified current-mode architectures where memory, computation, and decision-making are tightly integrated. The persistent polarity memory provides both noise immunity and ultra-sparse asynchronous operation, where logic states persist without dynamic power consumption between spike events. Future work will focus on layout implementation, post-layout simulation, and experimental silicon validation to characterize the impact of layout parasitics on bandwidth and matching.

Acknowledgments

The technology described in this paper is the subject of a U.S. Provisional Patent Application No. 63/897,109 and European Patent Application No. EP26175243.0, entitled “Current-mode switching circuits and analog computational systems”.

Funding

Arthur Fyon is a Postdoctoral Researcher of the Fonds de la Recherche Scientifique – FNRS, supported by grant ASP-REN 40024838. Loris Mendolia is a FRIA Grantee of the Fonds de la Recherche Scientifique – FNRS, supported by grant FRIA-B2 40029909. This work was supported by the Belgian Government through the Federal Public Service Policy and Support, under grant NEMODEI2.

Author contributions

- Arthur Fyon: Conceptualization (lead), Data curation, Formal analysis (lead), Investigation (lead), Methodology (equal), Software, Visualization (lead), Writing - original draft (lead), Writing - review and editing (lead).
- Loris Mendolia: Conceptualization (lead), Data curation, Formal analysis (lead), Investigation (lead), Methodology (equal), Software, Visualization (lead), Writing - original draft (lead), Writing - review and editing (lead).
- Jean-Michel Redouté: Conceptualization (supporting), Formal analysis (supporting), Funding acquisition (equal), Investigation (supporting), Methodology (equal), Project administration (supporting), Resources (equal), Supervision (supporting), Writing - original draft (supporting), Writing - review and editing (supporting).
- Alessio Franci: Conceptualization (lead), Formal analysis (supporting), Funding acquisition (equal), Investigation (supporting), Methodology (equal), Project administration (equal), Resources (equal), Supervision (equal), Writing - original draft (supporting), Writing - review and editing (supporting).
- Guillaume Drion: Conceptualization (lead), Formal analysis (supporting), Funding acquisition (equal), Investigation (supporting), Methodology (equal), Project administration

(equal), Resources (equal), Supervision (equal), Writing - original draft (supporting), Writing - review and editing (supporting).

Data availability

All data that support the findings of this study are included within the article. Cadence Virtuoso design files (schematics, symbols, and Maestro configurations) are not included in the public repository due to software licensing constraints and version compatibility issues. These files are available upon reasonable request to the corresponding author for researchers with access to Cadence tools.

Supplementary data

Transistors dimensions optimized for mismatch used in all simulations presented in this work are reported in Table 2.

Table 2. Ultra-low power Schmitt trigger circuit component dimensions.

Transistors	Q/M1 & Q/M4 & M7 & M9	Q/M2 & Q/M5 & M8	Q/M3 & M6
$W \times L$ (μm)	5.5×5	5×5	2×0.18

References

- [1] X. Ren et al. “A current-mode multiply-accumulate macro in sensing-computing fusion system for feature extraction and redundancy reduction”. In: *IEEE Trans. Circuits Syst. II, Exp. Briefs* (2025). DOI: [10.1109/tcsii.2025.3543173](https://doi.org/10.1109/tcsii.2025.3543173).
- [2] R. Sarpeshkar. “Analog Versus Digital: Extrapolating from Electronics to Neurobiology”. In: *Neural Comput.* 10.7 (1998), pp. 1601–1638. DOI: [10.1162/089976698300017052](https://doi.org/10.1162/089976698300017052).
- [3] A. Sebastian et al. “Memory devices and applications for in-memory computing”. In: *Nat. Nanotechnol.* 15.7 (2020), pp. 529–544. DOI: [10.1038/s41565-020-0655-z](https://doi.org/10.1038/s41565-020-0655-z).
- [4] D. Ielmini and H.-S. P. Wong. “In-Memory Computing with Resistive Switching Devices”. In: *Nat. Electron.* 1.6 (2018), pp. 333–343. DOI: [10.1038/s41928-018-0092-2](https://doi.org/10.1038/s41928-018-0092-2).
- [5] F. Aguirre et al. “Hardware implementation of memristor-based artificial neural networks”. In: *Nat. Commun.* 15.1 (2024), p. 1974. DOI: [10.1038/s41467-024-45670-9](https://doi.org/10.1038/s41467-024-45670-9).
- [6] C.-J. Jhang et al. “Challenges and trends of SRAM-based computing-in-memory for AI edge devices”. In: *IEEE Trans. Circuits Syst. I* 68.5 (2021), pp. 1773–1786. DOI: [10.1109/tcsi.2021.3064189](https://doi.org/10.1109/tcsi.2021.3064189).
- [7] Z. Lin et al. “A review on SRAM-based computing in-memory: Circuits, functions, and applications”. In: *J. Semicond.* 43.3 (2022), p. 031401. DOI: [10.1088/1674-4926/43/3/031401](https://doi.org/10.1088/1674-4926/43/3/031401).
- [8] P. Mannocci et al. “A fully integrated analogue closed-loop in-memory computing accelerator based on static random-access memory”. In: *Nat. Electron.* (2026), pp. 1–13. DOI: [10.1038/s41928-025-01549-1](https://doi.org/10.1038/s41928-025-01549-1).
- [9] H. Noguchi et al. “Which is the best dual-port SRAM in 45-nm process technology?—8T, 10T single end, and 10T differential”. In: *2008 IEEE International Conference on Integrated Circuit Design and Technology and Tutorial*. IEEE. 2008, pp. 55–58. DOI: [10.1109/icicdt.2008.4567245](https://doi.org/10.1109/icicdt.2008.4567245).
- [10] D. Marković et al. “Physics for neuromorphic computing”. In: *Nat. Rev. Phys.* 2.9 (2020), pp. 499–510. DOI: [10.1038/s42254-020-0208-2](https://doi.org/10.1038/s42254-020-0208-2).
- [11] V. Joshi et al. “Accurate deep neural network inference using computational phase-change memory”. In: *Nat. Commun.* 11.1 (2020), p. 2473. DOI: [10.1038/s41467-020-16108-9](https://doi.org/10.1038/s41467-020-16108-9).
- [12] A. P. James and L. O. Chua. “Variability-aware memristive crossbars—a tutorial”. In: *IEEE Trans. Circuits Syst. II* 69.6 (2022), pp. 2570–2574. DOI: [10.1109/tcsii.2022.3169416](https://doi.org/10.1109/tcsii.2022.3169416).
- [13] L. Shi et al. “Research progress on solutions to the sneak path issue in memristor crossbar arrays”. In: *Nanoscale Adv.* 2.5 (2020), pp. 1811–1827. DOI: [10.1039/d0na00100g](https://doi.org/10.1039/d0na00100g).
- [14] P. Livi and G. Indiveri. “A current-mode conductance-based silicon neuron for address-event neuromorphic systems”. In: *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*. 2009, pp. 2898–2901. DOI: [10.1109/iscas.2009.5118408](https://doi.org/10.1109/iscas.2009.5118408).

- [15] C. Bartolozzi, S. Mitra, and G. Indiveri. “An ultra low power current-mode filter for neuromorphic systems and biomedical signal processing”. In: *Proc. IEEE Biomed. Circuits Syst. Conf. (BioCAS)*. 2006, pp. 130–133. DOI: [10.1109/biocas.2006.4600325](https://doi.org/10.1109/biocas.2006.4600325).
- [16] D. V. Christensen et al. “2022 roadmap on neuromorphic computing and engineering”. In: *Neuromorphic Comput. Eng.* 2.2 (2022), p. 022501. DOI: [10.1088/2634-4386/ac4a83](https://doi.org/10.1088/2634-4386/ac4a83).
- [17] L. Khacef et al. “Spike-based local synaptic plasticity: A survey of computational models and neuromorphic circuits”. In: *Neuromorphic Comput. Eng.* 3.4 (2023), p. 042001. DOI: [10.1088/2634-4386/ad05da](https://doi.org/10.1088/2634-4386/ad05da).
- [18] C. D. Schuman et al. “Opportunities for neuromorphic computing algorithms and applications”. In: *Nat. Comput. Sci.* 2.1 (2022), pp. 10–19. DOI: [10.1038/s43588-021-00184-y](https://doi.org/10.1038/s43588-021-00184-y).
- [19] A. Rubino et al. *Neuromorphic analog circuits for robust on-chip always-on learning in spiking neural networks*. 2023. arXiv: [2307.06084](https://arxiv.org/abs/2307.06084) [cs.NE].
- [20] E. Gale. “Neuromorphic computation with spiking memristors: habituation, experimental instantiation of logic gates and a novel sequence-sensitive perceptron model”. In: *Faraday Discuss.* 213 (2019), pp. 521–551. DOI: [10.1039/C8FD00111A](https://doi.org/10.1039/C8FD00111A).
- [21] A. Ayuso-Martinez et al. “Construction of a spike-based memory using neural-like logic gates based on Spiking Neural Networks on SpiNNaker”. In: *IEEE Trans. Emerg. Top. Comput.* 11 (2023), pp. 868–881. DOI: [10.1109/TETC.2023.3281063](https://doi.org/10.1109/TETC.2023.3281063).
- [22] L. Mo and M. Wang. “LogicSNN: A Unified Spiking Neural Networks Logical Operation Paradigm”. In: *Electronics* 10.17 (2021), p. 2123. DOI: [10.3390/electronics10172123](https://doi.org/10.3390/electronics10172123).
- [23] H. Chen et al. “Logic gates based on neuristors made from two-dimensional materials”. In: *Nat. Electron.* 4.6 (2021), pp. 399–404. DOI: [10.1038/s41928-021-00591-z](https://doi.org/10.1038/s41928-021-00591-z).
- [24] G. Migliato Marega et al. “Logic-in-memory based on an atomically thin semiconductor”. In: *Nature* 587.7832 (2020), pp. 72–77. DOI: [10.1038/s41586-020-2861-0](https://doi.org/10.1038/s41586-020-2861-0).
- [25] B. L. Dokić. “CMOS Schmitt triggers”. In: *IEE Proc. G* 131 (1984), pp. 197–202. DOI: [10.1049/ip-g-1.1984.0037](https://doi.org/10.1049/ip-g-1.1984.0037).
- [26] I. M. Filanovsky and H. Baltes. “CMOS Schmitt trigger design”. In: *IEEE Trans. Circuits Syst. I* 41.1 (2002), pp. 46–49. DOI: [10.1109/81.260219](https://doi.org/10.1109/81.260219).
- [27] Z. Wang. “CMOS adjustable Schmitt triggers”. In: *IEEE Trans. Instrum. Meas.* 40.3 (2002), pp. 601–605. DOI: [10.1109/19.87026](https://doi.org/10.1109/19.87026).
- [28] J. P. Kulkarni, K. Kim, and K. Roy. “A 160 mV robust Schmitt trigger based subthreshold SRAM”. In: *IEEE J. Solid-State Circuits* 42.10 (2007), pp. 2303–2313. DOI: [10.1109/jssc.2007.897148](https://doi.org/10.1109/jssc.2007.897148).
- [29] F. De Geeter et al. *Parallelizable memory recurrent units*. 2026. arXiv: [2601.09495](https://arxiv.org/abs/2601.09495) [cs.LG].
- [30] J. Brandoit et al. *Improving the Performance and Learning Stability of Parallelizable RNNs Designed for Ultra-Low Power Applications*. 2026. arXiv: [2605.11855](https://arxiv.org/abs/2605.11855) [cs.LG].
- [31] A. Fyon et al. *Hardware-Software Co-Design of Scalable, Energy-Efficient Analog Recurrent Computations*. 2026. arXiv: [2605.15216](https://arxiv.org/abs/2605.15216) [cs.AR].
- [32] M. Siripruchyanun and J. Hirunporm. “A fully/electronically controllable voltage-mode Schmitt trigger based on only single VDGA and its applications”. In: *AEU - Int. J. Electron. Commun.* 131 (2021), p. 153602. DOI: [10.1016/j.aeue.2020.153602](https://doi.org/10.1016/j.aeue.2020.153602).
- [33] M. Steyaert and W. Sansen. “Novel CMOS Schmitt trigger”. In: *Electron. Lett.* 22.4 (1986), pp. 203–204. DOI: [10.1049/el:19860142](https://doi.org/10.1049/el:19860142).
- [34] H. Traff. “Novel approach to high-speed CMOS current comparators”. In: *Electron. Lett.* 28.3 (1992), pp. 310–311. DOI: [10.1049/el:19920192](https://doi.org/10.1049/el:19920192).
- [35] K. Kim, H.-W. Cha, and W.-S. Chung. “OTA-R Schmitt trigger with independently controllable threshold and output voltage levels”. In: *Electron. Lett.* 33.13 (1997), pp. 1103–1105. DOI: [10.1049/el:19970786](https://doi.org/10.1049/el:19970786).
- [36] R. Pal et al. “Single CDBA-based voltage-mode bistable multivibrator and its applications”. In: *Circuits Syst.* 6.11 (2015), pp. 237–251. DOI: [10.4236/cs.2015.611024](https://doi.org/10.4236/cs.2015.611024).
- [37] A. Srinivasulu. “A novel current conveyor-based Schmitt trigger and its application as a relaxation oscillator”. In: *Int. J. Circuit Theory Appl.* 39.6 (2011), pp. 679–686. DOI: [10.1002/cta.669](https://doi.org/10.1002/cta.669).

- [38] M. Siripruchyanun, P. Satthaphol, and K. Payakkakul. “A simple fully controllable Schmitt trigger with electronic method using VDTA”. In: *Appl. Mech. Mater.* 781 (2015), pp. 180–183. DOI: [10.4028/www.scientific.net/amm.781.180](https://doi.org/10.4028/www.scientific.net/amm.781.180).
- [39] Z. Wang and W. Guggenbohl. “Novel CMOS current Schmitt trigger”. In: *Electron. Lett.* 24.24 (1988), pp. 1514–1516. DOI: [10.1049/el:19881034](https://doi.org/10.1049/el:19881034).
- [40] F. Yuan. “A high-speed differential CMOS Schmitt trigger with regenerative current feedback and adjustable hysteresis”. In: *Analog Integr. Circuits Signal Process.* 63.1 (2010), pp. 121–127. DOI: [10.1007/s10470-009-9374-y](https://doi.org/10.1007/s10470-009-9374-y).
- [41] M. A. Eldeeb et al. “Low-voltage subthreshold CMOS current mode circuits: Design and applications”. In: *AEU-Int. J. Electron. Commun.* 82 (2017), pp. 251–264. DOI: [10.1016/j.aeue.2017.08.049](https://doi.org/10.1016/j.aeue.2017.08.049).
- [42] T. Srivyshnavi and A. Srinivasulu. “A current-mode Schmitt trigger based on current differencing transconductance amplifier”. In: *Proc. IEEE Int. Conf. Signal Process., Commun. Netw. (ICSCN)*. 2015, pp. 1–4. DOI: [10.1109/icscn.2015.7219884](https://doi.org/10.1109/icscn.2015.7219884).
- [43] A. Kumar and B. Chaturvedi. “Novel electronically controlled current-mode Schmitt trigger based on single active element”. In: *AEU - Int. J. Electron. Commun.* 82 (2017), pp. 160–166. DOI: [10.1016/j.aeue.2017.08.007](https://doi.org/10.1016/j.aeue.2017.08.007).
- [44] P. Silapan and M. Siripruchyanun. “A simple current-mode Schmitt trigger employing only single MO-CTTA”. In: *Proc. 6th IEEE Int. Conf. Electr. Eng./Electron., Comput., Telecommun. Inf. Technol. (ECTI-CON)*. 2009, pp. 556–559. DOI: [10.1109/ecticon.2009.5137068](https://doi.org/10.1109/ecticon.2009.5137068).
- [45] P. Silapan and M. Siripruchyanun. “Fully and electronically controllable current-mode Schmitt triggers employing only single MO-CCCDTA and their applications”. In: *Analog Integr. Circuits Signal Process.* 68.1 (2011), pp. 111–128. DOI: [10.1007/s10470-010-9593-2](https://doi.org/10.1007/s10470-010-9593-2).
- [46] S. Madira, V. V. Reddy, and A. Srinivasulu. “Current-mode Schmitt trigger based on ZC-current differencing transconductance amplifier”. In: *Proc. IEEE Int. Conf. Inventive Comput. Technol. (ICICT)*. 2016, pp. 1–5. DOI: [10.1109/inventive.2016.7823226](https://doi.org/10.1109/inventive.2016.7823226).
- [47] R. Linitha, A. Srinivasulu, and V. V. Reddy. “A Schmitt trigger based on DDCCCTA without any passive components”. In: *Proc. IEEE Int. Conf. Commun. Signal Process. (ICCSP)*. 2015, pp. 1695–1698. DOI: [10.1109/iccsp.2015.7322808](https://doi.org/10.1109/iccsp.2015.7322808).
- [48] A. N. Mazumder and T. Mohsenin. *A fast network exploration strategy to profile low energy consumption for keyword spotting*. 2022. arXiv: [2202.02361](https://arxiv.org/abs/2202.02361) [cs.LG].
- [49] C. Banbury et al. *MLPerf Tiny Benchmark*. 2021. arXiv: [2106.07597](https://arxiv.org/abs/2106.07597) [cs.LG].
- [50] J. Lin et al. “MCUNet: Tiny Deep Learning on IoT Devices”. In: *Advances in Neural Information Processing Systems*. Vol. 33. Virtual, 2020, pp. 11711–11722.
- [51] Y. Zhang et al. *Hello Edge: Keyword Spotting on Microcontrollers*. 2017. arXiv: [1711.07128](https://arxiv.org/abs/1711.07128) [cs.SD].