

Neuromorphic Computing and Engineering

Crossmark

PAPER

RECEIVED
30 Nov. 2025REVISED
23 Sep. 2026

A Neuromodulable Current-Mode Silicon Neuron for Robust and Adaptive Neuromorphic Systems

Loris Mendolia^{1,*}, Chenxi Wen², Elisabetta Chicca³, Giacomo Indiveri², Rodolphe Sepulchre⁴, Jean-Michel Redouté¹ and Alessio Franci^{1,5,*}¹Department of Electrical Engineering and Computer Science, University of Liège, Liège, Belgium²Institute of Neuroinformatics, University of Zurich & ETH Zurich, Zurich, Switzerland³Bio-Inspired Circuits and Systems Lab, Zernike Institute for Advanced Materials & Groningen Cognitive Systems and Materials Center, University of Groningen, Groningen, The Netherlands⁴Department of Engineering, University of Cambridge, Cambridge, U.K. & Department of Electrical Engineering, KU Leuven, Leuven, Belgium⁵WEL Research Institute, Wavre, Belgium

*Authors to whom any correspondence should be addressed.

E-mail: lmendolia@uliege.be, afranci@uliege.be**Keywords:** Neuromorphic engineering, Silicon neurons, Neuromodulation, CMOS analog circuits, Current-mode design**Abstract**

Neuromorphic engineering makes use of mixed-signal analog and digital circuits to directly emulate the computational principles of biological brains. Such electronic systems offer a high degree of adaptability, robustness, and energy efficiency across a wide range of tasks, from edge computing to robotics. Within this context, we investigate a key feature of biological neurons: their ability to carry out robust and reliable computation by adapting their input responses and spiking patterns to context through neuromodulation. Achieving analogous levels of robustness and adaptation in neuromorphic circuits through modulatory mechanisms is a largely unexplored path. We present a novel current-mode neuron design that supports robust neuromodulation with minimal model complexity, compatible with standard CMOS technologies. We first introduce a mathematical model of the circuit and provide tools to analyze and tune the neuron behavior; we then demonstrate both theoretically and experimentally the biologically plausible neuromodulation adaptation capabilities of the circuit over a wide range of parameters. All theoretical predictions were verified in experiments on a low-power 180 nm CMOS implementation of the proposed neuron circuit. Thanks to the analog underlying feedback structure, the proposed adaptive neuromodulable neuron exhibits a high degree of robustness, flexibility, and scalability across operating ranges of currents and temperatures, making it a perfect candidate for real-world neuromorphic applications.

1 Introduction

The remarkable efficiency and adaptability of the human brain emerge not only from the dynamics of spiking neurons and plastic synapses, but also from a cellular regulation mechanism known as neuromodulation [1–4]. Neuromodulators, such as dopamine and serotonin, shape neuronal behavior over timescales ranging from seconds to minutes by adjusting excitability, firing thresholds and spiking patterns, and by regulating rhythmic activity [5]. The study of the role of neuromodulation in shaping rhythmic circuits, and in particular central pattern generators (CPGs), has provided fundamental insights into how neural systems achieve quick and robust adaptability to changing environments. This ability to flexibly switch between behaviors without structural rewiring of neuronal circuits can be a powerful, yet largely unexplored source of inspiration for neuromorphic hardware design [6].

The opportunities provided by neuromodulation are illustrated in Figure 1. The top traces are physiological recordings of a neuron undergoing neuromodulation, switching between slow tonic spiking and transient bursting. The first mode supports linear rate-based encoding of the input strength, while the second allows a nonlinear detection of input changes, a "wake-up call" response.

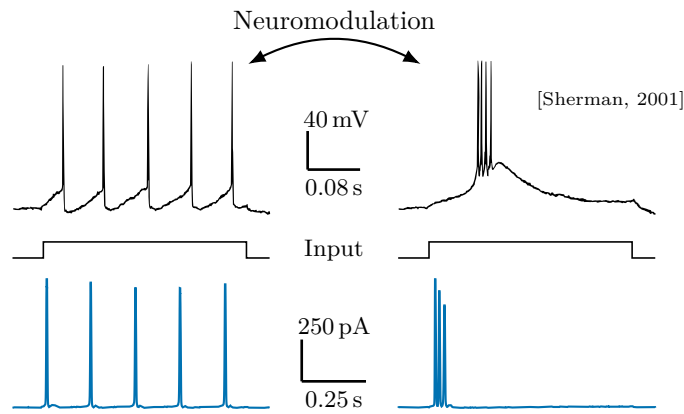


Figure 1. Neuromodulation in thalamocortical relay neurons (top, adapted from [7]) vs. neuromodulation recorded in our silicon neuron (bottom). For the same input current step (middle trace), neuromodulation enables a switch between tonic spiking (left) and a single transient burst (right), corresponding respectively to a linear rate-based encoding or a nonlinear "wake-up call" response to changes. In thalamocortical relay neurons, this response change is caused by hyperpolarization, which can be driven by neuromodulators. In our silicon neuron, the same change is obtained by varying a bias voltage. Subthreshold integration dynamics are also reproduced in our neuron, but are much faster than biological neurons due to the limited capacitor sizes.

The bottom traces show the same modulation recorded experimentally on our neuromorphic chip presented in this work, where varying a single bias voltage enables reliable behavioral switches across all neurons present on chip. Capturing such transitions in silicon not only brings us closer to the richness of biological computation but also enables a new range of possibilities for flexible and adaptive behaviors in neuromorphic systems. This example is one of many possibilities for functional switches in behaviors achievable using neuromodulation.

Neuromorphic engineering aims to replicate neural computation using analog, digital, or mixed-signal circuits that mimic the asynchronous, event-driven, and massively parallel architecture of the brain [8–13]. In the analog and mixed-signal domains, subthreshold transistor operation and current-mode designs have naturally emerged as powerful techniques for implementing power-efficient circuits emulating neuronal dynamics [10, 14]. Subthreshold circuits exploit the exponential current-voltage relationship of field-effect transistors (FETs) near the threshold voltage to generate nonlinearities at ultra-low currents, and current-mode design allows direct addition and subtraction of signals, across several orders of magnitude of current ranges despite limited voltage headrooms [8]. Most modern silicon neuron designs for large-scale analog and mixed-signal implementations are based on variations of compact integrate-and-fire (I&F) models [15, 16]. Their efficiency, robustness, and compactness make them highly scalable but come at the cost of missing most of the key dynamical features needed to emulate biological neuromodulation in silicon. More than a biological curiosity, neuromodulation is a fundamental neural mechanism for generating diverse temporal patterns, enabling context-dependent information processing, and supporting the emergence and regulation of different behavioral states. The ability to flexibly switch between dynamical regimes is crucial for functions including rhythmic pattern generation, sensory filtering, and behavioral switching [3, 5]. Reproducing it in compact, low-power neuromorphic hardware remains a challenge to date, as it involves using larger neuron models containing various nonlinear interactions between a larger number of state variables across multiple timescales. Some works have started addressing this issue [17–19], but do not achieve the level of integration and power efficiency required by large-scale integration.

Nevertheless, both neuroscience and neuromorphic computing communities increasingly recognize the computational and functional benefits of neuromodulation and more complex excitable behaviors. Bursting in particular has been shown to enhance the performance of artificial spiking neural networks in learning tasks [20–23]. Translating the robust and tunable rhythmic properties of bursting CPGs into hardware has also been the focus of several recent works [19, 24–27]. However, current large-scale analog and mixed-signal neuromorphic platforms, such as [28–30], lack native and robust support for intrinsic bursting and neuromodulation. Instead, these platforms rely on generating population-level emergent rhythms from large groups of spiking neurons or on exploiting biologically implausible dynamical features. Such strategies either lead to non-robust behaviors or resource-intensive implementations, which limits their applicability in real-world scenarios. The only exception to date is the silicon neuron presented in [19]. However, its voltage-mode design offers lower dynamic range and energy efficiency compared to current-mode

subthreshold designs.

Recently, "mixed-feedback" modeling has emerged as a promising framework to address the trade-off between biological plausibility, behavioral richness, and hardware viability. In mixed-feedback models, the complex dynamics of numerous interacting neural ionic currents are captured by the superposition of a reduced number of positive and negative feedback loops on a well-defined hierarchy of timescales [19, 31–35]. These models produce rich and robustly tunable neuronal behaviors while remaining low-dimensional and tractable. The minimality of mixed-feedback models paves the way toward plausible large-scale implementations of neuromodulable neurons and also makes them more tractable for systematic analysis and tuning, as already highlighted in [34].

In this work, we bridge the gap between the theoretical richness of mixed-feedback models and state-of-the-art analog neuromorphic circuit design. We present a fully analog mixed-feedback neuromodulable neuron implemented in current-mode subthreshold circuits [10, 36, 37]. Our design preserves the core dynamical structure of mixed-feedback models and introduces a series of practical improvements tailored to reduce power consumption and area. The resulting circuit exhibits fully modulable excitable behaviors while remaining compact and low-power. This approach lays the foundation for scalable neuromorphic systems that can exploit circuit-level neuromodulation for adaptive behavior and context-aware computation in real-world scenarios.

In Section 2, we introduce the proposed mixed-feedback neuron model and describe its implementation in subthreshold current-mode Complementary Metal-Oxide-Semiconductor (CMOS) circuits for a compact, modular, and ultra-low-power hardware realization of a neuromodulable neuron. In the model, the different timescales are continuously coupled, as opposed to being linked by events only. This subtle difference drastically enhances the expressivity of our model. We detail the use of differential-pair integrator (DPI) [38] and current-mode sigmoid blocks, including a novel biologically inspired positive feedback inactivation mechanism. We also present an analysis framework that enables prediction and tuning of the neuron's excitable behavior by connecting circuit-level tuning and model equations. In Section 3, we present experimental results obtained from a 180 nm CMOS prototype that exhibits consistent spiking, bursting, and neuromodulation capabilities. We evaluate robustness to device mismatch and show that tuning the characteristic scale of bias currents enables progressive tuning from an ultra-low-power mode to a strongly reliable mode, while maintaining subthreshold operation. We also report an energy efficiency, at room temperature and as a function of spiking frequency, of 40 to 200 pJ/spike at a 1.8 V supply, and further validate the circuit's resilience to temperature changes (5 to 45 °C). In Section 4, we compare our design with state-of-the-art bursting neuron implementations and discuss integration within larger neuromorphic systems and platforms. Since this work focuses on the design, analysis, and experimental validation of a single neuron circuit rather than a complete neuromorphic system, we frame the proposed neuron as a modular building block that can be integrated into a wide range of architectures and communication schemes, independent of a specific system-level organization. Finally, Section 5 concludes the paper and outlines future research directions.

2 The mixed-feedback neuron circuit

To capture the essential dynamics of neuronal excitability and neuromodulation and implement them efficiently in neuromorphic hardware, we adopt a mixed-feedback approach [19, 31, 32, 34, 35] that uses a superposition of positive and negative feedbacks across distinct timescales. In contrast to the few existing mixed-feedback neuron implementations [19, 34], we propose a mixed-feedback architecture using current-mode circuits, ensuring more compact, robust, and energy-efficient designs [10]. All state variables, such as the neuron's membrane "potential" and the positive and negative feedback terms, are therefore represented as physical currents. This choice naturally supports the modularity of the feedback design by exploiting Kirchhoff's current law to implement sum and difference operations. It also ensures compatibility with ultra-low-power subthreshold CMOS circuits, even in technology nodes characterized by limited voltage headroom [36, 37].

This section introduces the structure of our mixed-feedback neuron model and its specificities, details its implementation using subthreshold current-mode CMOS circuits, and presents a mathematical formulation for the analysis and tuning of the circuit.

2.1 A current-mode mixed-feedback neuron model

The design of a mixed-feedback architecture requires two building blocks: first-order low-pass filters and static sigmoidal functions.

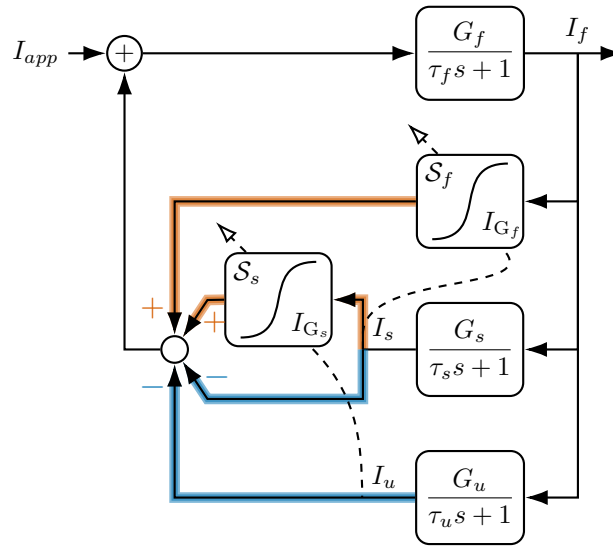


Figure 2. Mixed-feedback neuromodulable neuron structure. Red (*resp.* blue) highlighted arrows indicate positive (*resp.* negative) feedback paths. The two types of blocks use the notations introduced in Eqs. (1) and (3): the low-pass filter blocks are denoted using their transfer function, and the sigmoid blocks using their symbol, their gain variable, and the shape of their steady-state response. The dashed arrows indicate positive feedback inactivation described by Eq. (4), they represent a modulation of the indicated gain parameter of the sigmoids they traverse. I_f is the current-mode analog of the membrane potential. I_s and I_u respectively provide slow repolarization and ultraslow spike-frequency adaptation currents. The nonlinear sigmoid blocks provide positive feedback that creates the fast spike upstroke and slow regenerative dynamics.

A first order current-mode low-pass filter, with input I_{in} and output I_{out} , is described in state-space representation as

$$\tau \frac{dI_{\text{out}}}{dt} = -I_{\text{out}} + GI_{\text{in}}, \quad (1)$$

where τ is the time constant of the filter and G its gain. In the Laplace domain, (1) is represented by the transfer function

$$\frac{I_{\text{out}}}{I_{\text{in}}} = H(s) = \frac{G}{\tau s + 1}, \quad (2)$$

with s the complex variable of the Laplace domain. Low-pass filters serve two complementary purposes in the mixed-feedback architecture. First, they enable the accumulation and integration of signals over time. Second, they create well-separated time constants for different feedback pathways, reflecting the variety of timescales observed in neural ion channel kinetics [39].

We denote static sigmoidal current-mode input-output characteristics as

$$I_{\text{out}} = \mathcal{S}(I_{\text{in}}; I_{\text{G}}), \quad (3)$$

where I_G is the sigmoid gain. Such sigmoidal nonlinearities serve as a minimal model of neural ionic currents with gated and bounded conductances. These nonlinear functions introduce thresholding and saturation, which are key to creating the rich and tunable neuronal responses of mixed-feedback models. Examples of such current-mode sigmoidal functions will be shown in Fig. 6. Importantly, the combination of saturating nonlinearities and separated time constants enables excitable feedback dynamics that are expressive, robust, and tunable through a small number of parameters, allowing the neuron to exhibit qualitatively distinct firing regimes under different neuromodulation settings.

Using these two building blocks, our mixed-feedback neuron combines nonlinear feedback pathways across multiple timescales into a compact dynamical system. The resulting structure, implemented exclusively with current-mode low-pass filters and sigmoidal nonlinearities, is represented in Fig. 2. The internal dynamics of the model are organized around three sharply distinct timescales (fast, slow, and ultraslow) defined by the time constants of three low-pass filters, two linear negative feedback loops (highlighted in blue), and two nonlinear positive feedback loops (highlighted in orange). The circuit implementations of both types of blocks will be discussed in Section 2.2.

The fast low-pass filter acts as a leaky integrator and models the passive membrane dynamics of the neuron. Its output, the current I_f , serves as a current-mode analog of the neuron's membrane

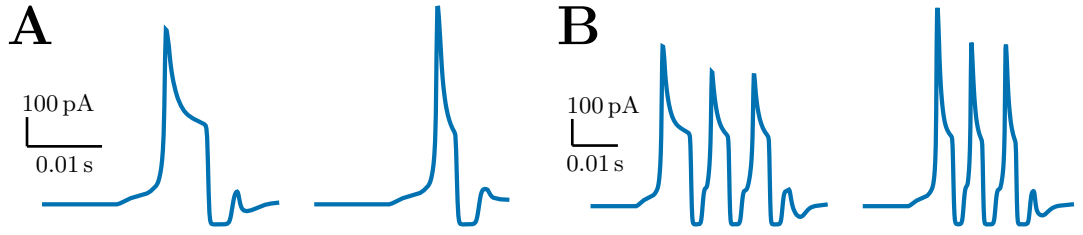


Figure 3. Spike (A) and burst (B) with (right) and without (left) positive feedback inactivation. The temporal extent of spikes and bursts is reduced thanks to the inactivation, but they remain long enough in time to directly signal to physical systems (in the spirit of [42]).

potential. It receives the external inputs to the neuron I_{app} and integrates the effects of all the feedback loops, including the positive self-feedback loop through $\mathcal{S}_f$. The two other low-pass filters define the slow and ultraslow current-mode state variables I_s and I_u . I_s provides both linear slow negative feedback and nonlinear slow positive feedback, through $\mathcal{S}_s$, on the membrane potential I_f , while I_u provides ultra-slow negative feedback. These feedback pathways correspond to those provided by ionic current on membrane potential variations in biological neurons [31, 32, 39–41]: the fast positive feedback mimics the rapid activation of sodium channels responsible for spike initiation; the slow positive feedback simulates low-threshold calcium currents that support bursting or regenerative depolarization; the slow and ultraslow negative feedbacks capture delayed-rectifier and calcium-activated potassium currents responsible for spike repolarization, spike-frequency adaptation, and burst termination.

Besides its current-mode nature, our neuron design departs from [19, 34] in two other fundamental aspects. First, the negative feedback loops in the proposed mixed-feedback architecture are linear, removing additional gating and saturating sigmoidal blocks. This simplification reduces circuit complexity, area, and power consumption, while minimally affecting robustness and tunability. Indeed, negative feedback enforces stability and adaptation, whereas regime selection and neuromodulation are governed by the nonlinear positive feedback pathways. This design choice preserves the qualitative shape of the steady-state characteristics that determine firing regimes, as confirmed by the steady-state curves reported later in Section 2.3. Second, inspired by ionic current inactivation kinetics in biological neurons [39, 40, 43], our model includes a positive feedback inactivation mechanism that promotes shorter and more power-efficient spikes. In practice, the gains of the fast and slow positive feedbacks are modulated by subtracting the slow I_s and ultraslow I_u currents from the fast $I_{G_f,0}$ and slow $I_{G_s,0}$ sigmoid gains, respectively. The resulting modulated sigmoid gains $I_{G_f}(t)$ and $I_{G_s}(t)$ are defined as

$$I_{G_f}(t) = I_{G_f,0} - I_s(t), \quad (4a)$$

$$I_{G_s}(t) = I_{G_s,0} - I_u(t). \quad (4b)$$

Because the fast dynamics are assumed to be much faster than the slower ones, the multiplicative interactions created by positive feedback inactivation have a negligible impact on spike initiation but become significant during repolarization. By attenuating positive feedback right after a spike is generated, it shortens spike duration, lowering per-spike power consumption and making spike events more localized in time, without interfering with the underlying excitability and modulation properties. The effect of positive feedback inactivation is illustrated in Fig. 3, which compares simulations of spiking and bursting traces with and without inactivation.

These waveforms illustrate a full spike or burst cycle, including an input integration phase, a rapid depolarization driven by the nonlinear positive feedback, followed by repolarization mediated by the slower negative feedback pathways implemented through the low-pass filters. The fast timescale governs spike onset, while the slow and ultraslow dynamics progressively suppress the positive feedback, bringing the neuron back to its resting state and enforcing a refractory period. For bursting, the slow positive feedback enables new spikes after repolarization, before the ultraslow negative feedback suppresses the activity entirely, ending the burst.

2.2 Implementation of current-mode circuit blocks

To implement current-mode low-pass filters, we use the differential-pair integrator (DPI) circuit [38] shown in Fig. 4. The DPI has become a staple in analog and mixed-signal neuromorphic systems due to its compact design, low-power operation, and tunable gain and timescale.

Under the assumptions of subthreshold operation, and provided that the input current exceeds the leakage current ($I_{in} > I_\tau$), so that the output current will eventually dominate the threshold

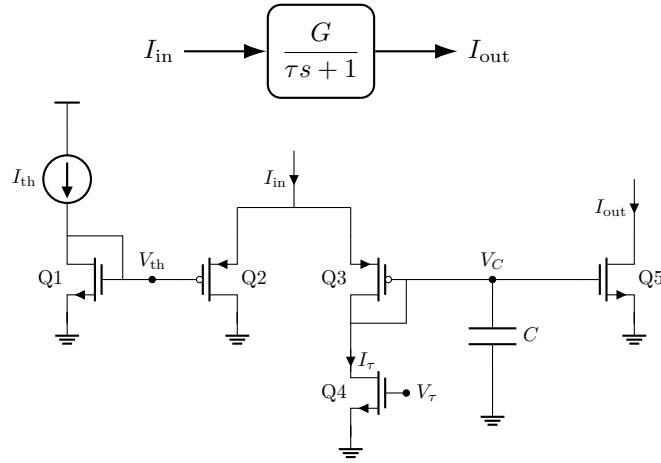


Figure 4. Differential-pair integrator (DPI) circuit (from [10, 38, 44, 45]), tunable via its two bias voltages V_{th} and V_{τ} . Q2-3 are the differential pair receiving the input current I_{in} . With Q1, Q2 sets the gain $G = \frac{I_{th}}{I_{\tau}}$ of the circuit by diverting part of the input current depending on I_{th} , while Q3 sets the voltage V_C of the capacitor. Q4 provides the leakage current I_{τ} that discharges the capacitor over time. Q5 provides an output current I_{out} depending on the capacitor voltage V_C .

current ($I_{out} \gg I_{th}$), its dynamics can be approximated by those of a first-order low-pass filter, as expressed in (1), with a gain $G = \frac{I_{th}}{I_{\tau}}$ and a time constant $\tau = \frac{CU_T}{\kappa I_{\tau}}$, where $I_{\tau} = I_0 e^{\frac{\kappa V_{\tau}}{U_T}}$, with I_0 the transistor leakage current, κ the subthreshold slope factor, and U_T the thermal voltage [45]. Both G and τ are tunable via the two bias voltages V_{th} and V_{τ} .

The mixed-feedback model relies on a strong separation between the different timescales to justify the quasi steady-state approximation that supports its theoretical structure (Section 2.3). In hardware, this translates into DPI filters with time constants spanning multiple orders of magnitude, implemented here through scaling of the capacitor sizes. In our circuit, we used capacitors ranging from hundreds of fF for the fast timescale to several pF for the ultraslow one, as reported in Table 2. Capacitor sizes increase by a factor of 4 between each timescale, setting the basis to achieve the desired timescale separation. Indeed, considering a leakage current $I_{\tau} = 2$ pA, which is achievable in mature CMOS nodes, one obtains $\tau_f = 9$ ms, $\tau_s = 35$ ms, and $\tau_u = 143$ ms at room temperature using the expression for τ reported above. This range is consistent with the fast, slow, and ultraslow dynamics of spiking and bursting in cortical neurons [7], as illustrated in Fig. 1, and provides a sufficient timescale separation to ensure proper circuit operation. If desired, the leakage currents of the individual DPIs may be further adjusted to accentuate the differences between timescales. As will be discussed later in Section 4.1, these capacitors occupy most of the neuron's area on chip, representing the main physical cost of faithfully implementing biologically plausible timescales.

The two nonlinear sigmoids $\mathcal{S}_f(I_f; I_{G_f})$ and $\mathcal{S}_s(I_s; I_{G_s})$ in the neuron model are implemented using a custom current-mode subthreshold circuit, shown in Fig. 5. This design combines a simple comparator with diode-connected transistors and a gain branch to produce a fully tunable sigmoidal current-to-current relationship. Three bias voltages (associated with bias currents through the standard subthreshold equation of NFETs in the saturation regime $I_b = I_0 e^{\frac{\kappa V_b}{U_T}}$) independently provide full control over the sigmoid input-output characteristic. V_{thr} sets the input threshold current I_{thr} at which the circuit starts to output current; V_{lin} controls the size of the input current range over which the sigmoidal output is monotonically increasing and roughly linear; and V_G sets the maximum output current I_G . The effect of these three bias currents is illustrated in Fig. 6. The result is a compact, low-power, and easily tunable current-mode sigmoid function, well-suited for designing neuromorphic circuits with nonlinear feedback dynamics. Mathematical developments proving the sigmoidal shape of the input-output relationship of the circuit are provided in Appendix C.

The circuit shown in Fig. 5 also includes a gain modulation subcircuit that implements the positive feedback inactivation dynamics described in Section 2.1. The inactivation current I_{mod} is subtracted from the baseline gain current $I_{G,0}$ using current mirrors, such that the effective gain bias voltage V_G fed to the sigmoid gain branch produces a gain current $I_G(t) = I_{G,0} - I_{mod}(t)$.

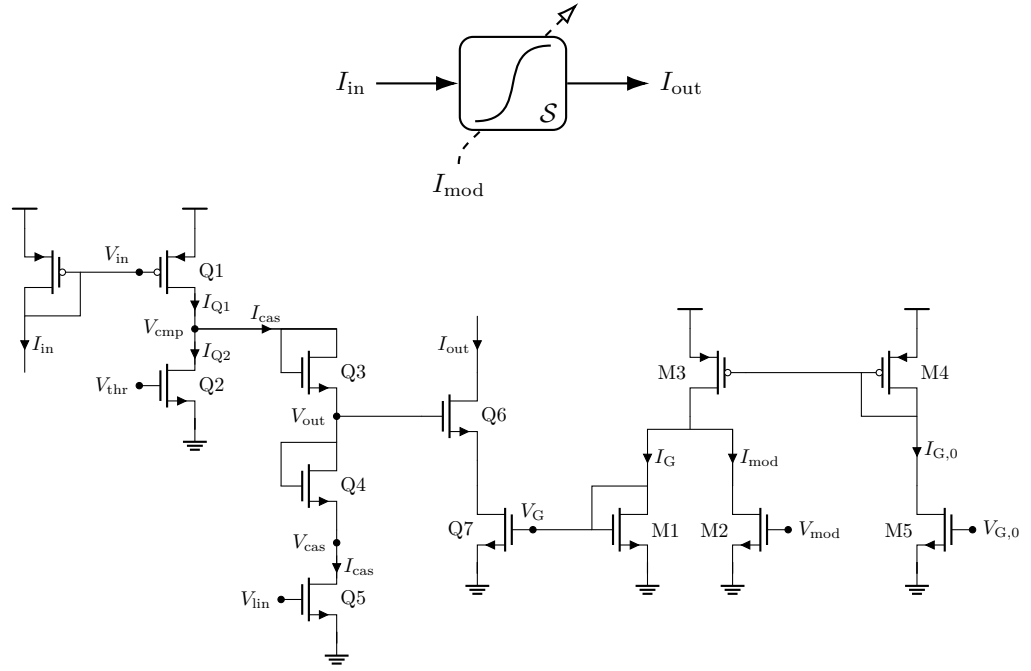


Figure 5. Current-mode sigmoid circuit with inactivation mechanism. The three bias voltages V_{thr} , V_{lin} and $V_{G,0}$ are assumed to be obtained through NMOS current mirrors and linked to the bias current parameters I_{thr} , I_{lin} and $I_{G,0}$ through $I_b = I_0 \exp\left(\frac{\kappa V_b}{U_T}\right)$. Q1-2 form a simple current comparator circuit: when $I_{in} > I_{thr}$, the voltage V_{cmp} starts to increase. Q3-5 control the rate of increase of V_{cmp} : the higher V_{lin} is, the more current is drawn by this branch, increasing the response range of the comparator. Q6-7 set the gain of the circuit, defining the maximum output current I_G at which the sigmoid saturates. The role of M1-5 is to implement the inactivation mechanism by subtracting I_{mod} from the parameter $\hat{I}_{gain}$.

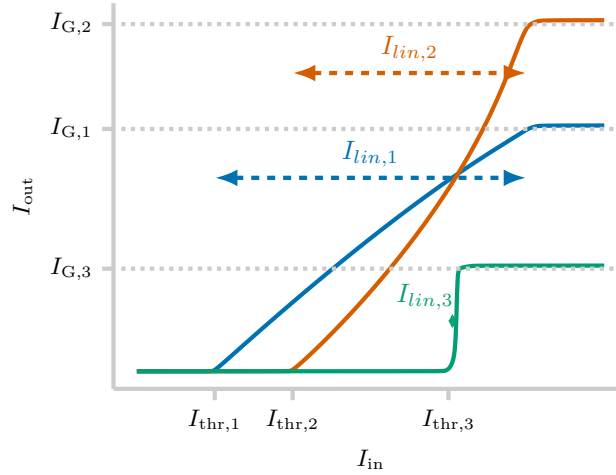


Figure 6. Current-mode sigmoid circuit response for different bias parameter values. The bias currents I_{thr} , I_{lin} , and I_G accurately set the input threshold, the width of the monotonically increasing range, and the maximum output current respectively, for any combination of subthreshold bias parameters.

Using the DPI and sigmoid circuits, the entire mixed-feedback model presented in Fig. 2 can be implemented with only two different analog blocks, as shown in the full circuit schematic in Fig. 14, simplifying not only tuning but also chip design and layout. This modularity is a key strength of the approach: each feedback loop is implemented using the same circuit templates, with the resulting feedback behavior controlled entirely through the 12 bias currents (3 for each of the 2 sigmoids, and 2 for each of the 3 DPIs). The use of subthreshold current-mode design further ensures ultra-low-power operation, making the neuron well-suited for large-scale deployment in power-constrained neuromorphic systems. Moreover, this neuron can easily be interfaced with modern event-based communication schemes such as Address Event Representation (AER) to enable large-scale communication. Input current can be directly provided by DPI synapses, while spike events can be extracted from the fast sigmoidal output node V_{S_f} and converted into digital

pulses, creating a natural separation between continuous-time internal dynamics and spike signaling.

Current-scale invariance Because all state variables are currents and interact through linear DPI filters and current-mode summation, the model dynamics are invariant under uniform scaling of the bias currents, provided the system operates in the subthreshold, or weak inversion, regime where the drain current exhibits an exponential dependence on gate voltage. This region is usually defined by $V_{GS} - V_{th} \leq 3$ to $4 U_T$, where the threshold voltage V_{th} is technology-dependent [46]. In this regime, a uniform scaling of all biases indeed preserves the relative strength of the positive and negative feedback pathways, as justified in Section 2.3.

In our 180 nm technology, the neuron maintains its qualitative dynamical behavior up to bias currents of approximately 7 μA (for the fast sigmoid gain $I_{G,0f}$). Beyond this point, a departure from the predicted scale invariance is observed as devices enter moderate inversion and the subthreshold assumptions behind the derivation of the DPI dynamics (1), which justify the operation of the mixed-feedback model in Section 2.3, are no longer met. Increasing the operating current within the subthreshold limits reduces mismatch sensitivity (as shown later in Section 3.2.4) at the expense of higher power consumption, while lower currents favor ultra-low-power operation. The lower bound for operating currents is thus set by the acceptable level of variability for a given application, down to typical transistor leakage currents of the technology. This flexibility makes the approach suitable for both energy-constrained systems and performance-critical scenarios.

Temperature invariance Similar arguments as for the current-scale invariance apply when considering temperature variations. Because the subthreshold currents scale with temperature, all feedback loop currents and time constants change proportionally, preserving their relative ratios. Consequently, the neuron dynamics remain qualitatively invariant, with temperature primarily rescaling the temporal evolution. This proportional scaling accounts for the temperature invariance experimentally observed in Fig. 13.

2.3 Model tuning and theoretical analysis

To capture the continuous-time dynamics of our mixed-feedback neuron, we can leverage the structure of the model and write the input-output relationship of each low-pass filter, which yields

$$\tau_f \dot{I}_f = -I_f + G_f (\mathcal{S}_f(I_f; I_{G_f}) + \mathcal{S}_s(I_s; I_{G_s}) - I_s - I_u + I_{app}) , \quad (5a)$$

$$\tau_s \dot{I}_s = -I_s + G_s I_f , \quad (5b)$$

$$\tau_u \dot{I}_u = -I_u + G_u I_f . \quad (5c)$$

These equations enable the use of the techniques introduced in [31, 32] for biophysical conductance-based models and in [34] for voltage-mode mixed-feedback circuits to analyze the emergence of spiking and bursting behaviors from the interaction of the different feedback loops in this continuous mixed-feedback model. They provide a fast and systematic way of tuning the various parameters of the model by revealing the excitability thresholds and bistable regions, allowing to skip lengthy transient simulations and tune bias voltages solely based on DC characteristics of the feedback loops.

To illustrate these techniques, we compute the steady-state "output-input" curves used in [19, 34] of the three feedback loops. These curves are conceptually similar to the I-V (current-voltage) curves measured using voltage clamp experiments in neuroscience. To that end, we assume timescale separation, that is, $\tau_f \ll \tau_s \ll \tau_u$, and neglect the effect of positive feedback inactivation. This is a reasonable assumption since the fast (*resp.* slow) inactivation depends on the slow (*resp.* ultraslow) variable, which is negligible in the timescale of interest through a quasi steady-state approximation enabled by the different capacitor sizes described in Section 2.2. We also set $G_f = G_s = G_u = 1$, so that the DPI circuits behave like linear leaky integrators. We can derive the expression of the three steady-state characteristics by sequentially setting the derivatives in Eq. (5) to zero, starting from the fastest subsystem and neglecting the effect of slower variables, to obtain

$$\dot{I}_f = 0 \Leftrightarrow I_{app} = \bar{I}_f - \mathcal{S}_f(\bar{I}_f; \bar{I}_{G_f}) , \quad (6a)$$

$$\dot{I}_f, \dot{I}_s = 0 \Leftrightarrow I_{app} = 2\bar{I}_s - \mathcal{S}_f(\bar{I}_s; \bar{I}_{G_f}) - \mathcal{S}_s(\bar{I}_s; \bar{I}_{G_s}) , \quad (6b)$$

$$\dot{I}_f, \dot{I}_s, \dot{I}_u = 0 \Leftrightarrow I_{app} = 3\bar{I}_u - \mathcal{S}_f(\bar{I}_u; \bar{I}_{G_f}) - \mathcal{S}_s(\bar{I}_u; \bar{I}_{G_s}) . \quad (6c)$$

Examples of these curves and the resulting simulated neuron activity are shown in Fig. 7. The slope of these curves indicates the stability of the corresponding equilibria: regions of positive

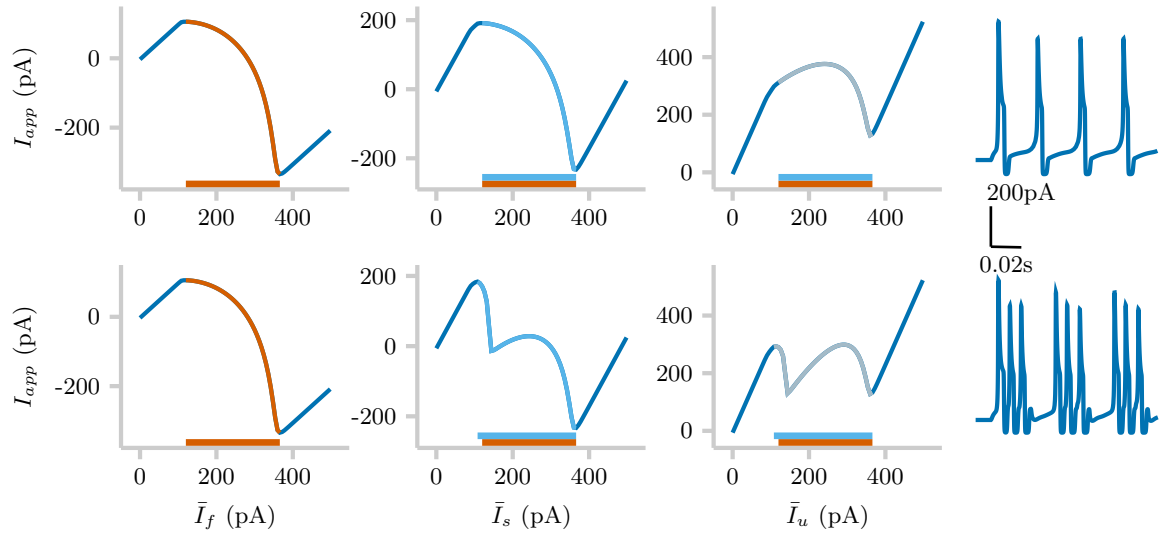


Figure 7. Examples of steady-state curves (left) of our mixed-feedback model and the corresponding neuron responses (right), using the parameters of Table 3. The red (*resp.* cyan) regions are the bistability region of the fast (*resp.* slow) subsystems. When the slow bistability region is entirely contained within the fast one (top), the neuron can only exhibit tonic spiking. When the slow bistability region threshold comes before the fast one (bottom), the neuron becomes capable of bursting. The y-axis of the ultraslow curve indicates which input current will put the neuron in a certain region.

(negative) slope correspond to stable (unstable) equilibria. By comparing the relative positions of the fast, slow, and ultraslow bistability thresholds (corresponding to the maxima and minima), one can immediately infer whether the neuron will exhibit tonic spiking, bursting, or purely passive behavior. A region of negative slope in the fast steady-state curve translates to the existence of positive feedback, responsible for spike initiation. If a bistability threshold appears in the slow steady-state curve before the fast one, it shows a bistability between tonic spiking and silence, from which bursting can arise when an ultraslow variable slowly drives the system across this bistable region. A monotonically increasing ultraslow steady-state curve guarantees that, at the slowest timescale, the system is monotonically stable, ensuring that it will go back to rest after a spike or a burst [34].

This geometric interpretation provides a powerful visual tool for understanding how feedback interactions and timescale separation generate complex dynamics. Moreover, these steady-state curves only depend on $\mathcal{S}_f$ and $\mathcal{S}_s$ and can therefore be analyzed by simply simulating the DC characteristics of the two sigmoid circuits.

This analysis also predicts the scaling properties of the model. Because all state variables and parameters are currents and interact through linear current-mode filters, the relative threshold positions remain invariant under uniform scaling of the bias currents, explaining the current and temperature invariance discussed in Section 2.2. These invariance properties, intrinsic to the mixed-feedback current-mode formulation, contribute to the robustness of the proposed neuromorphic architecture.

3 Experimental results

To validate the proposed mixed-feedback neuron architecture and its current-mode implementation, we fabricated and experimentally characterized the silicon neuron under various operating conditions. This section demonstrates that the fabricated circuit reproduces the key behaviors predicted by the model, including spiking and bursting dynamics, robust neuromodulation, low-power operation, and temperature invariance. We first describe the experimental setup and measurement methodology, followed by an analysis of the basic excitability and modulation properties. Specifically, we demonstrate the emergence of bursting through tuning of a single parameter and highlight the relationship between input strength and firing frequency, both for slow (Type-I) tonic spiking and tonic bursting. We then report power consumption simulations for different firing patterns and frequencies. We also provide Monte Carlo mismatch simulations, showing a tradeoff between energy efficiency and robustness comparable to the state-of-the-art. Finally, we present the results of a temperature variation experiment, showing how our mixed-feedback neuron behaves at various operating temperatures. All measurements focus on neuron-level behavior and metrics, independently of a specific neuromorphic system or application.

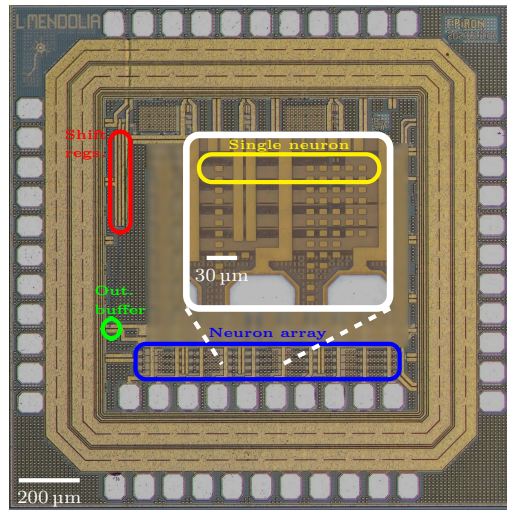


Figure 8. Micrograph of the prototype chip (2023) containing the test mixed-feedback neurons. Blue: array of the 16 mixed-feedback neurons. Green: output buffer stage. Red: shift registers. Inset: zoom on 4 mixed-feedback neurons stacked on top of one another. Yellow: a single neuron. Circuits unrelated to this work are blurred.

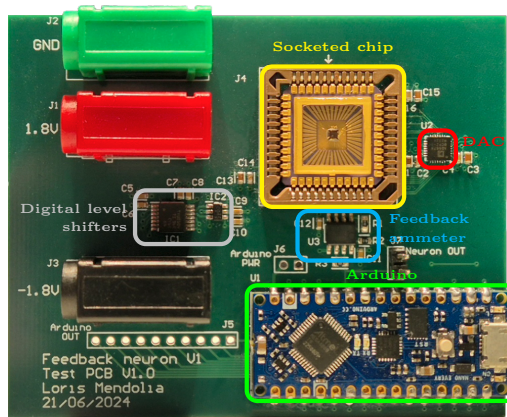


Figure 9. Custom PCB used for characterization of the on-chip mixed-feedback neurons. The board hosts the fabricated CMOS die (center, yellow), an external 12-bit DAC (AD5674, red) for bias generation, and an operational amplifier configured as a feedback ammeter (blue) for on-board current-to-voltage conversion. A microcontroller (Arduino Nano Every, green) controls the on-chip multiplexer for output selection and programming of the DAC for bias generation. Output signals were acquired with an oscilloscope (Analog Discovery 3) for data acquisition.

3.1 Experimental setup

An array of 16 mixed-feedback neurons was fabricated on a test chip shared among different projects in a 180 nm CMOS X-FAB process. An active area of $750 \times 90 \mu\text{m}^2$ was dedicated to this end. A micrograph of the fabricated chip is shown in Fig. 8, highlighting the neuron array, control logic, and output. All neurons share a common set of 12 bias voltages (for the 2 sigmoids and 3 DPIs), generated by an external DAC (an Analog Devices AD5674 12-bit, 16-channel digital-to-analog converter (DAC)). A single analog output is provided through a transmission gate multiplexer, controlled by on-chip shift registers. The transmission gates allow the connection of one of the three internal currents (I_f , I_s , or I_u) of one neuron at a time to an output buffer stage, injecting an amplified analog copy of the selected current directly to the output pad, ensuring a reliable off-chip readout of the pA or nA internal currents.

The output current is converted into a voltage on the test printed circuit board (PCB) shown in Fig. 9 using a precision operational amplifier in feedback ammeter configuration. This configuration allows to easily achieve different gains as required. After a second amplification stage using an inverting amplifier, the resulting voltage is measured by a digital oscilloscope (Digilent Analog Discovery 3, 14-bit resolution at up to 125 MS/s, 30 MHz bandwidth), enabling a highly accurate acquisition of the neural traces. An Arduino Nano Every is mounted on the PCB to configure the shift registers and the DAC, and can optionally stream output data. All results presented here were acquired using the oscilloscope for improved accuracy and flexibility. Unless otherwise stated, all measurements were performed at room temperature and at the nominal supply voltage of 1.8 V.

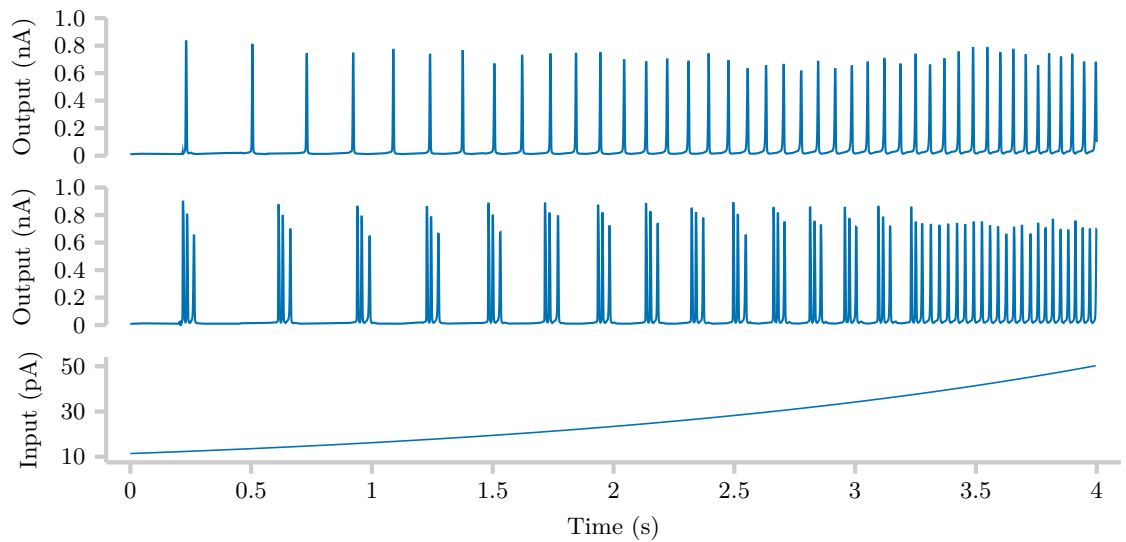


Figure 10. Measured neuron responses to increasing input current (bottom), in spiking (top) and bursting (middle) configurations. The neuron exhibits tonic excitability, showing firing frequencies increasing with input current in both modes, starting as low as a few Hz.

3.2 Measured dynamics in silicon

To validate and characterize the behavior of our neuron in silicon, we performed various measurements on the fabricated test chip. These experiments aim to confirm the neuron’s ability to robustly produce and switch between different firing regimes as predicted by the model’s mixed-feedback theoretical analysis. Extensive experimental exploration was performed, with several experimental runs on different days, different neurons, and different bias baselines to ensure the consistency of qualitative results. In addition, simulated power consumption metrics are reported to benchmark energy per spike in spiking and bursting regimes and to quantify the baseline power draw at rest. The experimental results presented in this section focus on the qualitative behavior of individual neurons. To complement these measurements, robustness to device mismatch is evaluated through Monte Carlo simulations based on a revised design incorporating mismatch-aware sizing and layout. An experimental characterization of variability is also reported in Appendix D.

3.2.1 Response to exogenous input currents Figure 10 shows the response of an on-chip neuron to an increasing input current. Both in tonic spiking (top) and bursting (middle) regimes, the neuron exhibits a consistent increase in firing activity with the input, as expected from the mixed-feedback model. Despite the different internal dynamics, in both configurations the neuron responds in a consistent and reproducible way. In line with biological neurons, the spiking and bursting frequency of our neuron increases in response to an increasing exogenous input. In bursting regime and for sufficiently large applied currents, the bursts eventually overlap, and the neuron transitions from bursting to fast spiking, once again in line with biological neurons.

3.2.2 Response to neuromodulatory inputs Figure 11 demonstrates the neuromodulation capabilities of the fabricated neuron by varying the slow positive feedback gain I_{G_s} while keeping the input current constant. As the neuromodulation parameter is incrementally increased, the neuron smoothly transitions from a tonic spiking to a tonic bursting regime, with progressively longer burst durations and more spikes per burst. These measurements illustrate how neuromodulatory tuning of a single bias current enables a smooth and predictable transition between firing regimes. Bursting characteristics, such as interburst period or spikes per burst, are directly and predictably modulated through I_{G_s} .

The observed neuromodulation dynamics are consistent with the theory of slow positive feedback: increasing the slow gain increases the slow current’s contribution to spike and burst excitability without interfering with the fast positive feedback responsible for the spike generation itself. The neuromodulatory transition achieved here is analogous to those observed in biophysical conductance models by increasing the maximal conductance of slow regenerative ionic currents, which create slow positive feedback on membrane potential variations [31, 32, 47].

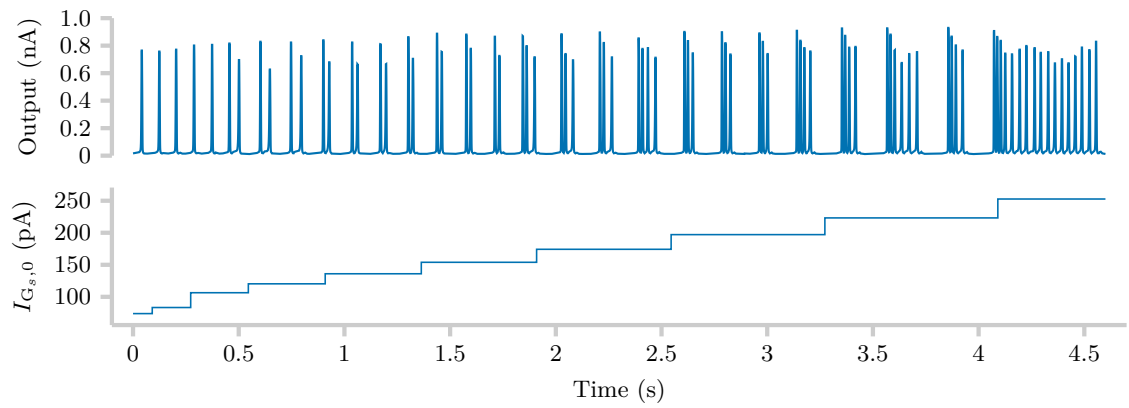


Figure 11. Measured neuromodulation from spiking to bursting (top) through an increase in slow positive feedback $I_{G_{s,0}}$ (bottom). The neuron undergoes a smooth transition from spiking to bursting, with a gradual increase in the number of spikes per burst and a consistent inter-burst interval.

Together, the measurements presented in Figs. 10 and 11 establish the neuron’s ability to reliably operate in both tonic spiking and bursting modes, with tunable transitions between the two. Our hardware neuron exhibits tunable excitability across a wide input dynamic range, with interpretable and reliable spiking mode control via specific bias currents. The control of bursting through a single (slow positive feedback) bias illustrated here is only one out of the many neuromodulatory pathways that can be explored and achieved in the proposed current-mode neuromorphic design.

As already remarked in Section 2.3, the neuron dynamics are preserved under a uniform scaling of all bias currents. This is a direct consequence of the current-mode mixed-feedback implementation: as long as the system remains in subthreshold and steady-state relationships are preserved, all time constants and feedback loops scale proportionally with bias currents. As a result, operating the neuron at 100 pA or 100 nA yields the same qualitative behaviors, from tonic spiking to bursting, with a tunable trade-off between energy efficiency and mismatch sensitivity.

3.2.3 Simulated power consumption SPICE simulations were used to estimate the power consumption of our neuron (based on a revised layout and transistor sizing reported in Table 2 optimized for mismatch, relative to the version implemented in the first test chip). The reported metrics exclude bias generation, digital control, and output circuitry, and focus solely on the neuron circuit described in Section 2. Due to the shared nature of the test chip presented in the rest of this section, experimental validation of the metrics reported here is not possible, but will be the subject of future works. Under the same bias conditions used throughout the measurements in this section, a neuron consumes approximately 3 nW at rest (zero input), with instantaneous power momentarily rising to 10 nW during spike generation.

In Type-I tonic spiking at 23 Hz, the dissipation over a half-second window of continuous analog activity, including input integration, spike generation, frequency adaptation, and other subthreshold dynamics, is 217 pJ/spike. After modulation to reach tonic bursting with 3 spikes per burst at 18 bursts per second, the average dissipation drops to 90 pJ/spike. As the tonic spiking frequency is increased, the dissipation drops down to 101 pJ/spike at 50 Hz, and 41 pJ/spike at 160 Hz. These results highlight the neuron’s low-power operation across multiple dynamical states, with increasing energy efficiency at higher spiking rates. As these energy per spike metrics pertain to complex, continuous-time, yet temporally sparse fully analog events, they must be distinguished from the fundamentally different dense, clock-driven “per MAC (Multiply-Accumulate)” benchmarks used in the digital accelerator hardware literature, where energy consumptions of < 1 pJ/MAC are frequently reported [48].

3.2.4 Statistical variability and mismatch The initial prototype presented in this work focused on validating the mixed-feedback architecture and its dynamical properties. In a revised implementation, transistor sizing was optimized through statistical simulations, and systematic mismatch-aware layout techniques, such as common-centroid placement and use of dummy transistors, were incorporated. Transistor sizings are reported in Appendix A and Table 2, and experimental population-level measurements obtained from both implementations are reported in

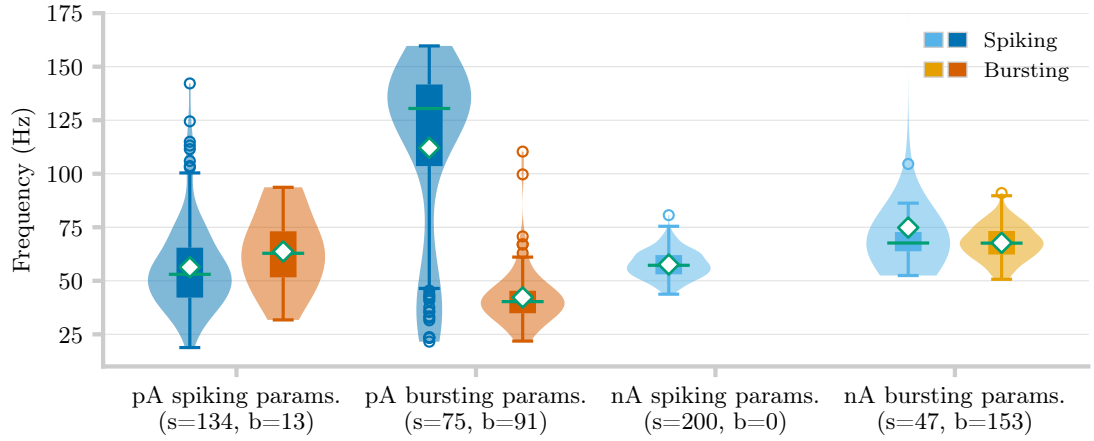


Figure 12. Monte Carlo mismatch analysis ($N = 200$) results of nominal spiking and bursting configurations biased in the picoampere range (Table 3) and after $1000\times$ uniform bias scaling to the nanoampere range. Violin plots depict the kernel density of the frequency distribution for spiking and bursting neurons. The green bar marks the median, the diamond indicates the mean, the box spans the interquartile range (IQR) (Q1-Q3), and the whiskers extend to $1.5 \times \text{IQR}$, setting the bounds for outliers shown as hollow circles. At ultra-low currents, mismatch leads to regime mixing and larger frequency variability. Increasing bias currents restores full yield and reduces frequency dispersion.

Appendix D. To further assess the expected variability in the optimized design, we performed Monte Carlo mismatch simulations of the neuron using foundry-provided models with 200 points under constant input for nominal spiking and bursting parameter sets in the picoampere regime (reported in Table 3). We then repeated the same simulations after uniformly scaling all bias currents by $1000\times$ into the nanoampere range and adjusting the input current to obtain comparable firing frequencies. Fig. 12 shows the resulting distributions of spiking and bursting (interburst) frequencies (measured as the inverse of the period between the start of two bursts).

In the picoampere regime, the yield (number of neurons tonic firing) is between 75 and 80%. For nominal spiking parameters, a few neurons transition to bursting, and firing frequency exhibits a coefficient of variation (CV) of 36%. For nominal bursting parameters, about half of the neurons maintain bursting behavior, while the remaining active neurons predominantly transition to high frequency spiking. In that case, the CV of firing frequencies is 31% for bursting neurons and 38% for spiking ones.

Scaling up the bias currents to the nanoampere range drastically improves reliability to mismatch. Yield improves to 100% in both cases, and, in the spiking case, all neurons remain in the correct regime with a frequency dispersion of 11%. Although 23% of bursting neurons transition to slow tonic spiking under mismatch, average spiking and interburst frequencies are comparable and exhibit a dispersion of 11% in bursting and 9% in spiking (excluding 3 outliers), showing that the underlying timescale structure is better preserved. These figures are close to state-of-the-art current-mode neurons such as [36]. The measured I-F characteristics in fabricated neurons using the revised layout and the same nanoampere bias currents, reported in Appendix D, also exhibit good agreement across neurons. All measured neurons remained in the intended spiking regime, with an average firing rate CV of 24%.

These results reveal a clear tradeoff between energy efficiency and robustness to device mismatch. Ultra-low current operation maximizes energy efficiency but increases sensitivity to device variability, whereas current scaling, enabled by the current scale invariance property (Section 2.2), improves regime stability and frequency reproducibility at the cost of increased power consumption. A sensitivity analysis of the simulations shows that the current mirrors formed by M_f1 and S_f7 (modulated fast positive feedback gain), $Q4$ and D_u4 (ultraslow negative feedback), and transistor S_s2 (slow positive feedback threshold) have the largest mismatch contribution to frequency variation and require the most attention during layout.

3.3 Stability of the mixed-feedback model over time and temperature

To assess the robustness of our mixed-feedback neuron to environmental variations, we characterized the test chip's response across a wide temperature range using a climatic chamber. Proper measures were taken to ensure temperature stabilization with a thermal camera and to stay within the operating temperature range of the DAC used to generate bias voltages, also monitored throughout the experiment to ensure they remained constant.

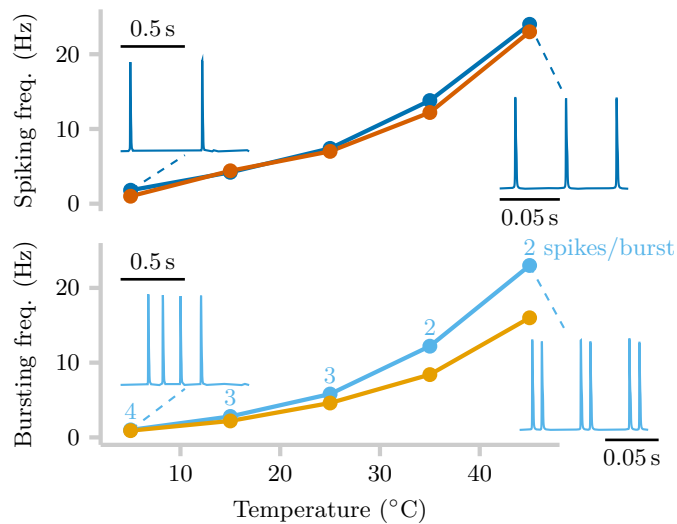


Figure 13. Measured variation in spiking (top) and bursting frequency (inverse of the period between the start of two bursts, bottom) of two different neurons as a function of ambient temperature, with representative output traces at two extreme temperatures. Numbers above the bursting data points indicate the number of spikes per burst. Frequency increases with temperature and follows a comparable trajectory across neurons and firing regimes. The recorded waveforms compress in time and speed up but remain in the same qualitative firing regime, confirming temperature-robust dynamics. The bursting neuron goes from 4-spike bursts at 5 °C to 2-spike bursts at 45 °C due to the accelerated ultraslow negative feedback dynamics.

Fig. 13 reports the evolution of the spiking and bursting (interburst) frequency of two representative neurons with temperature. In both cases, frequency increases gradually with temperature, but the overall spiking and bursting behaviors remain stable and qualitatively unchanged. The neuron responses at higher temperatures effectively correspond to sped-up or time-compressed versions of those at lower temperatures, a behavior analogous to the temperature robustness observed in biological neurons of species that experience large temperature variations, such as crabs [49, 50]. This observation further emphasizes the biophysical realism of our proposed mixed-feedback design.

Quantitatively, the measured spiking and inter-burst frequency increased from approximately 0.5 Hz at 5 °C to 25 Hz at 45 °C. These changes remained smooth and monotonic, without any loss of excitatory behavior or irregular activity. Across multiple trials and bias conditions, no degradation or drift was observed over repeated heating-cooling cycles, confirming the long-term stability and repeatability of the mixed-feedback neuron dynamics.

The observed increase in frequency arises naturally from transistor-level temperature effects. As temperature increases, the thermal voltage $U_T = kT/q$ and the carrier mobility μ both change, resulting in higher subthreshold currents for identical gate bias conditions. In the DPI filters, this results in proportionally faster charging and discharging, effectively reducing the time constants of the fast, slow, and ultraslow timescales. Otherwise, since all bias voltages are set by the same external source, changes in currents scale proportionally across all feedback loops, preserving the relative strength of the fast, slow, and ultraslow feedback pathways. As a result, the mixed-feedback neuron maintains its excitability regime, while its temporal dynamics accelerate uniformly. Note that, in the bursting regime, the number of spikes per burst decreases at higher temperatures. This is consistent with our model, since the ultraslow negative feedback accelerates with temperature without an accompanying positive component to counterbalance it. Importantly, the interplay between the fast and slow timescales which gives rise to bursting remains unaffected, and the neuron maintains its excitability type despite the change in burst length. Indeed, this interplay is determined by the relative organization of the bistability thresholds of the steady-state characteristics, as explained in Section 2.3, which is preserved under temperature variations, consistently with the scaling of all currents as per established analytical models of subthreshold operation [51].

Overall, the mixed-feedback architecture provides an intrinsic form of temperature and bias self-regulation: when environmental conditions shift, the system’s internal currents scale coherently, preserving its qualitative behavior without requiring external compensation. This property further enhances the stability and robustness of the proposed model.

Reference	Technology	Implement.	Model	Biologically plausible NMD	Area	Energy/Power
Hynna [17]	0.25 μm CMOS	V-mode	T-Channel Axon-Hillock	Yes	774 μm^2	?
Wijekoon [52]	0.35 μm CMOS	V-mode	Izhikevich (accelerated)	No	2800 μm^2	9 pJ/spike (8 to 40 μW)
Livi [45]	0.35 μm CMOS	I-mode	AdEx	N/A	913 μm^2	7 pJ/pulse, 267 pJ/spike
Yu [55]	0.5 μm CMOS	V-mode	Extended HH / Morris-Lecar	Yes	0.72 mm^2	80 nJ/spike (160 μW)
Folowosele [56]	0.5 μm CMOS	Switched capacitors	Mihalaş-Niebur	No	0.05 mm^2	2.375 μW
Wang [57]	130 nm CMOS	Mixed	I&F	No	26.5 μm^2	High (FPGA)
Aamir [28, 29]	65 nm CMOS	V-mode	AdEx (accelerated)	N/A	2352 μm^2	(790 $\pm$ 170) pJ/spike
Liu [21]	Pt/Co ₃ O _{4-x} /ITO	Memristive	—	N/A	—	—
Liu [19]	180 nm CMOS	V-mode	Mixed-feedback	Yes	2590 μm^2	697 to 969 nJ/spike
Xiao [58]	NbO ₂ + ECRAM	Memristive	Fast-slow memristive	N/A	—	—
Our work	180 nm CMOS	Analog I-mode	Mixed-feedback (w/ inactivation)	Yes	5400 μm^2	40 to 200+ pJ/spike (simulated)

Table 1. Comparison of state-of-the-art bursting silicon neurons (I&F: integrate-and-fire, HH: Hodgkin–Huxley, AdEx: Adaptive Exponential I&F). For our work, area and energy refer to the mismatch-optimized layout (Table 2).

4 Discussion

4.1 Comparison of state-of-the-art bursting silicon neurons

To position our silicon neuron implementation within the state-of-the-art, we present a comparative overview of silicon neurons capable of generating bursting dynamics in the literature in Table 1. Unlike most prior work, which predominantly relies on voltage-mode implementations and simplified models such as the Izhikevich or AdEx neuron, our design offers a fully analog, current-mode implementation of the mixed-feedback model, extended here with a biologically motivated inactivation mechanism. This current-mode approach enables lower power consumption without sacrificing the richness of the dynamics, providing an efficient alternative to both digital implementations and transconductance-based analog designs. Compared to earlier works, such as those of Hynna [17] and Wijekoon [52], our neuron supports more diverse and biologically plausible behaviors while maintaining comparable or superior energy efficiency. The mixed-feedback model used here has been shown to uniquely exhibit a biologically consistent phase-plane structure, unlike the Izhikevich model, which suffers from limited tunability [11, 53, 54].

While recent work by Liu et al. [19] has demonstrated a first silicon implementation of the mixed-feedback model in voltage-mode, our current-mode architecture further improves energy efficiency (down to 45 pJ/spike at 105 Hz) and simplifies interfacing in large-scale neuromorphic systems. Overall, our neuron offers a unique combination of functional richness, biological plausibility, and energy efficiency, enabled by the choice of a fully analog current-mode implementation of a robust and tunable phase-portrait-based model.

The relatively large area of our neuron ($\sim 5400 \mu\text{m}^2$) is primarily driven by the capacitors implementing the slow and ultraslow DPI filters, which are essential to implement biologically relevant time constants in subthreshold operation and separate the timescales of the mixed-feedback model by a few orders of magnitude. This reflects a fundamental trade-off between biophysical realism and integration density. Several circuit-level techniques could in principle reduce the required capacitor area, including active capacitance multiplication [46], switched-capacitor time constant emulation [59], and bulk biasing to reduce leakage currents [60].

These approaches reduce physical capacitance area at the cost of additional circuit complexity, increased power consumption, potential deviations from ideal dynamics, added noise sources, and increased sensitivity to mismatch. The choice between explicit capacitor-based integration and more compact circuit techniques therefore reflects a broader trade-off between density and robustness of the neuron's dynamical behavior. More radical density improvements may arise from emerging neuromorphic devices such as memristive devices [61, 62] now available in CMOS technology nodes [63], and novel uses of existing devices for physics-based integration mechanisms [64]. Such approaches could partially replace large explicit capacitors by exploiting intrinsic device dynamics for integration and memory, offering promising directions for future implementations of the mixed-feedback architecture.

Technology scaling is another important consideration that offers both benefits and constraints. While migration to more advanced, smaller nodes would reduce dynamic energy consumption due to lower supply voltages and smaller parasitic capacitances, it limits voltage headroom and typically increases leakage currents [65]. Moreover, in subthreshold analog circuits, transistor dimensions are primarily dictated by mismatch and noise constraints, and capacitor density does not scale proportionally with feature size. Migrating to smaller nodes would therefore not necessarily result in proportional area reduction. As a result, while the mixed-feedback architecture is in principle compatible with advanced nodes, energy and area scaling will depend on careful circuit design optimization, although energy per spike is generally expected to decrease.

4.2 Interfacing and system-level considerations

While this work focuses on the design and characterization of a single neuromorphic neuron, practical deployment requires interconnection with other neurons and synapses through a suitable communication scheme. Many neuromorphic systems address this using event-based protocols such as Address Event Representation (AER) or continuous-time current-mode interconnects in more tightly coupled architectures. While the energy and area overhead associated with these interfaces can be significant at scale, they are largely orthogonal to the intrinsic neuron dynamics presented here and depend strongly on communication sparsity and system-level design trade-offs. The neuron-level energy per spike reported in this work therefore provides a meaningful and generalizable metric for comparing neuronal primitives, with interface optimization more appropriately addressed at the system design stage.

In the proposed architecture, the output of the fast sigmoidal block provides a natural and reliable indicator of spike onset. Thanks to its sharp, saturating transition, this signal reliably switches state during each action potential, independently of slower adaptation or bursting dynamics. As a result, it can be directly interpreted as a spike event without requiring additional thresholding or edge-detection circuitry. It can then be easily copied, rectified, or level-shifted using simple current-mode circuits, enabling straightforward interfacing with event-based communication schemes such as AER, as well as with hybrid continuous-time and digital neuromorphic architectures. This separation between the internal continuous-time dynamics and an explicit spike signaling node facilitates modular integration of the neuron into larger networks while preserving its intrinsic low-power operation.

Beyond single-neuron properties, several features of the current-mode mixed-feedback architecture directly support scalable integration. Synaptic and neuronal interactions are naturally expressed as currents, enabling direct summation without additional conversion or arbitration circuitry. Energy per spike remains low and largely independent of absolute current scaling, which is advantageous in large, sparsely active networks. Moreover, the modular separation between neuron dynamics, spike signaling, and communication interfaces allows interconnect architectures to be optimized independently of the neuron. While these characteristics do not, by themselves, constitute a complete neuromorphic system, they provide concrete architectural advantages that motivate the use of the proposed neuron as a building block for large-scale neuromorphic platforms.

5 Conclusions

We have demonstrated a fully analog current-mode implementation of a biologically inspired mixed-feedback neuron model that enables robust and tunable neuromodulation in neuromorphic hardware. The proposed circuit uses two types of subthreshold current-mode blocks interconnected in a feedback configuration and introduces a positive-feedback inactivation mechanism. The resulting neuron can be tuned using mathematical steady-state analyses and exhibits predictable and reliable excitability and neuromodulation in simulation and hardware. A 180 nm CMOS prototype exhibits spiking, bursting, and real-time neuromodulation between the two using a single

bias parameter across wide temperature ranges, validating the model and the robustness of the current-mode mixed-feedback approach to global current variations. The neuron operates at 40 to 200 pJ/spike at a 1.8 V supply, confirming ultra-low-power operation at the single neuron level and suitability for integration into large-scale neuromorphic systems. Experimental measurements indicate good neuron-to-neuron consistency across fabricated devices, and Monte Carlo simulations further show that uniform current scaling provides an effective design knob to trade ultra-low-power operation for improved regime yield and frequency consistency under device mismatch. Overall, the proposed architecture demonstrates that reliable neuromodulable bursting and spiking dynamics can be achieved with current-mode design principles and scalable energy operation. By combining analytical grounding, silicon validation, and robustness evaluation, this work establishes the proposed neuron as a practical, scalable building block for energy-efficient neuromorphic systems.

Future work will showcase the capabilities of networks of mixed-feedback neurons interconnected through synaptic and neuromodulatory interactions to enable adaptive signal processing and sensorimotor control applications. A forthcoming chip will integrate an array of the mixed-feedback neurons presented here, with a revised layout to minimize mismatch, and programmable synaptic connections and neuromodulatory pathways to demonstrate network-level behavioral modulation. This new chip will also enable experimental validation of the energy per spike and power consumption metrics presented in this work. In parallel, we will investigate closed-loop neuromodulation controllers, such as the one presented in [66], to autonomously tune bias currents and compensate for device mismatch using knowledge of the neuron's mathematical model. Together, these developments aim to advance mixed-feedback neuromorphic hardware from single-neuron demonstrations towards adaptive, energy-efficient analog computing systems.

Acknowledgments

We gratefully acknowledge Philipp Klein for his advice and suggestions on the neuron layout, François Piron for his work on the floorplanning of the test chip and his support during the tapeout phase, and Guillaume Drion for his feedback and advice on the modeling aspects of this work.

Funding

This work was supported by the Belgian Government through the Federal Public Service Policy and Support grant NEMODEL. Loris Mendolia is a FRIA Grantee of the Fonds de la Recherche Scientifique - FNRS. The authors would like to acknowledge the financial support of the CogniGron research center, the Ubbo Emmius Funds (Univ. of Groningen), and the HORIZON EUROPE EIC Pathfinder Grant ELEGANCE (Grant No. 101161114).

Author contributions

- Loris Mendolia: Conceptualization (lead), Data curation, Formal analysis (lead), Investigation (lead), Methodology (equal), Software, Visualization (lead), Writing - original draft (lead), Writing - review and editing (lead).
- Chenxi Wen: Conceptualization (supporting), Investigation (supporting), Methodology (supporting), Writing - review and editing (supporting).
- Elisabetta Chicca: Conceptualization (supporting), Investigation (supporting), Resources (supporting), Writing - review and editing (supporting).
- Giacomo Indiveri: Conceptualization (supporting), Investigation (supporting), Writing - review and editing (supporting).
- Rodolphe Sepulchre: Conceptualization (supporting), Writing - review and editing (supporting).
- Jean-Michel Redouté: Conceptualization (supporting), Funding acquisition (equal), Investigation (supporting), Project administration (equal), Resources (equal), Supervision (equal), Writing - original draft (supporting), Writing - review and editing (supporting).
- Alessio Franci: Conceptualization (lead), Formal analysis (supporting), Funding acquisition (equal), Investigation (supporting), Methodology (equal), Project administration (equal), Resources (equal), Supervision (equal), Visualization (supporting), Writing - original draft (supporting), Writing - review and editing (lead).

Data availability

All data that support the findings of this study are included within the article. A Julia-based solver of the circuit equations (5) is available on github.com/LorisMendolia/IMF-Neuron-Circuit-Sim.

Supplementary data

A Full circuit schematic

The full schematic of the current-mode mixed-feedback neuron presented in this work is displayed in Fig. 14. Transistor dimensions and capacitor sizes used in a revised layout optimized for mismatch are reported in Table 2. The dimensions of all transistors of the test circuits used to obtain the experimental results in Section 3 of this work are $W \times L = 3 \mu\text{m} \times 300 \text{ nm}$.

Transistors	$D_{f1,2}$	$D_{s,u1,2}$	D3	D_{f4}	$D_{s,u4}$	S1	S2,5,7	S3,4,6	M1,2,5	M3,4
$W \times L$ (μm)	1×3	2.5×4	4×5	2×2	5×5	3×5	4×5	2×0.6	4×5	2×5
Capacitor						C_f	C_s	C_u		
Total capacitance						0.5 pF	2 pF	8 pF		

Table 2. Mixed-feedback neuron circuit component dimensions and values (from a mismatch-optimized layout).

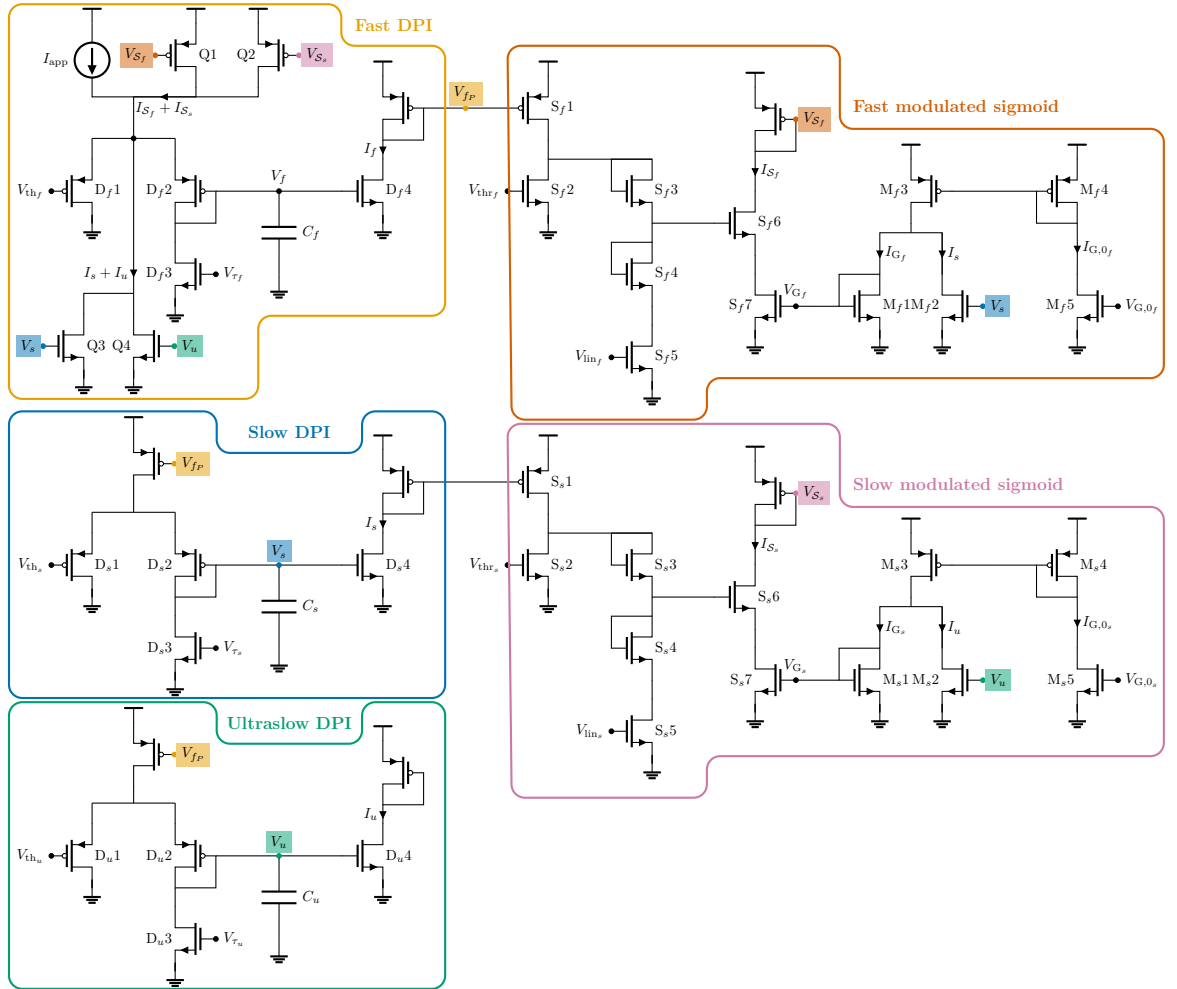


Figure 14. Full current-mode mixed-feedback neuron schematic, implementing the structure detailed in Section 2.1 and in Fig. 2, using the sub-circuits presented in Section 2.2 and shown in Figs. 4 and 5. All transistors operate in the subthreshold regime. The fast DPI (D_{f1-4} , yellow) models the passive membrane dynamics of the neuron. The fast current-mode sigmoid (S_{f1-7} , orange) provides fast positive feedback on the membrane potential to create the spike upstroke, corresponding to rapid sodium channel dynamics. The slow and ultraslow DPIs ($D_{s/u1-4}$, blue and green) introduce linear slow and ultraslow negative feedback to the system, providing repolarization and spike-frequency adaptation currents to the membrane respectively, capturing the effects of delayed-rectifier and calcium-activated potassium currents [40, 41]. The slow current-mode sigmoid (S_{s1-7} , pink) provides slow positive feedback on the membrane to create slow regenerative dynamics, mimicking low-threshold calcium currents which support bursting or regenerative depolarization. The positive feedback inactivation circuits ($M_{f/s1-5}$) in the sigmoid blocks subtract copies of the slow and ultraslow currents from the base gain current of the fast and slow sigmoids respectively, inspired by biological sodium channel inactivation observed following spike initiation [43]. All unlabeled transistors are part of current mirrors that copy the currents associated with the highlighted gate voltages to implement the various feedback loops of the model.

B Nominal bias parameters

The nominal bias parameters used for all simulations of our mixed-feedback neuron presented in this work are reported in Table 3. For experimental results, these currents were converted to bias voltages and applied directly to the corresponding transistor gates.

I_{τ_f}, I_{th_f}	I_{τ_s}, I_{th_s}	I_{τ_u}, I_{th_u}	I_{thr_f}	I_{lin_f}	$I_{G,0_f}$	I_{thr_s}	I_{lin_s}	$I_{G,0_s}$ (spk./bst.)
100 pA	20 pA	10 pA	110 pA	250 pA	700 pA	90 pA	50 pA	200 pA/270 pA

Table 3. Nominal bias currents used in all simulations and approximated in all experiments reported in this work.

C Sigmoid circuit equations

Writing the standard subthreshold MOSFET equations without channel length modulation effect (eq. (3.2.15 of [67])) for transistors Q1-7 of Fig. 5, only assuming saturation for transistor Q6, yields

$$\text{Q1: } I_{Q1} = I_0 e^{\kappa(V_{DD}-V_{in})/U_T} \left(1 - e^{-(V_{DD}-V_{cmp})/U_T}\right), \quad (7)$$

$$\text{Q2: } I_{Q2} = I_0 e^{\kappa V_{thr}/U_T} \left(1 - e^{-V_{cmp}/U_T}\right), \quad (8)$$

$$\text{Q3: } I_{cas} = I_0 e^{(\kappa V_{cmp}-V_{out})/U_T} \left(1 - e^{-(V_{cmp}-V_{out})/U_T}\right), \quad (9)$$

$$\text{Q4: } I_{cas} = I_0 e^{(\kappa V_{out}-V_{cas})/U_T} \left(1 - e^{-(V_{out}-V_{cas})/U_T}\right), \quad (10)$$

$$\text{Q5: } I_{cas} = I_0 e^{\kappa V_{in}/U_T} \left(1 - e^{-V_{cas}/U_T}\right), \quad (11)$$

$$\text{Q6: } I_{out} = I_0 e^{(\kappa V_{out}-V_{mid})/U_T}, \quad (12)$$

$$\text{Q7: } I_{out} = I_0 e^{\kappa V_G/U_T} \left(1 - e^{-V_{mid}/U_T}\right). \quad (13)$$

writing the KCL at the common drain between Q1 and Q2 also yields

$$I_{cas} = I_{Q1} - I_{Q2}. \quad (14)$$

The input voltage V_{in} can be assumed to come from a properly saturated PMOS transistor:

$$I_{in} = I_0 e^{\kappa(V_{DD}-V_{in})/U_T}. \quad (15)$$

From Eqs. (12) and (13), the output current can be expressed as a function of V_{out} as

$$I_{out} = I_0 \frac{e^{\kappa V_G/U_T}}{1 + e^{\kappa(V_G-V_{out})/U_T}}, \quad (16)$$

which takes the shape of a shifted and scaled logistic function $\mathcal{S}(V_{out}) = k \frac{1}{1+e^{-V_{out}}} + b$. If the uniqueness and monotonicity of a solution for V_{out} as a function of V_{in} can be proven, this justifies the sigmoidal input-output characteristic of the circuit.

The three devices Q3-5 form a series stack carrying a common current I_{cas} . At this stage, I_{cas} is treated as an unknown scalar parameter.

- For a given I_{cas} , (11) uniquely determines V_{cas} , since the right-hand side is continuous and strictly increasing in V_{cas} .
- With V_{cas} fixed, (10) uniquely determines V_{out} , as the current is strictly increasing in V_{out} .
- With V_{out} fixed, (9) uniquely determines V_{cmp} , as the current is strictly increasing in V_{cmp} .

Thus, the cascode chain defines unique, strictly increasing functions

$$V_{cas} = f_5(I_{cas}), \quad V_{out} = f_4(I_{cas}), \quad V_{cmp} = f_3(I_{cas}). \quad (17)$$

Substituting (7) and (8) into (14) yields

$$I_{cas} = I_0 e^{\kappa(V_{DD}-V_{in})/U_T} \left(1 - e^{-(V_{DD}-V_{cmp})/U_T}\right) - I_0 e^{\kappa V_{thr}/U_T} \left(1 - e^{-V_{cmp}/U_T}\right). \quad (18)$$

The right-hand side of (18) is continuous and strictly increasing in V_{cmp} , and strictly decreasing in V_{in} .

Substituting $V_{\text{cmp}} = f_3(I_{\text{cas}})$ into (18) yields a single implicit equation in I_{cas} :

$$I_{\text{cas}} = I_0 e^{\kappa(V_{DD} - V_{\text{in}})/U_T} \left(1 - e^{-(V_{DD} - f_3(I_{\text{cas}}))/U_T}\right) - I_0 e^{\kappa V_{\text{thr}}/U_T} \left(1 - e^{-f_3(I_{\text{cas}})/U_T}\right). \quad (19)$$

This equation does not admit a closed-form solution in elementary functions.

For fixed V_{in} , both sides of the implicit equation are continuous and strictly increasing functions of I_{cas} . Therefore, a unique solution for I_{cas} exists. Since $V_{\text{out}} = f_4(I_{\text{cas}})$, the output voltage is also uniquely defined.

Moreover, because I_{cas} is strictly decreasing in V_{in} and V_{out} is strictly increasing in I_{cas} , the input-output characteristic satisfies

$$\frac{dV_{\text{out}}}{dV_{\text{in}}} < 0, \quad (20)$$

i.e., the input-output characteristic is strictly monotonic.

Adding that V_{in} is strictly increasing in I_{in} from (15), and with at the V_{out} to I_{out} relationship in (16), this proves that our sigmoid circuit implements a strictly monotonic and increasing scaled and shifted logistic sigmoidal relationship between the input current I_{in} and the output current I_{out} . $\square$

D Experimental variability evaluation

To assess the effect of device mismatch on the fabricated neuron circuits, we experimentally measured the input-frequency (I-F) characteristics of neurons from both the original prototype presented in Section 3 and from the revised layout (Table 2). In both cases, we used the same nominal spiking bias parameters in the nanoampere range used for the Monte Carlo analysis of Section 3.2.4. The input current was swept over the same interval for all neurons without any parameter tuning.

For the revised implementation, the resulting I-F curves shown in the left panel of Fig. 15 indicate that, despite transistor mismatch and process variations, all neurons follow a similar increase in firing rate over the full input range, with slight variations in rheobases and slopes. The average coefficient of variation (CV) of the firing rate over the measured input range is 24%. These measurements are consistent with the Monte Carlo analysis of Section 3.2.4 and indicate that the proposed circuit provides a reproducible qualitative dynamical behavior across fabricated neurons under fixed bias parameters without requiring neuron-specific calibration.

By contrast, the original prototype, which used a simpler layout without optimized transistor sizing, exhibits more substantial neuron-to-neuron variability and lower yield, as shown in the right panel of Fig. 15. The measured I-F curves show more pronounced variations in rheobase and slope, with an average firing rate CV of 50%. Since the circuit topology, bias parameters, input current range, and measurement procedure are identical between the two measurements, the difference in observed variability provides an experimental illustration of the importance of the revised device dimensions and layout for mismatch reduction. We therefore promote this revised implementation as the reference design and basis for further scaling in larger-scale neuromorphic systems.

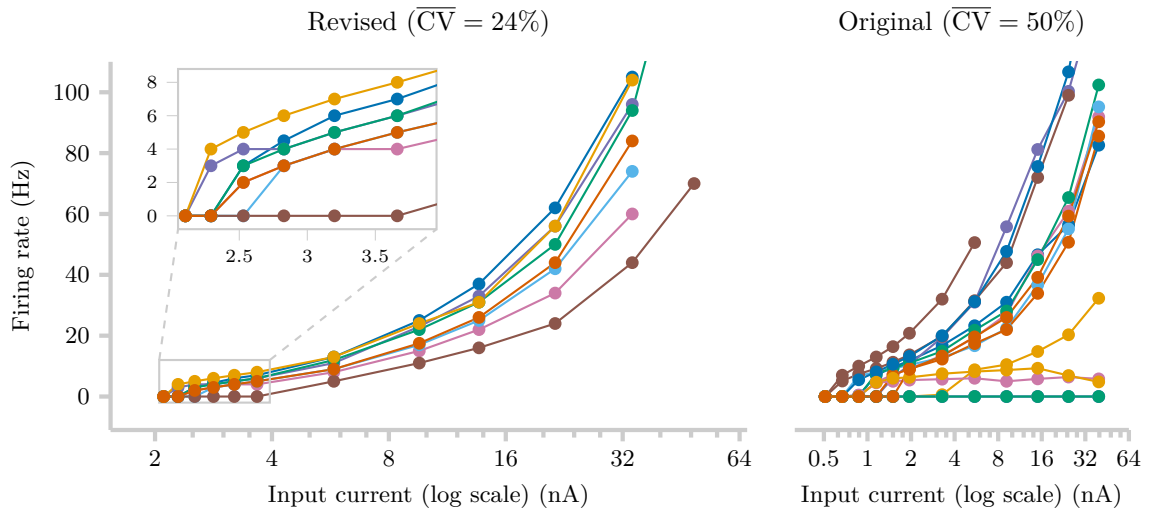


Figure 15. Experimental measurement of the input-frequency (I-F) characteristics of 8 neurons fabricated using the revised layout (left) and the 16 neurons of the original prototype (right), with identical nominal nanoampere-range spiking bias parameters. All neurons using the revised layout follow the same qualitative increase in firing rate, with an average coefficient of variation (CV) of 24%, while the original version exhibits greater variability.

References

- [1] C. I. Bargmann, “Beyond the connectome: how neuromodulators shape neural circuits,” *BioEssays: News and Reviews in Molecular, Cellular and Developmental Biology*, vol. 34, pp. 458–465, June 2012.
- [2] E. Marder, “Neuromodulation of Neuronal Circuits: Back to the Future,” *Neuron*, vol. 76, pp. 1–11, Oct. 2012.
- [3] M. C. Avery and J. L. Krichmar, “Neuromodulatory Systems and Their Interactions,” *Frontiers in Neural Circuits*, vol. 11, p. 108, Dec. 2017.
- [4] G. Drion, A. Franci, and R. Sepulchre, “Cellular switches orchestrate rhythmic circuits,” *Biological Cybernetics*, vol. 113, pp. 71–82, Apr. 2019.
- [5] D. A. McCormick and M. P. Nusbaum, “Editorial overview: Neuromodulation: Tuning the properties of neurons, networks and behavior,” *Current opinion in neurobiology*, vol. 29, pp. iv–vii, Dec. 2014.
- [6] C. Bartolozzi, G. Indiveri, and E. Donati, “Embodied neuromorphic intelligence,” *Nature Communications*, vol. 13, p. 1024, Feb. 2022.
- [7] S. Sherman, “Tonic and burst firing: dual modes of thalamocortical relay,” *Trends in Neurosciences*, vol. 24, pp. 122–126, Feb. 2001.
- [8] C. Mead, “Neuromorphic electronic systems,” *Proceedings of the IEEE*, vol. 78, pp. 1629–1636, Oct. 1990.
- [9] G. Indiveri, “Neuromorphic is dead. long live neuromorphic,” *Neuron*, pp. 1–4, Oct. 2025.
- [10] E. Chicca, F. Stefanini, C. Bartolozzi, and G. Indiveri, “Neuromorphic Electronic Circuits for Building Autonomous Cognitive Systems,” *Proceedings of the IEEE*, vol. 102, pp. 1367–1388, Sept. 2014.
- [11] C. D. Schuman, T. E. Potok, R. M. Patton, J. D. Birdwell, M. E. Dean, G. S. Rose, and J. S. Plank, “A Survey of Neuromorphic Computing and Neural Networks in Hardware,” May 2017. arXiv:1705.06963 [cs].
- [12] E. O. Neftci, “Data and Power Efficient Intelligence with Neuromorphic Learning Machines,” *iScience*, vol. 5, pp. 52–68, July 2018.
- [13] J.-Q. Yang, R. Wang, Y. Ren, J.-Y. Mao, Z.-P. Wang, Y. Zhou, and S.-T. Han, “Neuromorphic Engineering: From Biological to Spike-Based Hardware Nervous Systems,” *Advanced Materials*, vol. 32, no. 52, p. 2003610, 2020.
- [14] C.-S. Poon and K. Zhou, “Neuromorphic Silicon Neurons and Large-Scale Neural Networks,” *Frontiers in Neuroscience*, vol. 5, p. 108, Sept. 2011.
- [15] C. S. Thakur, J. L. Molin, G. Cauwenberghs, G. Indiveri, K. Kumar, N. Qiao, J. Schemmel, R. Wang, E. Chicca, J. Olson Hasler, J.-s. Seo, S. Yu, Y. Cao, A. van Schaik, and R. Etienne-Cummings, “Large-Scale Neuromorphic Spiking Array Processors: A Quest to Mimic the Brain,” *Frontiers in Neuroscience*, vol. 12, p. 891, Dec. 2018.
- [16] T. Wunderlich, A. F. Kungl, E. Müller, A. Hartel, Y. Stradmann, S. A. Aamir, A. Grübl, A. Heimbrecht, K. Schreiber, D. Stöckel, C. Pehle, S. Billaudelle, G. Kiene, C. Mauch, J. Schemmel, K. Meier, and M. A. Petrovici, “Demonstrating advantages of neuromorphic computation: A pilot study,” *Frontiers in Neuroscience*, vol. 13, 2019.
- [17] K. M. Hynna and K. Boahen, “Silicon neurons that burst when primed,” in *2007 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 3363–3366, May 2007. ISSN: 2158-1525.
- [18] T. Yu and G. Cauwenberghs, “Analog VLSI Biophysical Neurons and Synapses With Programmable Membrane Channel Kinetics,” *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, pp. 139–148, June 2010.

- [19] K. Liu, S. Hashemkhani, J. Rubin, and R. Kubendran, “BioNN: Bio-Mimetic Neural Networks on Hardware Using Nonlinear Multi-Timescale Mixed-Feedback Control for Neuromodulatory Bursting Rhythms,” *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 13, pp. 914–926, Dec. 2023.
- [20] X. Li, Q. Chen, and F. Xue, “Bursting dynamics remarkably improve the performance of neural networks on liquid computing,” *Cognitive Neurodynamics*, vol. 10, pp. 415–421, Oct. 2016.
- [21] H. Liu, X. Zhu, Z. Guo, R. He, X. Li, Q. Sun, X. Ye, C. Sun, Y. Tian, and R.-W. Li, “Artificial Spiking Neuron with Bursting Dynamics for Noise-Resistant Neuromorphic Coding,” *ACS Applied Electronic Materials*, vol. 5, pp. 3454–3461, June 2023.
- [22] M. Stuck, X. Wang, and R. Naud, “A burst-dependent algorithm for neuromorphic on-chip learning of spiking neural networks,” *Neuromorphic Computing and Engineering*, vol. 5, p. 014010, Feb. 2025.
- [23] J. Mei, A. Rodriguez-Garcia, D. Takeuchi, G. Wainstein, N. Hubig, Y. Mohsenzadeh, and S. Ramaswamy, “Improving the adaptive and continuous learning capabilities of artificial neural networks: Lessons from multi-neuromodulatory dynamics,” Jan. 2025. arXiv:2501.06762 [q-bio].
- [24] A. J. Ijspeert, “Central pattern generators for locomotion control in animals and robots,” *Neural Networks*, vol. 21, pp. 642–653, May 2008.
- [25] E. Donati, R. Krause, and G. Indiveri, “Neuromorphic Pattern Generation Circuits for Bioelectronic Medicine,” Feb. 2021. arXiv:2102.09630 [cs].
- [26] A. Athota, B. Caccam, R. Kochis, A. Ray, G. Cauwenberghs, and F. D. Broccard, “Neuromorphic Instantiation of Spiking Half-Centered Oscillator Models for Central Pattern Generation,” in *2021 43rd Annual International Conference of the IEEE Engineering in Medicine & Biology Society (EMBC)*, pp. 6703–6706, Nov. 2021.
- [27] P. Lopez-Osorio, A. Patiño-Saucedo, J. P. Dominguez-Morales, H. Rostro-Gonzalez, and F. Perez-Peña, “Neuromorphic adaptive spiking CPG towards bio-inspired locomotion,” *Neurocomputing*, vol. 502, pp. 57–70, Sept. 2022.
- [28] C. Pehle, S. Billaudelle, B. Cramer, J. Kaiser, K. Schreiber, Y. Stradmann, J. Weis, A. Leibfried, E. Müller, and J. Schemmel, “The BrainScaleS-2 accelerated neuromorphic system with hybrid plasticity,” Feb. 2022. arXiv:2201.11063 [cs].
- [29] S. A. Aamir, Y. Stradmann, P. Müller, C. Pehle, A. Hartel, A. Grübl, J. Schemmel, and K. Meier, “An Accelerated LIF Neuronal Network Array for a Large-Scale Mixed-Signal Neuromorphic Architecture,” *IEEE Transactions on Circuits and Systems—Part I: Regular Papers*, vol. 65, pp. 4299–4312, Dec. 2018.
- [30] O. Richter, C. Wu, A. M. Whatley, G. Köstinger, C. Nielsen, N. Qiao, and G. Indiveri, “DYNAP-SE2: a scalable multi-core dynamic neuromorphic asynchronous spiking neural network processor,” *Neuromorphic Computing and Engineering*, vol. 4, p. 014003, Jan. 2024. Publisher: IOP Publishing.
- [31] A. Franci, G. Drion, V. Seutin, and R. Sepulchre, “A Balance Equation Determines a Switch in Neuronal Excitability,” *PLOS Computational Biology*, vol. 9, p. e1003040, May 2013.
- [32] G. Drion, A. Franci, J. Dethier, and R. Sepulchre, “Dynamic Input Conductances Shape Neuronal Spiking,” *eneuro*, vol. 2, pp. ENEURO.0031–14.2015, Jan. 2015.
- [33] F. Castaños and A. Franci, “Implementing robust neuromodulation in neuromorphic circuits,” *Neurocomputing*, vol. 233, pp. 3–13, Apr. 2017.
- [34] L. Ribar and R. Sepulchre, “Neuromodulation of Neuromorphic Circuits,” *IEEE Transactions on Circuits and Systems—Part I: Regular Papers*, vol. 66, pp. 3028–3040, Aug. 2019.
- [35] R. Sepulchre, G. Drion, and A. Franci, “Control Across Scales by Positive and Negative Feedback,” *Annual Review of Control, Robotics, and Autonomous Systems*, vol. 2, pp. 89–113, May 2019.

- [36] A. Rubino, C. Livanelioglu, N. Qiao, M. Payvand, and G. Indiveri, “Ultra-Low-Power FDSOI Neural Circuits for Extreme-Edge Neuromorphic Intelligence,” *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, pp. 45–56, Jan. 2021.
- [37] A. Rubino, *Mixed-Signal Neuromorphic Circuits and Systems for Extreme-Edge Computing*. PhD thesis, University of Zurich, Zürich, Mar. 2025.
- [38] C. Bartolozzi, S. Mitra, and G. Indiveri, “An ultra low power current-mode filter for neuromorphic systems and biomedical signal processing,” in *2006 IEEE Biomedical Circuits and Systems Conference*, pp. 130–133, Nov. 2006. ISSN: 2163-4025.
- [39] B. Hille, *Ion Channels of Excitable Membranes*. Sinauer Associates Inc., U.S., 2001.
- [40] A. L. Hodgkin and A. F. Huxley, “A quantitative description of membrane current and its application to conduction and excitation in nerve,” *The Journal of Physiology*, vol. 117, pp. 500–544, Aug. 1952.
- [41] E. M. Izhikevich, *Dynamical Systems in Neuroscience: The Geometry of Excitability and Bursting*. The MIT Press, July 2006.
- [42] S. DeWeerth, L. Nielsen, C. Mead, and K. Astrom, “A simple neuron servo,” *IEEE Transactions on Neural Networks*, vol. 2, pp. 248–251, Mar. 1991.
- [43] Y. Zang, E. Marder, and S. Marom, “Sodium channel slow inactivation normalizes firing in axons with uneven conductance distributions,” *Current Biology*, vol. 33, pp. 1818–1824.e3, May 2023.
- [44] C. Bartolozzi and G. Indiveri, “Synaptic dynamics in analog VLSI,” *Neural Computation*, vol. 19, pp. 2581–2603, Oct. 2007.
- [45] P. Livi and G. Indiveri, “A current-mode conductance-based silicon neuron for address-event neuromorphic systems,” in *2009 IEEE International Symposium on Circuits and Systems*, pp. 2898–2901, May 2009. ISSN: 2158-1525.
- [46] B. Razavi, *Design of analog CMOS integrated circuits*. New York, NY: McGraw-Hill Education, second edition ed., 2017.
- [47] A. Franci, G. Drion, and R. Sepulchre, “Robust and tunable bursting requires slow positive feedback,” *Journal of Neurophysiology*, vol. 119, pp. 1222–1234, Mar. 2018.
- [48] M. D. Gomony, B. Ahn, R. Luiken, Y. Biyani, A. Gebregiorgis, A. Laborieux, F. Zenke, S. Hamdioui, and H. Corporaal, “Achieving PetaOps/W Edge-AI Processing,” in *Proceedings of the 61st ACM/IEEE Design Automation Conference, DAC ’24*, (New York, NY, USA), pp. 1–4, Association for Computing Machinery, Nov. 2024.
- [49] L. S. Tang, A. L. Taylor, A. Rinberg, and E. Marder, “Robustness of a Rhythmic Circuit to Short- and Long-Term Temperature Changes,” *Journal of Neuroscience*, vol. 32, pp. 10075–10085, July 2012.
- [50] J. Ratliff, A. Franci, E. Marder, and T. O’Leary, “Neuronal oscillator robustness to multiple global perturbations,” *Biophysical Journal*, vol. 120, pp. 1454–1468, Apr. 2021. Publisher: Elsevier.
- [51] B. V. Benjamin, R. L. Smith, and K. A. Boahen, “An Analytical MOS Device Model With Mismatch and Temperature Variation for Subthreshold Circuits,” *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, pp. 1826–1830, June 2023.
- [52] J. H. B. Wijekoon and P. Dudek, “Compact silicon neuron circuit with spiking and bursting behaviour,” *Neural Networks*, vol. 21, pp. 524–534, Mar. 2008.
- [53] G. Drion, A. Franci, V. Seutin, and R. Sepulchre, “A Novel Phase Portrait for Neuronal Excitability,” *PLOS ONE*, vol. 7, no. 8, p. e41806, 2012.
- [54] K. Jacquerie and G. Drion, “Robust switches in thalamic network activity require a timescale separation between sodium and T-type calcium channel activations,” *PLOS Computational Biology*, vol. 17, no. 5, p. e1008997, 2021.

- [55] T. Yu, T. J. Sejnowski, and G. Cauwenberghs, “Biophysical Neural Spiking, Bursting, and Excitability Dynamics in Reconfigurable Analog VLSI,” *IEEE Transactions on Biomedical Circuits and Systems*, vol. 5, pp. 420–429, Oct. 2011.
- [56] F. Folowosele, T. J. Hamilton, and R. Etienne-Cummings, “Silicon Modeling of the Mihalaş–Niebur Neuron,” *IEEE Transactions on Neural Networks*, vol. 22, pp. 1915–1927, Dec. 2011.
- [57] R. Wang, C. S. Thakur, T. J. Hamilton, J. Tapson, and A. Van Schaik, “A compact aVLSI conductance-based silicon neuron,” in *2015 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, (Atlanta, GA, USA), pp. 1–4, IEEE, Oct. 2015.
- [58] Y. Xiao, Y. Liu, B. Zhang, P. Chen, H. Zhu, E. He, J. Zhao, W. Huo, X. Jin, X. Zhang, H. Jiang, D. Ma, Q. Zheng, H. Tang, P. Lin, W. Kong, and G. Pan, “Bio-plausible reconfigurable spiking neuron for neuromorphic computing,” *Science Advances*, vol. 11, p. eadr6733, Feb. 2025.
- [59] T. C. Carusone, *Analog integrated circuit design*. Hoboken, NJ: J. Wiley & Sons, 2nd ed ed., 2012.
- [60] N. Qiao, G. Indiveri, and C. Bartolozzi, “Automatic gain control of ultra-low leakage synaptic scaling homeostatic plasticity circuits,” Aug. 2019. arXiv:1908.07412 [cs].
- [61] R. Berdan, E. Vasilaki, A. Khiat, G. Indiveri, A. Serb, and T. Prodromakis, “Emulating short-term synaptic dynamics with memristive devices,” *Scientific Reports*, vol. 6, no. 18639, pp. 1–9, 2016.
- [62] T. Moon, K. Soh, J. S. Kim, J. E. Kim, S. Y. Chun, K. Cho, J. J. Yang, and J. H. Yoon, “Leveraging volatile memristors in neuromorphic computing: from materials to system implementation,” *Materials Horizons*, vol. 11, no. 20, pp. 4840–4866, 2024.
- [63] M. Atia, M. Ismail, and M. Alhawari, “Hybrid Integration of Rram and Cmos Circuits Using Open-Source 130-nm PDK,” in *2025 37th International Conference on Microelectronics (ICM)*, pp. 1–6, Dec. 2025. ISSN: 2159-1679.
- [64] S. Pazos, K. Zhu, M. A. Villena, O. Alharbi, W. Zheng, Y. Shen, Y. Yuan, Y. Ping, and M. Lanza, “Synaptic and neural behaviours in a standard silicon transistor,” *Nature*, vol. 640, pp. 69–76, Apr. 2025.
- [65] H. Sood, V. M. Srivastava, and G. Singh, “Advanced MOSFET Technologies for Next Generation Communication Systems - Perspective and Challenges: A Review,” *Journal of Engineering Science and Technology Review*, vol. 11, pp. 180–195, Apr. 2018.
- [66] A. Fyon, P. Sacré, A. Franci, and G. Drion, “Reliable neuromodulation from adaptive control of ion channel expression,” *IFAC-PapersOnLine*, vol. 56, pp. 458–463, Jan. 2023.
- [67] S.-C. Liu, *Analog VLSI*. A Bradford book, Cambridge, Mass.: The MIT Press, Nov. 2002.