# Reducing Parasitic Oscillations of Capacitive Dividers Using Coaxial Symmetry in the Low-Voltage Arm

Thor Wens, Jean-François Fagnard, Philippe Laurent, Christophe Greffe and Philippe Vanderbemden

***Abstract*—In this paper, a new design rule to mitigate parasitic oscillations superimposing to the measurement of high-voltage pulses is proposed. We establish a transfer function of capacitive dividers that includes not only the self inductances of the high and low-voltage arms of the divider but also the mutual inductance that exists between both arms of the dividers. Mathematical analysis and experimental validation demonstrate that the parasitic oscillations can be significantly reduced by using a coaxial configuration of the low-voltage arm printed circuit board (PCB). The proposed design rule can be implemented on any capacitive divider, enabling a compact low-voltage side design, whose voltage division factor can be conveniently modified. In this work, the design rule is validated on a custom-built capacitive divider, designed to measure high-voltage pulses generated by spiral generators. The designed capacitive divider successfully measured pulses up to 289 kV with a voltage division factor exceeding 100,000 with minimal parasitic oscillations.**

***Index Terms*—capacitive divider, parasitic oscillations, design rule, high-voltage pulses, spiral generator.**

## I. Introduction

HIGH-VOLTAGE pulses of short duration (tens to hundreds of kilovolts lasting a few hundreds of nanoseconds) are essential in various industrial applications. They are used in rock fracturing [1], food sterilization without alteration of the nutrition [2] or as trigger generator for other devices, such as the input voltage of X-ray tubes [3]. Designing high-voltage pulse generators requires accurate measurement of the generated pulse amplitude, a challenging task. The measurement device must simultaneously withstand the high-voltage without undergoing dielectric breakdown, offer a sufficiently wide frequency bandwidth, and maintain a sufficiently small input capacitance to avoid altering the behavior of the voltage generator. Even when all these conditions are met, the measured signal contains undesired parasitic oscillations, limiting the achievable voltage division factors.

Several methods exist to measure high-voltage pulses, such as sphere gaps [4], Kerr cells [5], reflection type attenuators [6], or voltage dividers, the latter being the method studied in this paper. A voltage divider consists of two impedances connected in series, a high-voltage one $Z_{\mathrm{HV}}$ and a low-voltage one $Z_{\mathrm{LV}}$. The high-voltage input $V_{HV}$ is applied to both impedances, and the low-voltage output is measured across $Z_{\mathrm{LV}}$. Several topologies of voltage dividers can be obtained by changing the nature of the impedances $Z_{\mathrm{HV}}$ and $Z_{\mathrm{LV}}$. Resistive dividers have a limited bandwidth [7], which can be overcome using specific designs with $CuSO_4$ solutions [8], or using resistive-capacitive dividers or capacitive dividers. D-dot sensors are voltage dividers in which $Z_{\mathrm{LV}}$ is the impedance of the measuring device itself [9]. This paper focuses on capacitive voltage dividers. Even among capacitive dividers, several topologies exist. For example, in some configurations $C_{\mathrm{HV}}$ is formed by a stray capacitance [10].

Due to the parasitic elements of the capacitances $C_{\mathrm{LV}}$ and $C_{\mathrm{HV}}$, a pulse applied to the input of a capacitive divider induces self-resonance, causing undesired parasitic oscillations [11]. While it is possible to use specific filters to remove the oscillations by post-processing measurement signals [12], this can cause distortion of the measured signals. This work aims to deepen the understanding of the origin of the parasitic oscillations appearing in capacitive dividers and propose a new design rule that can be employed in any design of capacitive dividers to significantly reduce their amplitude.

Table I provides an overview of papers from the literature in which pulse voltage dividers are designed. It contains two main categories of information. Columns 2 to 6 present how the authors addressed parasitic oscillations in their designs. Columns 7 to 9 summarize the achieved characteristics of the dividers in terms of frequency limit $f_{\max}$, maximum voltage $V_{\max}$, and voltage division coefficient $K$, defined as the ratio between $V_{\mathrm{HV}}$ and $V_{\mathrm{LV}}$. When the paper specifies a minimum rise time $t_{rise}$ instead of a bandwidth, the frequency limit is estimated as $f_{\max} = 0.35\, t_{\mathrm{rise}}^{-1}$ [13], with the value shown in parentheses. Similarly, if the maximum voltage appears in parentheses, it indicates that the value was not explicitly specified. Instead, the highest value from the experimental data reported in the paper is provided.

When modeling capacitive dividers with parasitic elements, most studies consider the presence of self inductances. To reduce this parasitic inductance, the common guidelines are

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TABLE I
LITERATURE REVIEW OF HOMEMADE DIVIDERS FOR HIGH-VOLTAGE PULSE MEASUREMENTS.

| Reference | Guidelines for reduced parasitic oscillations | | | | | Performance | | |
|---|---|---|---|---|---|---|---|---|
| | SMD | Shield | $\nearrow f_{\mathrm{res}}$ | Distributed low-voltage | Special feature | $f_{\max}$ | $V_{\max}$ | $K$ |
| Hõbejõgi & Biela 2011 [14] | ✓ | ✓ | ✓ | | | >1 MHz | 200 kV | 1,000 |
| Pecquois et al. 2012 [15] | ✓ | ✓ | | ✓ | | 55 MHz | >500 kV | 10,000 |
| Ryu et al. 2016 [16] | | | | | | 1.62 GHz | (2 kV) | 102 |
| Wang et al. 2019 [17] | ✓ | | | ✓ | Optimized current flow to reduce magnetic flux | (234 MHz) | (2 kV) | 120,000 (2 stages) |
| Yu et al. 2019 [18] | | | | ✓ | Specific matching circuit near measurement device | (70 MHz) | NA | 25,000 |
| Betrakov et al. 2020 [19] | ✓ | | ✓ | | | 30 MHz | 30 kV | 2200 |
| Xie et al. 2022 [20] | ✓ | | ✓ | | Proper damping | 10 MHz | 700 kV | 10,500 |
| Kuhnke et al. 2023 [21] | ✓ | | ✓ | | | 139 kHz | 10 kV | 1300 |

to use Surface Mount Devices (SMD) capacitors (Table I, column 2) and to form a distributed low-voltage side (Table I, column 4), for example by placing several components in parallel. Some papers suggest increasing the inherent resonance frequency $f_{\mathrm{res}}$ of the divider (Table I, column 3), but this approach leads to lower voltage division factors [21]. Several papers also emphasize the importance of placing the low-voltage side inside a shielded chamber, connected to earth (Table I, column 2). In terms of performance, the bandwidths of the designed dividers fall within the range of tens of megahertz. The highest reported bandwidth is 1.62 GHz, but is associated with a relatively low voltage division factor and the experiments conducted with this divider do not exceed 2 kV. Most dividers have maximum voltages ranging from tens to hundreds of kilovolts. The highest voltage division factor achieved is 120,000 and is obtained with a 2-stage voltage division. This means that a second voltage division with a factor of 2 is performed by matching the impedance of the cable connecting the divider to the measurement device, with the input impedance of the measurement device itself.

This work introduces, for the first time, the inclusion of a mutual inductance between the high-voltage and low-voltage arms into the physical model of capacitive dividers. Based on the mathematical analysis of this enhanced physical model, a design rule is established, stating that minimizing both the self inductance and the mutual inductance of the divider is essential to reduce parasitic oscillations. This requirement can be met by using coaxial symmetry for the return path for the current in the low-voltage side. It is important to note that the coaxial symmetry discussed in this paper differs from the coaxial shape of so-called coaxial capacitive dividers [14] in which the entire structure is coaxial for compactness and design simplicity. The divider designed by Wang *et al.* [17] appears to follow the design rule suggested in the present work, although their paper does not explicitly mention mutual inductance.

The design rule established in this paper can be implemented on any capacitive divider by placing the low-voltage side PCB inside a coaxial cable, between the central conductor and the grounded shield. In this work, it is implemented on a custom-built capacitive divider, specifically designed to measure the output voltage generated by a spiral generator, a compact and lightweight family of pulse generators. Since the pulses of interest generated by such generators exhibit an oscillating behavior [22], it is crucial to minimize the parasitic oscillations without relying on post-processing filtering techniques which might also distort the useful oscillations. The resulting design can withstand pulses up to at least 500 kV, with a bandwidth of 17 MHz. It incorporates a highly compact low-voltage arm and allows for easy adjustment of the voltage division factor $K$ of the divider, with values exceeding 100,000.

This paper is an extended version of a conference paper presented at the IEEE International Conference on High-Voltage Engineering and Applications (ICHVE 2024) [23]. In the conference paper, the design rule was only stated, with experimental validation as the sole evidence. In the present paper, the mathematical developments leading to the design rule are presented in detail. Additionally, this work provides a more comprehensive description of the custom-built divider, providing the required characteristics it must fulfill and the methods used to achieve them.

## II. THEORY

### A. Ideal Capacitive Divider

An ideal capacitive divider is shown in Fig. 1(a). In this circuit, $C_{\mathrm{HV}}$ represents the equivalent capacitance of the high-voltage arm, and $C_{\mathrm{LV}}$ the equivalent capacitance of the low-voltage arm. Analyzing this circuit without parasitic elements, a simple and well-known transfer function relating the output voltage $V_{LV}$ to the input voltage $V_{HV}$ is obtained:

$$V_{\mathrm{LV}} = \frac{C_{\mathrm{HV}}}{C_{\mathrm{LV}} + C_{\mathrm{HV}}} V_{\mathrm{HV}} = \frac{1}{K} V_{\mathrm{HV}}. \tag{1}$$

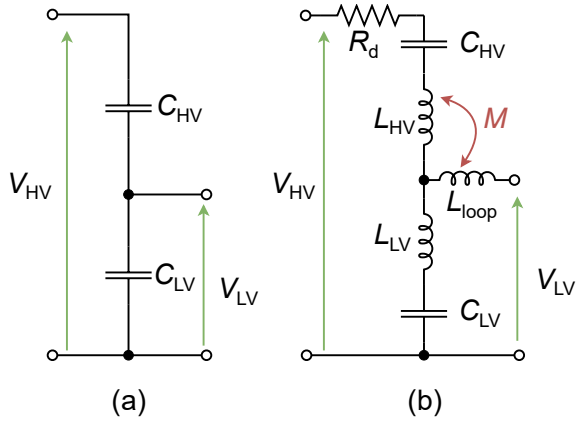


Fig. 1. Equivalent circuits of a capacitive divider. (a) Ideal. (b) With parasitic elements.

In this equation, $K$ is known as the voltage division factor.

### B. Modeling Parasitic Oscillations

In a real experimental design, parasitic elements are always present and must be considered when modeling a capacitive divider. Fig. 1(b) illustrates an equivalent circuit of a real capacitive divider. In addition to the equivalent capacitances, this model also contains several self inductances: $L_{\mathrm{HV}}$ the equivalent inductance of the connections of the high-voltage arm, $L_{\mathrm{LV}}$ the parasitic self inductance of the components used in the low-voltage arm and $L_{\mathrm{loop}}$ the inductance of the loop formed by the connections linking the low-voltage side to a measurement device. Unlike existing models of capacitive dividers, our work also considers the parasitic mutual inductance $M$ between the high-voltage and the low-voltage arm of the divider. This parameter accounts for the fact that when the high-voltage pulse is applied, the current flowing through the high-voltage arm generates a magnetic field that can induce a parasitic current in the low-voltage arm. The resistance $R_{\mathrm{d}}$ is not a parasitic element, but is intentionally added as a damping resistor, a well-known component used to reduce parasitic oscillations [20].

Solving this circuit in the Laplace domain yields the following transfer function for the divider:

$$H(s) = \frac{V_{\mathrm{LV}}(s)}{V_{\mathrm{HV}}(s)} = \frac{1}{K}\,\frac{s^2 C_{\mathrm{LV}}\left(L_{\mathrm{LV}}+M\right)+1}{s^2 C_{\mathrm{eq}} L_{\mathrm{eq}} + s R_{\mathrm{d}} C_{\mathrm{eq}} + 1}. \tag{2}$$

In this equation, $K$ is the voltage division factor of an ideal capacitive divider, $C_{\mathrm{eq}} = \frac{C_{\mathrm{HV}} C_{\mathrm{LV}}}{C_{\mathrm{HV}}+C_{\mathrm{LV}}}$ represents the expression of the two capacitors $C_{\mathrm{HV}}$ and $C_{\mathrm{LV}}$ connected in series, and $L_{\mathrm{eq}} = L_{\mathrm{HV}} + L_{\mathrm{LV}}$ represents the expression of the two inductances $L_{\mathrm{HV}}$ and $L_{\mathrm{LV}}$ connected in series.

### C. Analytical Results for a Voltage Ramp

Thanks to the damping resistance $R_{\mathrm{d}}$, the parasitic oscillations are expected to only occur at the beginning of the edge of the applied pulse, *i.e.*, at a moment where the rise is almost linear. It is therefore relevant to analyze the response of the transfer function (2) when a voltage ramp is applied as input stimulus $V_{\mathrm{HV}}(t) = \alpha t$. This corresponds in the Laplace domain to $V_{\mathrm{HV}}(s) = \alpha/s^2$. Defining $\omega = \left(\frac{1}{L_{\mathrm{eq}} C_{\mathrm{eq}}} - \frac{R_{\mathrm{d}}^2}{4L_{\mathrm{eq}}^2}\right)^{\frac{1}{2}}$ as the classical pulsating frequency and $\tau = \frac{2L_{\mathrm{eq}}}{R_{\mathrm{d}}}$ as the characteristic damping time associated with the underdamped resonating RLC circuits formed by $L_{\mathrm{eq}}$, $C_{\mathrm{eq}}$ and $R_{\mathrm{d}}$, it is then possible to perform the inverse Laplace transform. Doing so results in the following expression:

$$\begin{aligned} V_{\mathrm{LV}}(t) = {} & \frac{\alpha t}{K} \\ & + \frac{1}{K}\left\{ \frac{C_{\mathrm{eq}} R_{\mathrm{d}}^2 + 2L_{\mathrm{eq}}}{\sqrt{4\frac{L_{\mathrm{eq}}}{C_{\mathrm{eq}}} - R_{\mathrm{d}}^2}} \sin(\omega t) e^{\frac{-t}{\tau}} \right. \\ & \left. \qquad + C_{\mathrm{eq}} R_{\mathrm{d}} \left( \cos(\omega t) e^{\frac{-t}{\tau}} - 1 \right) \right\} \\ & + \frac{2\alpha\left(L_{\mathrm{LV}}+M\right)}{\sqrt{4\frac{L_{\mathrm{eq}}}{C_{\mathrm{eq}}} - R_{\mathrm{d}}^2}} \sin(\omega t) e^{\frac{-t}{\tau}}. \end{aligned} \tag{3}$$

The first term of this expression is the ideal output of the voltage divider and the other terms correspond to the parasitic voltage, which will be denoted $V_{\mathrm{par}}$. Notably, among these terms, only one component of $V_{\mathrm{par}}$ is not divided by the voltage division factor $K$. Since this paper focuses on high values of $K$ (as the goal is to measure high-voltage pulses), the parasitic voltage can be simplified by removing the terms proportional to $\frac{1}{K}$. It leads to the following expression:

$$V_{\mathrm{par}} \simeq \frac{2\alpha\left(L_{\mathrm{LV}}+M\right)}{\sqrt{4\frac{L_{\mathrm{eq}}}{C_{\mathrm{eq}}} - R_{\mathrm{d}}^2}} \sin(\omega t) e^{\frac{-t}{\tau}}. \tag{4}$$

Fig. 2 illustrates the time evolution of analytical results for a realistic capacitive divider with a voltage division factor $K$ = 10,000. The dashed curve corresponds to the ideal output voltage assuming no parasitic elements. The solid light red curve shows the response when the full expression (3) is considered, while the dashed blue curve represents the simplified parasitic term (4). The close overlap of the two parasitic curves validates the simplified expression of $V_{\mathrm{par}}$.

The simplified parasitic term is proportional to the term $L_{\mathrm{LV}} + M$. Based on this result, the design rule to reduce parasitic oscillations in a voltage divider is as follows: the low-voltage arm must be designed to minimize both the self inductance and the mutual inductance.

### D. Simulation of a 1.2/50 µs Lightning Impulse Signal

The design rule, analytically derived for a linear voltage, is now tested on a more realistic signal: a 1.2/50 µs lightning impulse (LI) signal (IEC 61000-4-5). This corresponds to the type of signals that will be used in the experimental validation of the design rule. Fig. 3 illustrates the response of the simulated capacitive divider using the transfer function (2) when the input stimulus is a 1.2/50 µs lightning impulse signal. Fig. 3(a) shows that decreasing the value of the self inductance of the low-voltage arm results in reduced parasitic

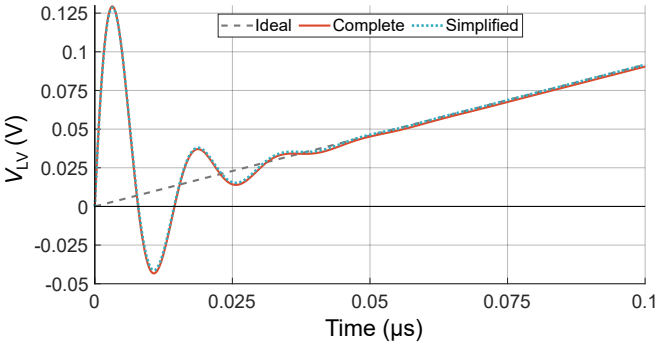


Fig. 2. Simulation of a capacitive divider with a voltage division factor $K$ = 10,000 when the input stimulus is a voltage ramp.

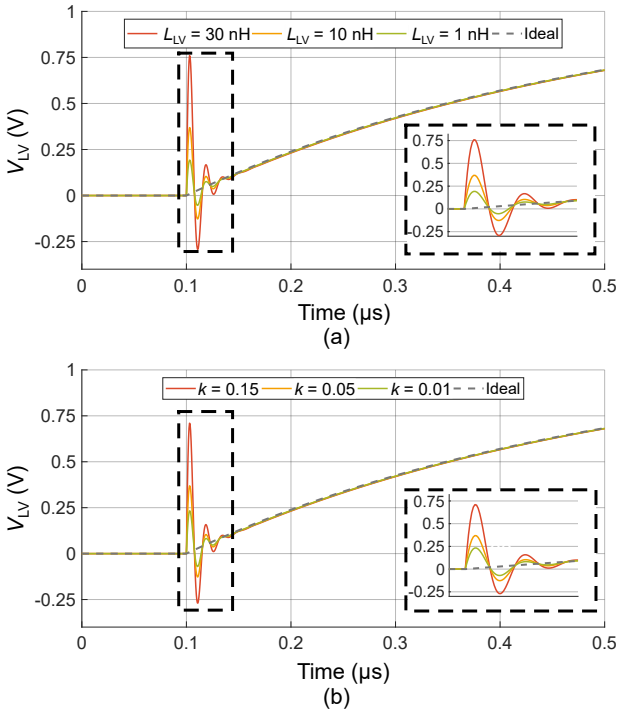


Fig. 3. Simulated output of a capacitive divider when the input signal is a 1.2/50 µs lightning impulse signal. (a) Modification of the self inductance $L_{\mathrm{LV}}$ of the low-voltage arm. (b) Modification of the mutual inductance $M$ between high-voltage and low-voltage arms.

oscillations superimposed to the LI signal. Fig. 3(b) shows the evolution of the output voltage of the capacitive divider for various values of the dimensionless coupling coefficient $k$ between the high-voltage side and the low-voltage side, defined such that $M = k\sqrt{L_{\mathrm{HV}} L_{\mathrm{loop}}}$. The results confirm that lower values of $k$ result in a reduction of parasitic oscillations, reinforcing that the design rule remains valid for LI signals.

## III. Design of the Capacitive Divider

The design rule established in Section II is now applied to the development of a custom-built capacitive divider. Although this design rule can be implemented on any design of capacitive dividers, in this study, the capacitive divider is specifically intended for measuring the output voltage generated by spiral generators, a family of compact pulse generators. To be compatible for this type of pulse generators, the capacitive divider must meet the following characteristics:

- The pulse generated by spiral generators can reach several hundreds of kilovolts [24]. Therefore, the high-voltage arm must withstand at least 500 kV without experiencing a dielectric breakdown.
- Considering a maximum voltage of 500 kV, in order to be able to observe the signals on a standard oscilloscope, the voltage division factor of the divider should be greater than 20,000.
- The rise time $t_{\mathrm{rise}}$ of the pulses is in the order of 100 ns [25]. Defining an equivalent frequency $f_{\mathrm{eq}} = 0.35\, t_{\mathrm{rise}}^{-1}$, the divider must maintain a flat bandwidth up to at least 3.5 MHz.
- The output capacitance of spiral generators is typically in the range of tens of picofarads [26]. To prevent significant alteration of the generated pulse, the equivalent input capacitance must be below 10 pF.

The following two sections detail the design of the capacitive divider, ensuring that it meets the required characteristics while minimizing parasitic oscillations by respecting the theoretical design rule established earlier.

### A. High-Voltage Arm

While the design rule for minimizing parasitic oscillations primarily applies to the design of the low-voltage arm, the design of the high-voltage arm will be briefly outlined in this section to provide an overall view of the custom-built capacitive divider. Appendix A provides additional details on the design of the high-voltage arm.

The high-voltage arm of the divider is schematically shown in Fig. 4. It consists of a stack of three stainless steel spheres, positioned inside a cylinder cast in polyurethane (PU) resin. The top sphere has a diameter of 80 mm, while the two bottom ones have diameters of 50 mm. The spheres are placed 40 mm apart. The PU cylinder is placed inside a tank filled with high-voltage insulating oil. The tank is housed inside a cubic Faraday cage with a side length of 2 m.

The dimensions are obtained following a design procedure proposed by Pecqois *et al.* [15]. The procedure combines finite element method (FEM) simulations and SPICE simulations. A first FEM simulation is used to retrieve the capacitance between the different spheres and between the sphere and earth. These capacitances are then used in a SPICE simulation that allows to determine (i) the bandwidth of the divider, (ii) the equivalent input capacitance, and (iii) the voltage distribution across the different spheres. The voltage distribution is then used in a second FEM simulation to find the electric field distribution when an input voltage of 500 kV is applied to the divider. Comparing the electric field distribution with the dielectric strength of the PU resin and the insulating oil, it is possible to assess whether the divider can withstand the applied pulse.

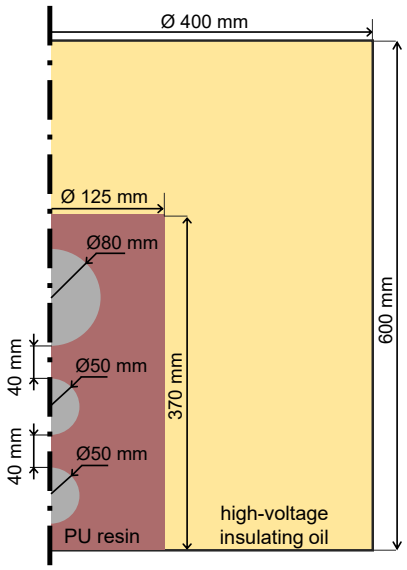


Fig. 4. Axisymmetric cross-sectional view of the high-voltage capacitor. The red area represents polyurethane resin and the yellow area represents high-voltage insulating oil. For improved visibility, this view is not up to scale.

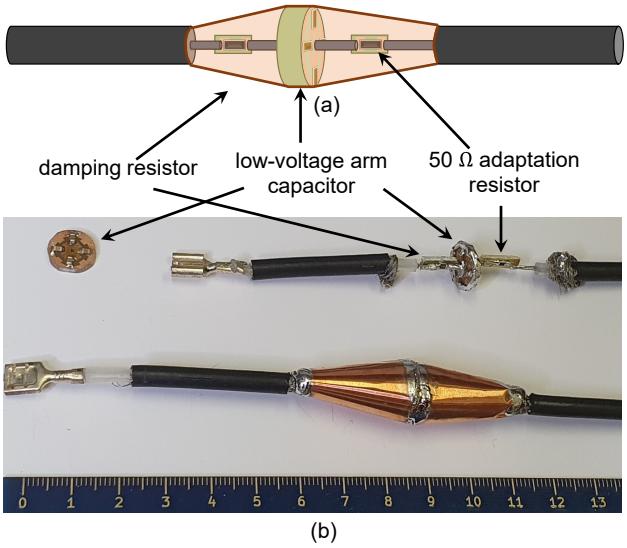


Fig. 5. (a) Schematic of the low-voltage part of the voltage divider. (b) Photograph showing the individual components of the low-voltage section and, at the bottom, the fully assembled low-voltage side embedded inside a coaxial cable.

The equivalent circuit used for the SPICE simulations, and the FEM simulations are provided in Appendix A. The results indicate that the upper frequency limit of the divider is 17 MHz, and that it has an input capacitance of about 11.5 pF. While it is slightly above the required threshold, it remains acceptable. In terms of dielectric breakdown, FEM simulations show that the divider, with the dimensions shown in Fig. 4, can withstand voltages up to at least 500 kV.

### B. Low-Voltage Arm

The low-voltage arm of the divider is responsible for setting the value of the voltage division factor $K$. Since the geometry of the high-voltage arm is fixed, $C_{\mathrm{HV}}$ has a constant value and the components in the low-voltage arm are used to adjust $C_{\mathrm{LV}}$, hence tuning $K$. The design rule of minimizing the sum of $L_{\mathrm{LV}}$ and $M$ is specifically implemented in this section of the divider.

First, to minimize the self inductance of the low-voltage arm, the design employs several SMD components connected in parallel, as recommended in the literature. Second, to minimize the mutual inductance $M$ between both arms of the divider, the part not previously mentioned in the literature, a coaxial symmetry of the low-voltage arm is employed. Using a coaxial return path for the current is known to result in an almost zero mutual inductance with any neighboring element [27].

The design of the low-voltage arm is shown in Fig. 5, both schematically and with photographs. It consists of a circular printed circuit board (PCB) that can accommodate up to 8 SMD capacitors (package type 0805), which are distributed radially in parallel. All these capacitors in parallel form the equivalent capacitor $C_{\mathrm{LV}}$. The coaxial symmetry is achieved by placing the PCB between the central conductor and the shield of an RG-58 coaxial cable. In addition to this array of capacitors, the low-voltage arm also includes an SMD 50 Ω resistor (package type 0805) for matching the impedance of the coaxial cable, as well as an SMD damping resistor $R_{\mathrm{d}} = 470\ \Omega$ (package type 0805) to decrease the time constant associated with the parasitic oscillations.

The direct integration of the components of the low-voltage arm into the coaxial cable brings another major advantage of the design proposed in this work: the low-voltage arm is extremely compact, as it simply consists of a short coaxial cable that connects the high-voltage arm to the measurement device. This means that the voltage division factor of the divider can be easily changed by replacing the cable, with other values of the capacitors, between the low extremity of the high-voltage arm and the oscilloscope. In this work, several low-voltage side coaxial cables were constructed, with voltage division factors ranging from approximately 5,000 to about 100,000.

## IV. Experiment

### A. Validation of the Design Rule

To experimentally validate the design rule established analytically in Section II, the design of the low-voltage arm is modified in two ways: (i) varying $L_{\mathrm{LV}}$ without changing $M$ and (ii) varying $M$ without changing $L_{\mathrm{LV}}$. In both cases, the amplitude of the parasitic oscillations is measured to confirm that a reduction in $L_{\mathrm{LV}}$ or a reduction of $M$ indeed reduces the amplitude of the parasitic oscillations.

To change the self inductance $L_{\mathrm{LV}}$ without affecting $M$, the number of capacitors placed in parallel on the low-voltage side PCB is varied between 1 and 8. The process for changing the mutual inductance $M$ without changing $L_{\mathrm{LV}}$ is shown

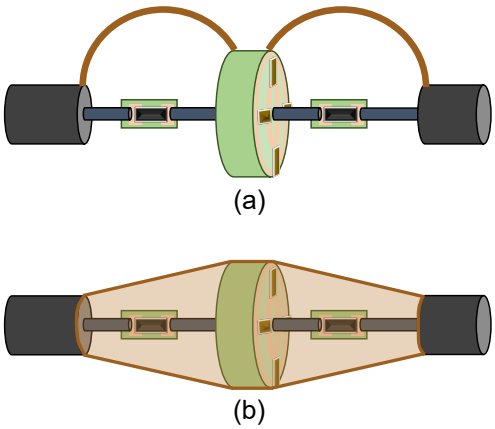


Fig. 6. Geometries of the low-voltage arm of the divider used to assess the effect of changing the mutual inductance $M$. (a) Single-wire return path for the current. (b) Coaxial return path for the current.

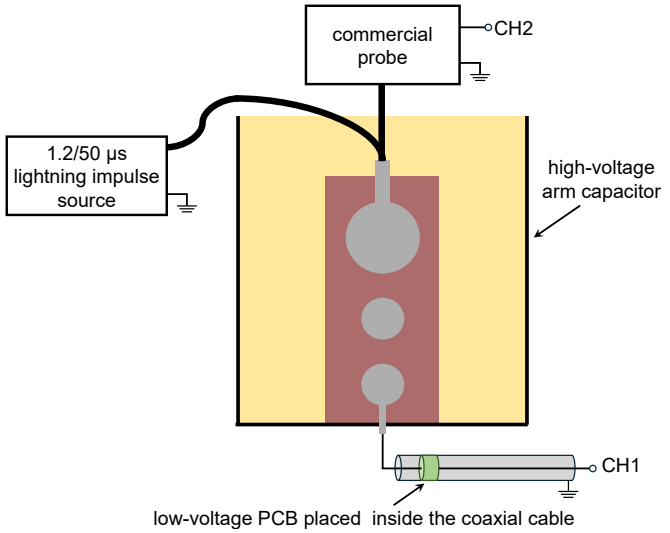


Fig. 7. Schematic diagram of the calibration procedure of the capacitive voltage using a 1.2/50 µs lightning impulse source and a commercial probe.

in Fig. 6. First, a single wire is used for the return path for the current. This wire forms a loop that can pick up parasitic magnetic flux, resulting in a non-zero mutual inductance $M$. Second, the coaxial geometry proposed in Section III-B is used, which eliminates the mutual inductance, resulting in $M \simeq 0$. In both geometries, the number of capacitors or the way they are placed on the PCB is left unchanged, resulting in a similar value of $L_{\mathrm{LV}}$.

The signal applied to the input of the capacitive divider is a 1.2/50 µs lightning impulse signal generated by a Passoni Villa® GTP-32 voltage source. A numerical high-pass filter ($f_{\mathrm{c}} = 5$ MHz) is applied to the measured signal to remove the useful signal, leaving only the parasitic voltage. This enables the quantification of the amplitude of the parasitic oscillations caused by the self-resonance of the divider when the input stimulus is applied. Two sets of 20 measurements are performed: one with a 10 kV amplitude of the LI source, and one with a 20 kV amplitude.

### B. Calibration of the Capacitive Divider

Before using the voltage divider to measure unknown voltage signals in real case applications, it is necessary to calibrate the voltage division factors associated with each PCB. To do this, the voltage divider is compared with a measurement obtained using a Tektronix® P6015a commercial probe (40 kV, 70 MHz, $K_{\mathrm{probe}}$ = 1,000±3%) for measuring $U_{\mathrm{LI}}$, the output voltage generated by a Passoni Villa® GTP-32 1.2/50 µs lightning impulse voltage source. The calibration setup is shown schematically in Fig. 7. Both the custom-built capacitive divider and the commercial probe are connected simultaneously at the output of the 1.2/50 µs lightning impulse source to ensure that it is always connected to the same equivalent load. The output signals from each measurement device are recorded with a Tektronix® TDS2204B oscilloscope (200 MHz, 2 Gsample/s, 1 MΩ ±1% // 13 pF ± 1.5 pF).

By comparing the signal obtained with the Tektronix® probe, which is known to be $U_{\mathrm{probe}} = U_{\mathrm{LI}}/K_{\mathrm{probe}}$, and the signal measured at the output of the capacitive divider $U_{\mathrm{divider}}$ with a given low-voltage capacitor, one can determine the value of the voltage division factor $K$ obtained with that specific low-voltage capacitor, *i.e.*:

$$K = \frac{U_{\mathrm{probe}} K_{\mathrm{probe}}}{U_{\mathrm{divider}}}. \tag{5}$$

The uncertainty in $K$ resulting from this calibration procedure is assessed in accordance with the Guide to the Expression of Uncertainty in Measurement (GUM) [28]. It corresponds to a Type B evaluation, derived from the specifications provided in the datasheets: 3% for the commercial probe and 2% for the oscilloscope. The standard uncertainties associated with these values are used to calculate a combined standard uncertainty. Multiplying this combined standard uncertainty by a coverage factor of $k$ = 2 (corresponding to a 95% confidence level) results in an expanded uncertainty of ±4.8%. It is important to note that the uncertainty value is not linked to the design rule presented in the paper, but rather to the uncertainty associated with the devices used during the calibration process.

### C. Spiral Generator

Once the various low-voltage side cables are calibrated, the divider is used to measure the output pulse generated by a spiral generator. Such a generator consists of a pair of conductors, separated by dielectric layers that are wound into a spiral of $N$ turns. The input voltage $U_{\mathrm{in}}$ is connected to a switch, which closes after the spiral is fully charged with a DC voltage $U_0$. The closing of the switch results in a transient over-voltage $U_{\mathrm{out}}$ at the other extremity of the spiral. This over-voltage has amplitudes that markedly exceed $U_0$ and is the pulse of interest [29]. Fig. 8(a) illustrates a schematic top view of a spiral generator, and Fig. 8(b) shows the schematic input and output voltage signals of such a generator. The aperiodic oscillating nature of the output voltage pulse

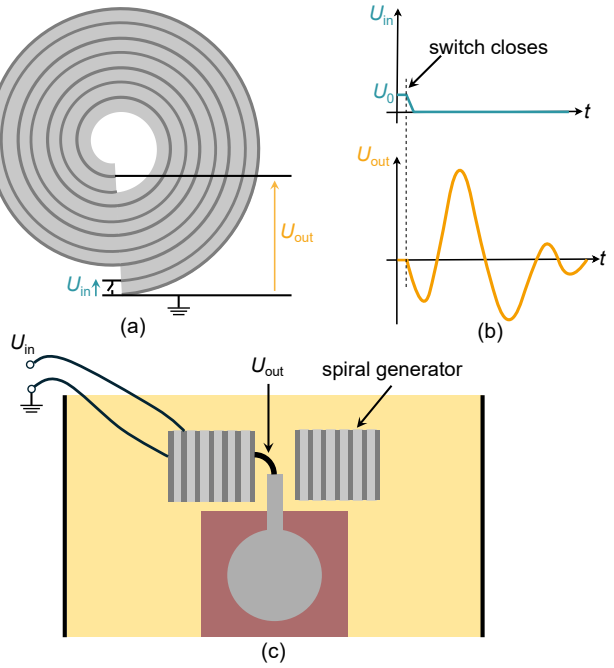


Fig. 8. (a) Schematic top view of a spiral generator. Dark gray areas represent conducting layers, while light gray areas represent dielectric layers. (b) Typical input and output waveforms of spiral generators. (c) Schematic cross-sectional view of the connections between the spiral generator and the capacitive divider.

makes it crucial to minimize parasitic oscillations, as certain signal processing techniques that would be performed is post-processing could distort the useful oscillations.

The spiral generator used in this study has $N = 70$ turns, an inner diameter of 70 mm, and an outer diameter of 140 mm. The input DC voltage $U_0$ applied to the generator is $U_0 = 7.4$ kV. Fig. 8(c) shows a schematic lateral cross-sectional view of how a spiral generator is connected to the divider. Due to the compact nature of these generators, they can be placed very close to the divider. This means that the cable connecting the output of the generator to the divider is only a few centimeters long. Therefore, when measuring the signal generated by a spiral generator, the inductance $L_{\mathrm{HV}}$ is reduced compared to the case where the voltage divider is used to measure the voltage generated by the LI voltage source.

## V. Results

### A. Validation of the Design Rule

*1) Measured Waveforms:* In this section, we present the experimental results regarding the effect of $L_{\mathrm{LV}}$ and $M$ on the amplitude of the parasitic oscillations observed when measuring a LI signal. Fig. 9 shows a superposition of the traces obtained while measuring a 10 kV lightning pulse signal using the capacitive divider with a low-voltage arm having a calibrated voltage division factor of 21,400. The red trace corresponds to the measurement when a single wire is used as the return path for the current, while the blue trace is obtained with a coaxial return path for the current with a single capacitor placed in the circular PCB of the low-voltage

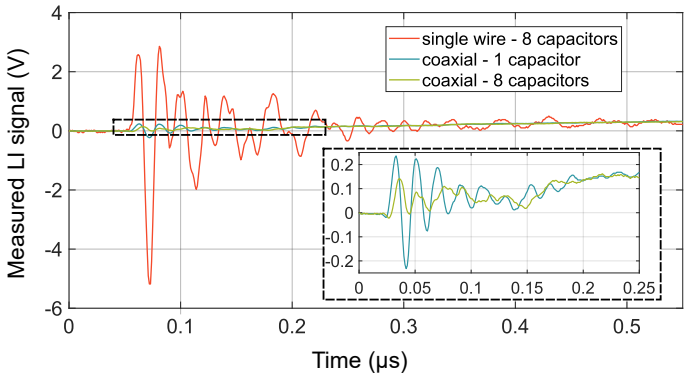


Fig. 9. Superposition of the traces obtained when measuring a 10 kV lightning impulse voltage with the capacitive divider with a voltage division factor of 21,400 for various configurations of the low-voltage arm PCB.

arm. The green curve is obtained with a coaxial return path for the current, and 8 capacitors evenly distributed on the circular PCB.

When a single wire is used as the return path for the current, the parasitic oscillations reach a peak-to-peak amplitude of approximately 10 V, which significantly exceeds the expected peak amplitude of the measurement of 0.47 V (*i.e.*, 10 kV divided by the calibrated voltage division factor of 21,400). Using a coaxial symmetry for the return path for the current significantly reduces parasitic oscillations. In both the blue and green curves, the amplitude of these parasitic oscillations remains below 0.25 V, as illustrated by the inset in Fig. 9, which provides a zoom on the rising edge of the blue and green curves. The inset also demonstrates that increasing the number of capacitors placed on the circular PCB from 1 to 8 further decreases the amplitude of the parasitic oscillations. Similar trends were observed for the other tested voltage division factors.

*2) Bar Plot of the Entire Study:* While Fig. 9 illustrates a specific example of the type of waveforms measured, Fig. 10 presents a bar plot summarizing the peak-to-peak amplitudes of the parasitic signals with and without coaxial symmetry (effect of $M$), and for 1, 4, and 8 capacitors in parallel on the PCB (effect of $L_{\mathrm{LV}}$). Each plot contains two bars: one for the measurement of 10 kV LI signals and another for the measurements of 20 kV LI signals. Each bar represents the result of 20 measurements. To illustrate the variability of the measurements, each bar is accompanied by an error bar representing the standard deviation calculated from the set of measurements. It can be directly observed that, regardless of the number of capacitors, the bars on the right, corresponding to a negligible mutual inductance, have an amplitude approximately one order of magnitude lower than those on the left.

Then, in terms of the number of capacitors, it appears that when a single wire is used as the return path for the current, the number of capacitors does not play a significant role. In

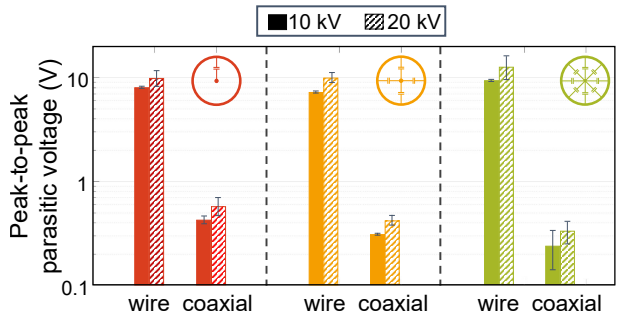


Fig. 10. Bar plot of the measured peak-to-peak amplitude of the parasitic oscillations obtained on lightning impulse signals for different configurations of low-voltage arm PCB and for two input voltages.

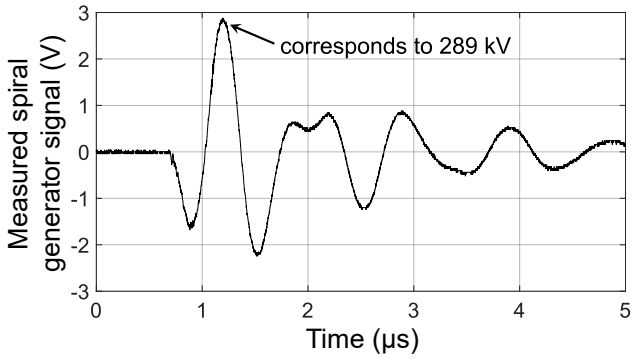


Fig. 11. Measurement of a pulse generated by a spiral generator with a voltage division $K$ = 102,000.

contrast, when a coaxial geometry is used for the return path for the current, the amplitude of the parasitic oscillations exhibits a monotonic decrease with the number of capacitors.

Finally, it can be observed that the evolution of the amplitude of the parasitic voltage follows a similar trend whether the input voltage is 10 kV or 20 kV.

These results provide experimental validation for the design rule proposed in this paper. While the importance of $L_{\mathrm{LV}}$ is well known, the importance of minimizing $M$ is, to the best of the authors' knowledge, not documented in the literature. The results presented in this section demonstrate that the mutual inductance $M$ plays a more significant role than the self inductance in influencing the amplitude of the parasitic oscillations. Note that without stating it explicitly, the divider designed by Wang *et al.* [17] appears to follow the design rule described in our work: in this paper, the return path for the current is optimized to reduce the self inductance of the low-voltage side. Doing so actually also reduces the mutual inductance.

Even with the highest number of capacitors considered in this work and with a coaxial symmetry in the low-voltage arm, parasitic oscillations persist, as observed in the green curve of Fig. 9. Several possible explanations account for the existence of these oscillations. First, to obtain a simple analytical expression, the model used in this paper does not take into account the impedance of the measurement device connected to the input of the divider. Second, the design rule was derived from the simplified analytical expression (4) where some terms were omitted. In practice, these omitted terms exist and also contribute to parasitic oscillations. Third, the remaining oscillations could be attributed to the use of a one-meter-long cable required to connect the LI source to the divider, which may cause high-frequency reflections between the divider and the LI source. Finally, there are other sources of high-frequency interferences and parasitic oscillations not explored in this paper. For instance, Zhao *et al.* [30] suggest that the presence of the oscillations might also be explained by the interaction between the damping resistor $R_{\mathrm{d}}$ and the output resistance of the 1.2/50 μs lightning impulse source.

### *B. Measurement on a Spiral Generator*

The bespoke capacitive divider discussed in this work is designed to measure pulses generated by spiral generators. Fig. 11 displays the oscilloscope trace obtained when measuring the oscillating output voltage of the spiral generator presented in Section IV-C. The trace is obtained with a low-voltage arm of the divider which has a calibrated voltage division factor of 102,000. It should be noted that the principal oscillations shown in Fig. 11 are not parasitic, but represent the useful signal, as illustrated by the schematic spiral generator output signal shown in Fig. 8(b). The parasitic oscillations are the ones visible at the very start of the pulse, during the falling edge of the first peak. Despite the high voltage division factor, the signal-to-noise ratio remains high, as the parasitic oscillations are barely noticeable. The amplitude of the useful signal is between approximately 1 V and 3 V for the three first oscillations, while the maximum amplitude of the parasitic oscillations is around 200 mV. This suggests that the remaining oscillations present in the inset of Fig. 9 were likely caused by the one-meter-long cable that was needed to connect the 1.2/50 μs lightning impulse source to the capacitive divider. Reducing the inductance of the connections of the high-voltage side of the divider results in a lower mutual inductance, as $M = k\sqrt{L_{\mathrm{HV}} L_{\mathrm{loop}}}$ but also in a smaller characteristic damping time $\tau$. These considerations explain why decreasing $L_{\mathrm{HV}}$ when measuring a spiral generator output voltage leads to reduced parasitic oscillations compared to the measurement of a LI signal using the same capacitive divider.

The maximum amplitude of the signal is 2.84 V. This corresponds to a maximum amplitude of 289 kV when multiplied by the voltage division factor. The measurement data shown in Fig. 11 provides evidence that the bespoke capacitive divider can be used for the intended application of measuring output voltages with amplitudes of several hundreds of kilovolts generated by spiral generators, with parasitic oscillations that are barely noticeable, even with a high-voltage division factor exceeding 100,000.

## VI. Conclusion

This paper presents a new design rule for reducing parasitic oscillations superimposing to the useful signal of capacitive dividers. The design rule states that both the parasitic self inductances of the low-voltage arm and the mutual inductance between the high-voltage and low-voltage arms of the divider must be minimized to reduce the parasitic oscillations. The design rule is established analytically and validated through experiments on the measurement of LI signals.

The authors propose an easy way to implement the design rule by utilizing a coaxial symmetry for the return path for the current. This is achieved by embedding the low-voltage arm PCB between the central conductor and the shield of a coaxial cable. In addition to canceling the mutual inductance, this design also has the advantage of being highly compact and allowing easy adjustment of the voltage division of the divider.

A custom-built capacitive divider, designed for measuring pulses generated by spiral generators, is presented and used to experimentally validate the proposed design rule. Results indicate that employing a coaxial symmetry for the return path of the current reduces the amplitude of parasitic oscillations by approximately one order of magnitude. Further reduction can be achieved by using multiple SMD capacitors in parallel on the PCB to lower the self inductance. However, this additional reduction is less significant than that achieved by the coaxial symmetry. These findings suggest that the primary source of undesired oscillations is the presence of mutual inductance.

The capacitive divider designed in this paper has a bandwidth of 17 MHz, can withstand pulses up to at least 500 kV, and has an input capacitance of approximately 11.5 pF. It was used in practice to measure pulses up to 289 kV with a voltage division factor of 102,000 without any noticeable parasitic oscillations in the measured signal. Compared to other custom-built capacitive dividers in the literature, it demonstrates one of the highest voltage division ratios and maximum input voltage capabilities. While the bandwidth sets a limitation, it remains well-suited for the intended application and could be further optimized for scenarios requiring shorter rise times.

The design rule proposed in this paper can be applied to any capacitive divider, regardless of its intended application. While this study focuses on a divider designed for spiral generators, the findings contribute to a broader understanding of parasitic oscillations in capacitive dividers and enable more accurate measurements of high-voltage pulses across various applications without requiring any post-processing of the measured signal.

## Appendix

### A. Complete Design Procedure for the High-voltage Arm

As mentioned in Section III-A, the high-voltage arm follows the design steps proposed by Pecquois *et al.* [15],

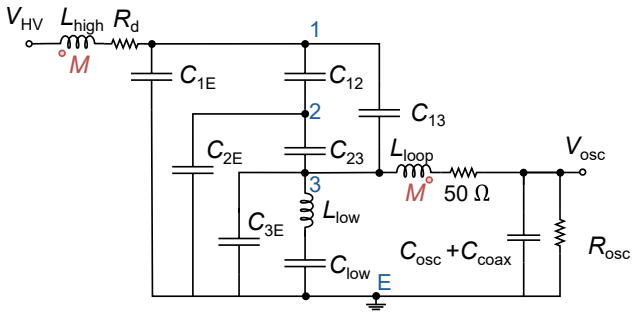


Fig. 12. Equivalent circuit solved in LTSPICE during the design of the high-voltage arm.

combining FEM and SPICE simulations (using the LTSPICE software). The complete circuit solved with SPICE is shown in Fig. 12. It contains the capacitances between the different stainless steel spheres $C_{\mathrm{ij}}$ and between the spheres and earth $C_{\mathrm{iE}}$, where $i = 1$ is the top sphere, $i = 2$ the middle sphere, $i = 3$ the bottom sphere and $E$ is earth. These capacitances were estimated using a FEM simulation with a Maxwell capacitance matrix [31]. The simulation also includes the equivalent capacitance of the low-voltage arm $C_{low}$. The parasitic elements of the high- and low-voltages sides of the divider $L_{\mathrm{high}}$ and $L_{\mathrm{low}}$, as well as the inductance of the loop connecting the divider to the oscilloscope, are also present in the equivalent circuit. $M = k\sqrt{L_{\mathrm{high}} L_{\mathrm{loop}}}$ is the mutual inductance between the high and low voltage side. Finally, it also contains the 50 Ω resistor for impedance matching, as well as the equivalent input impedance of the measurement device, which includes its resistor $R_{\mathrm{osc}}$, its capacitance $C_{\mathrm{osc}}$ and the capacitance of the cable $C_{\mathrm{coax}}$. The values of the different elements of the circuits are given in Table II and Table III.

The equivalent circuit used in the design of the high-voltage capacitor is more complex than the equivalent circuit used in Section II to establish the design rule. Appendix B shows how it is possible to retrieve the simple equivalent circuit of Fig. 1(b) starting from the complete circuit of Fig. 12.

TABLE II
Values of the Parameters of the High-Voltage Side of the Equivalent Circuit.

| Capacitance sphere-earth | Capacitance sphere-sphere | other |
|---|---|---|
| $C_{1E}$ = 8.02 pF | $C_{12}$ = 8.02 pF | $L_{\mathrm{high}}$ = 370 nH |
| $C_{2E}$ = 3.37 pF | $C_{23}$ = 2.55 pF | $R_{\mathrm{d}}$ = 470 Ω |
| $C_{3E}$ = 4.48 pF | $C_{13}$ = 1.15 pF | |

TABLE III
Values of the Parameters of the Low-Voltage Side of the Equivalent Circuit.

| Divider | Measurement device | |
|---|---|---|
| $C_{\mathrm{low}}$ = 21.3 nF | $L_{\mathrm{loop}}$ = 15 nH | $C_{\mathrm{coax}}$ = 100 pF |
| $L_{\mathrm{low}}$ = 5 nH | $k$ = 0.01 ($M$ = 0.47 nH) | $C_{\mathrm{osc}}$ = 13 pF |
| | | $R_{\mathrm{osc}}$ = 1 MΩ |

SPICE Simulations of this circuit show that the voltage gain remains constant up to nearly 5 MHz and the 3 dB frequency limit of the divider is reached at approximately 17 MHz. This circuit can also be used to estimate the input capacitance of the divider. This requires a simplification of the circuit, provided in Appendix B. By doing so, one obtains the estimated input capacitance of 11.5 pF.

In terms of dielectric breakdown of the divider, one can use the SPICE simulations to retrieve the potential at each node (1, 2, and 3) of the divider, corresponding to each sphere in the real device. This voltage distribution can then be used as boundary conditions of a FEM simulation to analyze the electric field distribution when a pulse of 500 kV is applied at the input of the divider. The datasheet for the PU resin [32] states that the DC dielectric strength is 20 kV/mm. This value is used as design criterion since it provides a worst-case scenario since the breakdown field is higher for short pulses than for DC voltages [33]. For the high-voltage insulating oil, the design can be validated using similar reasoning as the one used for the PU cylinder: compare the value of the electric field obtained by simulation with the dielectric strength at DC, which provides a lower bound on the dielectric strength for pulsed voltages. Considering oil that is less than half a year old, the dielectric breakdown voltage is about 30 kV for a 2.5 mm gap between two electrodes [34]. This corresponds to a breakdown voltage of 12 kV/mm.

Fig. 13 shows the electric field obtained from a FEM simulation when a 500 kV pulse is applied to the voltage divider. The left part of the figure shows the simulation results for both the PU cylinder and the tank filled with high-voltage insulating oil. The right part of the figure is a zoom of the transition between the PU cylinder and the oil, with an updated scale clamped at 6 kV/mm for improved visibility.In the left part of the figure, it can be seen that the maximum amplitude of the electric field is 11.5 kV/mm which is well below the DC breakdown field of 20 kV/mm. As for the oil, the right part of the figure shows that the maximum value is below 6 kV/mm in the oil, which, once again, is lower than the DC breakdown field.

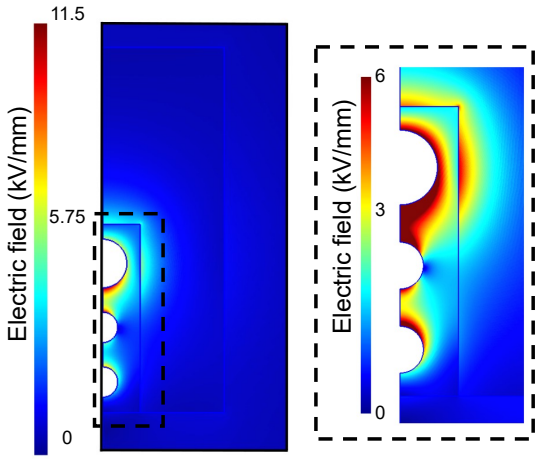


Fig. 13. Axisymmetric cross-sectional view of the electric field when a 500 kV voltage is applied at the high-voltage terminal of the divider. The right image is a zoom with an adjusted scale for the electric field value in the high-voltage insulating oil.

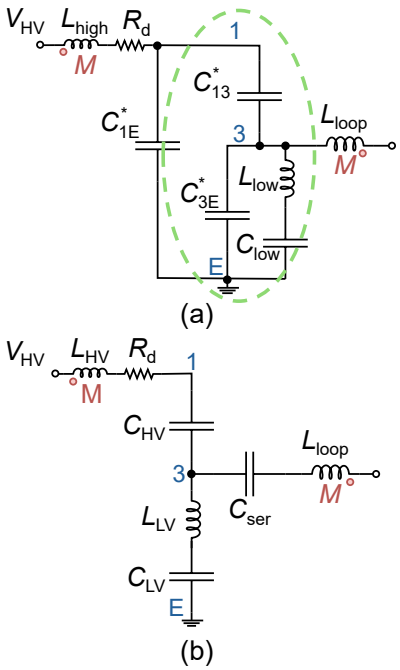


Fig. 14. Simplification of the entire circuit used for the LTSPICE after two successive Kennelly transformations. (a) Circuit after first Kennelly transformation. (b) Second after first Kennelly transformation.

## B. Re-obtaining the Simple Model

The design rule proposed in this paper was obtained for the circuit shown in Fig. 1(b). This section aims at showing that, under certain assumptions, it is possible to simplify the entire circuit of Fig. 12 used in the SPICE situations into a simpler, generic form of a damped capacitive divider with parasitic self and mutual inductances.

The Kennelly theorem can be used to transform a Y configuration of admittances into a $\Delta$ configuration of admittances connected to the same three nodes of a circuit as follows [35]:

$$Y_{\mathrm{ij}} = \frac{Y_{\mathrm{iT}} Y_{\mathrm{jT}}}{Y_{\mathrm{iT}} + Y_{\mathrm{jT}} + Y_{\mathrm{kT}}}. \tag{A1}$$

Similarly, it is possible to re-obtain the Y configuration using the following three relations (where $T$ is the central node):

$$Y_{\mathrm{iT}} = \frac{Y_{\mathrm{ij}} Y_{\mathrm{jk}} + Y_{\mathrm{ki}} Y_{\mathrm{ij}} + Y_{\mathrm{jk}} Y_{\mathrm{ki}}}{Y_{\mathrm{jk}}}. \tag{A2}$$

The same kind of expressions exist for impedances, but as the paper focuses on a capacitive divider, working with admittances renders the expressions directly applicable for capacitances.

By applying two successive Kennelly transformations to the complete circuit, it is possible to obtain the circuits shown in Fig. 14(a) and (b), respectively.

The first transformation for simplifying the equivalent circuit of Fig. 12 is a Y-$\Delta$ transformation for capacitances $C_{12}$, $C_{2\mathrm{E}}$, and $C_{23}$. Further neglecting the impedance of the coaxial cable, the matching resistance, and the input impedance of the oscilloscope results in the equivalent circuit shown in Fig. 14(a). In this circuit, one has:

$$C^*_{1\mathrm{E}} = C_{1\mathrm{E}} + \frac{C_{12}C_{2\mathrm{E}}}{C_{12}+C_{23}+C_{2\mathrm{E}}} \,(\simeq 9.3 \text{ pF}), \tag{A3}$$

$$C^*_{13} = C_{13} + \frac{C_{12}C_{23}}{C_{12}+C_{23}+C_{2\mathrm{E}}} \,(\simeq 2.11 \text{ pF}), \tag{A4}$$

$$C^*_{3\mathrm{E}} = C_{3\mathrm{E}} + \frac{C_{23}C_{2\mathrm{E}}}{C_{12}+C_{23}+C_{2\mathrm{E}}} \,(\simeq 5.38 \text{ pF}). \tag{A5}$$

The numerical values correspond to the divider designed in this paper. In each equation, the first term is the capacitor that was already in the circuit before applying the Kennelly transformation, and the second term is the capacitance introduced by the Kennelly transformation.

The interest of this circuit is that it allows the estimation of the equivalent input capacitance formed by the divider. The value of the input capacitance is given by all the capacitors located between node 1 and node $E$ in Fig. 14(a). The equivalent capacitance between node 3 and node $E$ is given by $C^*_{3\mathrm{E}}+C_{\mathrm{low}} \simeq C_{\mathrm{low}}$ because $C_{\mathrm{low}}$ is in the nanofarad range and $C^*_{3\mathrm{E}}$ in the picofarad range. This equivalent capacitance is connected in series with $C^*_{13}$ in the green ellipse drawn in Fig. 14(a). Since $C^*_{13}$ is also in the picofarad range, these two capacitors in series form an equivalent capacitance of the orange ellipse, which is close to $C^*_{13}$. Finally, the input capacitance of the voltage divider can be estimated to be close to $C^*_{1\mathrm{E}}+C^*_{13}$ as $C^*_{1\mathrm{E}}$ is in parallel with the green ellipse.

Before proceeding further with the second Kennelly transformation, another assumption is made. It is assumed that the impedance of $C_{\mathrm{low}}$ in series with $L_{\mathrm{low}}$ remains much smaller than the impedance of $C^*_{3\mathrm{E}}$, *i.e.*, $C^*_{3\mathrm{E}}$ is removed from the circuit. To determine under which conditions this assumption holds, the series connections of $C_{\mathrm{low}}$ and $L_{\mathrm{low}}$ is rewritten as an equivalent frequency-dependent capacitor whose capacitance is given by: $C_{\mathrm{low,eq}}(f) = C_{\mathrm{low}}\left(1-\frac{1}{(2\pi)^2 L_{\mathrm{low}}C_{\mathrm{low}}f^2}\right)$. Removing $C^*_{3\mathrm{E}}$ from the circuit is valid when $C^*_{3\mathrm{E}} \ll C_{\mathrm{low,eq}}(f)$. In this work, $C_{\mathrm{low}} \simeq 20$ nF, $L_{\mathrm{low}} \simeq 10$ nH and $C^*_{3\mathrm{E}} \simeq 10$ pF, the assumption holds for frequencies below approximately 10 MHz. As the frequency range of interest in this work is below 2.5 MHz, this assumption is valid.

The second Kennelly transform used to transform the circuit shown in Fig. 14(a) into the circuit shown in Fig. 14(b) is a $\Delta$-Y transformation of capacitors $C_{\mathrm{LV,eq}}(f)$, $C^*_{13}$ and $C^*_{1\mathrm{E}}$. Calling $T$ the new node appearing at the center of the Y configuration, the following three expressions are obtained :

$$C^*_{1\mathrm{T}} = \frac{C_{\mathrm{LV,eq}}(f)C^*_{13}+C_{\mathrm{LV,eq}}(f)C^*_{1\mathrm{E}}+C^*_{13}C^*_{1\mathrm{E}}}{C_{\mathrm{LV,eq}}(f)} \simeq C^*_{13}+C^*_{1\mathrm{E}}(=11.4\,\mathrm{pF}), \tag{A6}$$

$$C^*_{\mathrm{ET}} = \frac{C_{\mathrm{LV,eq}}(f)C^*_{13}+C_{\mathrm{LV,eq}}(f)C^*_{1\mathrm{E}}+C^*_{13}C^*_{1\mathrm{E}}}{C_{13,\mathrm{eq}}} \simeq \frac{C^*_{13}+C^*_{1E}}{C^*_{13}}\,C_{\mathrm{LV,eq}}(f), \tag{A7}$$

$$C^*_{3\mathrm{T}} = \frac{C_{\mathrm{LV,eq}}(f)C^*_{13}+C_{\mathrm{LV,eq}}(f)C^*_{1\mathrm{E}}+C^*_{13}C^*_{1\mathrm{E}}}{C^*_{1\mathrm{E}}} \simeq \frac{C^*_{13}+C^*_{1\mathrm{E}}}{C^*_{1\mathrm{E}}}\,C_{\mathrm{LV,eq}}(f). \tag{A8}$$

The major assumption in these terms is that: $C_{\mathrm{LV,eq}}(f)C^*_{13} + C_{\mathrm{LV,eq}}(f)C^*_{1\mathrm{E}} \ll C^*_{13}C^*_{1\mathrm{E}}$ which is, again, valid for frequencies below about 10 MHz.

It is still assumed that the impedance formed by the coaxial cable and the oscilloscope is higher impedance than the impedance of the equivalent capacitance $C^*_{\mathrm{ET}}(f)$, *i.e.*, the coaxial cable and the oscilloscope are removed from the circuit. It is therefore assumed that no current flows through capacitance $C^*_{3\mathrm{T}}$. One should note that capacitance $C^*_{3\mathrm{T}}$ is called $C_{\mathrm{ser}}$ in Fig. 14(b), as it is a capacitance that appears in series with the output. As no current flows in that branch when the impedance of the oscilloscope is neglected, this capacitor is removed to obtain Fig. 1(b).

Defining $\lambda = \frac{C^*_{13}+C^*_{1\mathrm{E}}}{C^*_{13}} (= 5.4)$, one obtains the equivalent circuit shown in Fig. 14(b), with:

$$C_{\mathrm{HV}} = C^*_{13} + C^*_{1\mathrm{E}} (\simeq 11.4 \text{ pF}), \tag{A9}$$

$$C_{\mathrm{LV}} = \lambda C_{\mathrm{low}} (\simeq 113.4 \text{ nF}), \tag{A10}$$

$$L_{\mathrm{LV}} = \frac{L_{\mathrm{low}}}{\lambda} (\simeq 1.8 \text{ nH}). \tag{A11}$$

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