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Mitigation of Interface Trap-Induced Bump Effects in p-Type MOS Capacitor

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Introduction: electronics for power applications in cryogenic environments

- Growing interest in superconducting systems
  - Electrical machines
  - Aerospace sector

- Need for electronic control

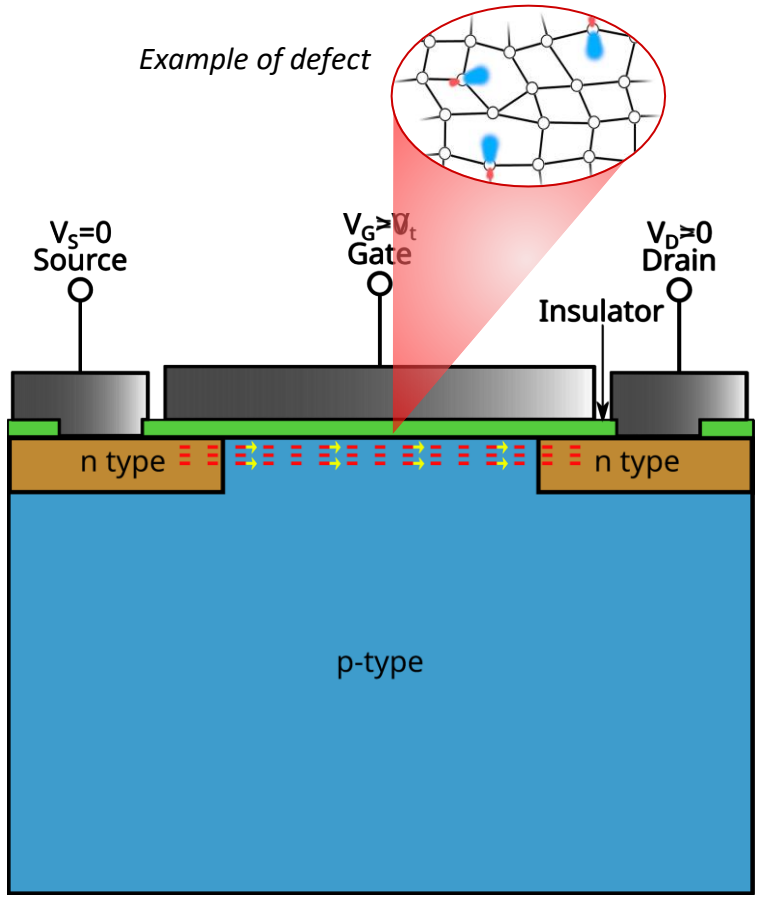
- Can we cool down the control electronics to gain in efficiency?
  - Can contribute to lower power dissipation
  - Smaller volume and weight

- Challenge for application
  - Important to understand the physical properties of power devices

Fundamental concepts of MOSFET

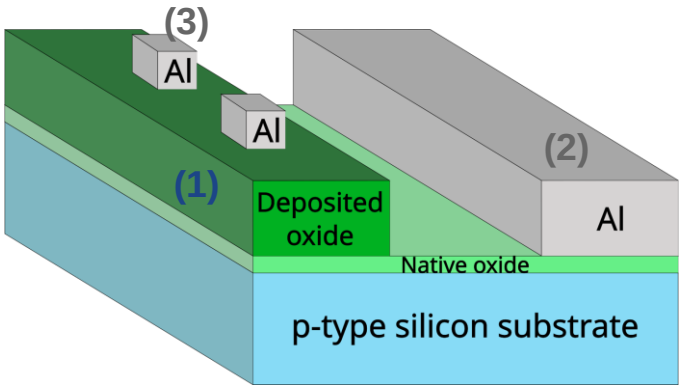
- $V_G = 0$
  Low conductivity between Source and Drain

- $V_G > V_t$
  Formation of conductive channel between Source and Drain
  - Related to the electrostatics of the MOS stack
  - Impacted by defects in the MOS stack



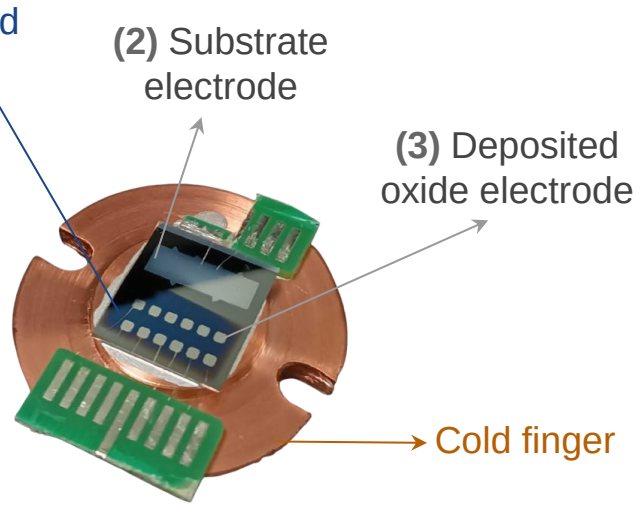
p type = holes as majority charge carriers
n type = electrons as majority charge carriers

Fabricated MOS capacitor for experimental studies



Design

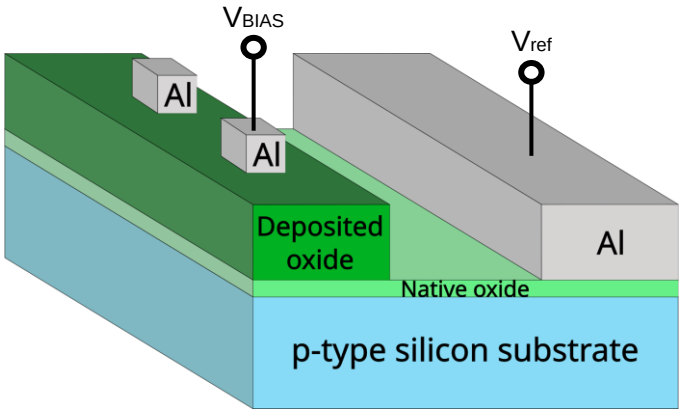
Fabrication

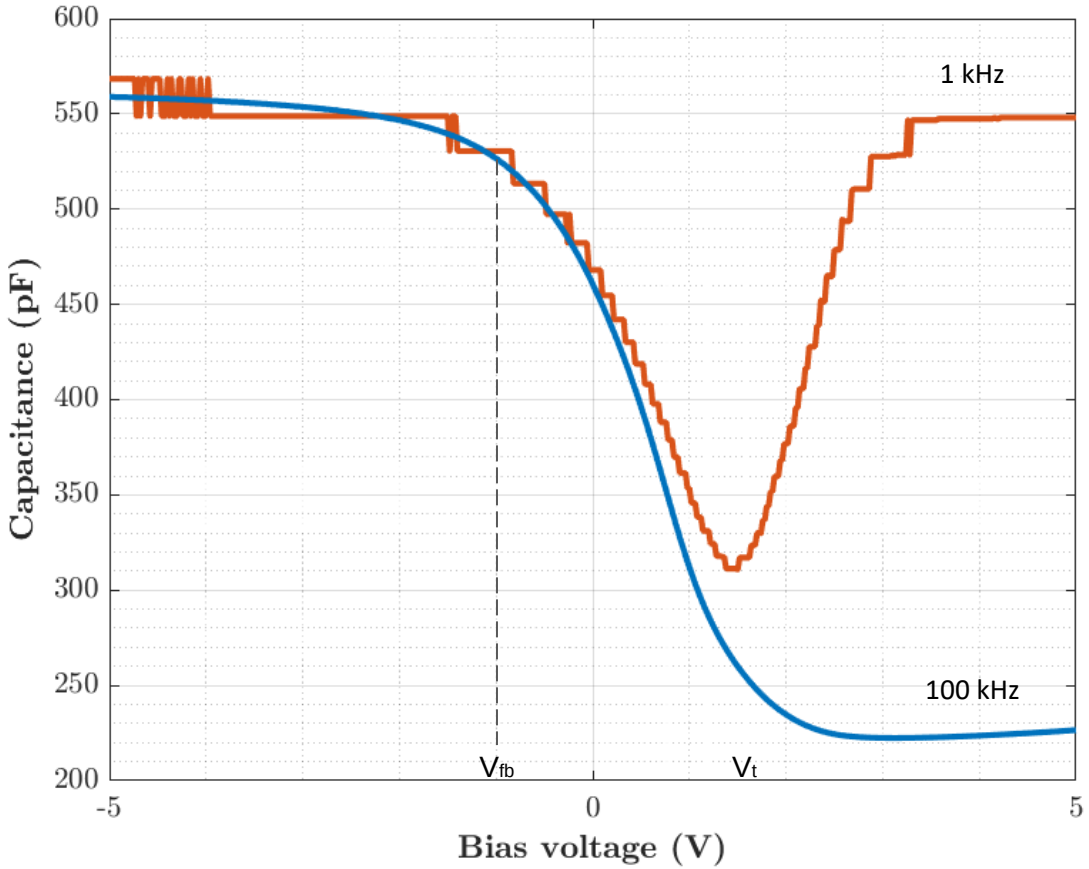


SiO_2 MOS capacitor structure designed on purpose with physical characteristics:

- Thickness (100 nm)
- Roughness (RMS = 0,2 nm)
- Stoichiometry (SiO_x)

Characteristic C-V curves

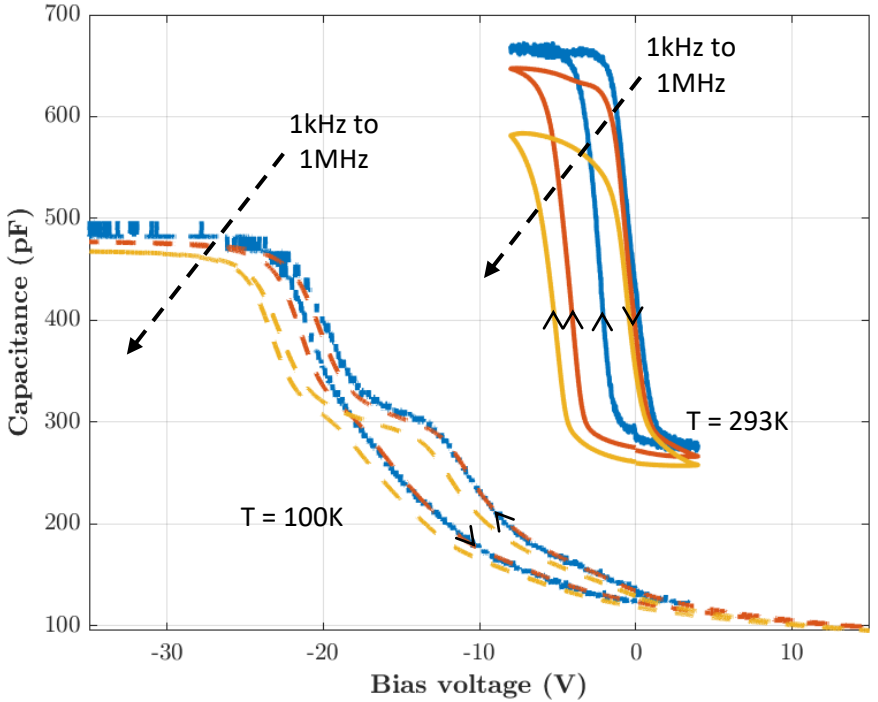




Results: C-V characteristics at room temperature and at 100K

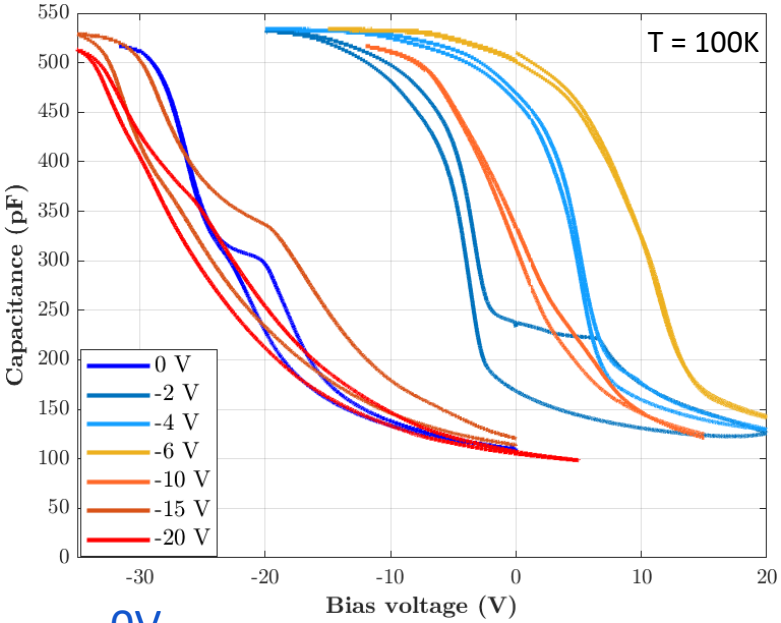
- **Trap-induced effects**
  - Hysteresis in Voltage Sweep
  - C(f) dispersion
  - Cryogenic behavior
    - Stretch-out effect
    - Bump effect

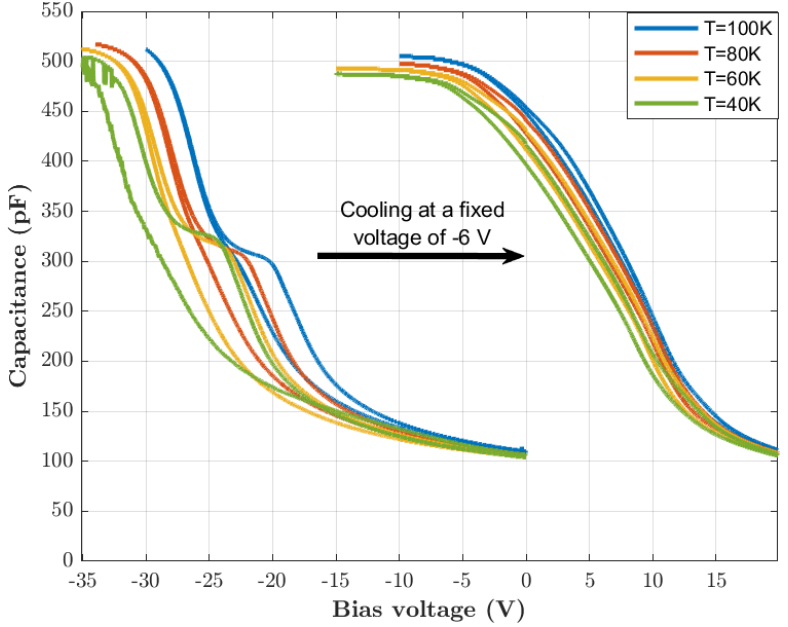
- **Classification of traps**
  - Fixed oxide charges
  - Oxide trap charges
  - Mobile ionic charges
    - $\Delta V_{fb}(V) > 0$ at accumulation
  - Interface trap charges
    - $\Delta V_{fb}(V) < 0$ at accumulation

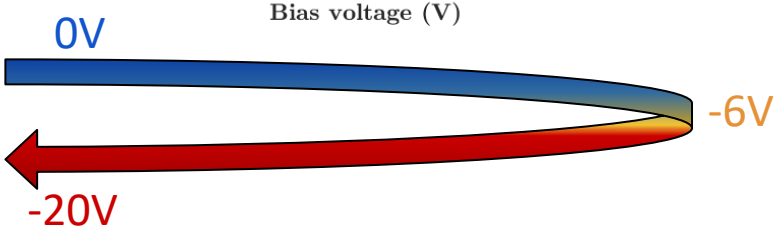


Bias voltage impact on trap states → Trap states impact ΔV_{fb} → T↓ Traps time constant↑

Results: impact of bias voltage while cooling the sample







Conclusion

To keep in mind

- Defects in MOS capacitors can greatly affect device performance
  - Instability effects may become more pronounced at low temperatures
- Applying a voltage bias to the device during the cooling phase can help improve the device response

Perspectives

- Investigation of the photoelectric response under illumination
- Extended physical-chemical characterisation of the MOS stack

Thank you for your attention!

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