Implementation and Validation of a Model Predictive Controller on a Lab-scale Three-Terminal MTDC Grid

Mohamed Moez Belhaouane, Khaled Almaksour, Lampros Papangelis, Oleg Gomozov, Frédéric Colas, Thibault Prévost, Xavier Guillaud and Thierry Van Cutsem

Abstract—In this paper, a reliable methodology is proposed in order to implement and validate a Model Predictive Control (MPC) scheme on an actual Voltage Source Converter (VSC) integrated in a scale-down multi-terminal DC grid. The objective of the investigated MPC controller is to enable AC frequency support among two asynchronous AC areas through a High Voltage Direct Current (HVDC) grid, while considering physical constraints, such as maximum and minimum DC voltage. A systematic and accurate implementation strategy is proposed, based mainly on the Hardware In the Loop (HIL) and Power Hardware In the Loop (PHIL), leading to the real-life testing on VSC, controlled by a classical microcontroller. The technical problems during the implementation process, as well as the proposed solutions, are described in detail through this paper. This procedure is deemed valuable to bridge the gap between offline simulation and the actual implementation of such advanced control scheme on experimental test rig.

Index Terms—Model Predictive Control, frequency support, Multi-terminal DC grid, HIL and PHIL, Experimental validation.

I. INTRODUCTION

THE shift to renewable energy production and the need to transfer bulk power over large distances has led to the development of HVDC systems [1]. The considered next step is the development of MTDC grids, for which VSC-HVDC is the most appropriate technology. The control of an MTDC grid is crucial for its correct operation and has received significant attention in the literature, e.g. in [2], [3], [4]. The advanced control flexibility offered by VSCs can be further exploited to provide ancillary services to the adjacent AC systems, such as power oscillation damping and frequency support [5]-[9]. The basic principle is to enable the VSCs to respond to AC frequency deviations by adjusting their power set-points, and thus, the power flowing through the MTDC grid [10]. Several methods have been proposed ranging from conventional control strategies, such as dual droop control

Mohamed Moez Belhaouane (Corresponding Author), Khaled Almaksour, Oleg Gomozov, Frédéric Colas and Xavier Guillaud are with Univ. Lille, Arts et Metiers Institute of Technology, Centrale Lille, Junia, ULR 2697 - L2EP, F-59000 Lille, France. (e-mails: mohamed-moez.belhaouane@centralelille.fr, khaled.almaksour@junia.com, Frederic.colas@ensam.eu, xavier.guillaud@centralelille.fr).

Lampros Papangelis is with Engie Impact, Brussels, Belgium (e-mail:lampros.papangelis@engie.com).

Thibault Prévost is with Réseau de Transport d'Electricite (RTE), Research and Development Dept. of RTE (e-mail: thibault.prevost@rte-france.com).

Thierry Van Cutsem is with Fund for Scientific Research (FNRS), University of Liège, Belgium (e-mail: t.vancutsem@uliege.be).

detailed in [11], to optimization-based ones [12]. In fact, the voltage-droop control technique ensures the reliable operation of the DC grid, while the frequency-droop control technique provides assistance to the interconnected AC grids. An ideal MTDC system should have both: a strong and reliable DC grid as well as a good support to the interconnected AC grids. However, this combination can be problematic since it degrades the performances of both the voltage droop and the frequency droop due to the contradiction of their objectives. In addition, the dual droop method suffers from the difficulty of respecting the constraints on DC voltages (i.e., risk of disrupting the operation of the DC grid) and powers (i.e., risk of reaching the limits of converter). Therefore, in order to achieve a better compromise between the frequency support and DC voltage regulation, while respecting the constraints and without disturbing the DC grid stability, Model Predictive Control (MPC) is an interesting option [13]. Its application to MTDC systems has been proposed and tested in offline simulation in [12]. In addition, these references have also demonstrated the usefulness of using MPC to support the AC grid frequency through MTDC system based on VSC [14]-[17].

When dealing with control algorithms testing and implementation, a full hardware simulation of the actual controller is hard to set up. This is particularly the case when an advanced control scheme is considered. In addition, some approximations are usually made, such as, the use of average models to represent the VSCs, which could decrease the accuracy of the obtained results. In the context of AC/DC systems, the implementation and testing of a control strategy for primary frequency regulation on a physical VSC, integrated into a real MTDC system has been little investigated in the literature. On the other hand, it is clear that conducting an experimental study on a real high-voltage power system is impossible. Instead, the Power Hardware In the Loop (PHIL) concept is an attractive alternative to increase the accuracy of the simulation, while providing experimental validation of the control strategies [18], [19].

Initial results were obtained in the context of the European Project Twenties [20]. Similarly, the dual droop control proposed in [5] was also validated in [21] using a scaled-down MTDC grid. Nevertheless, the focus in the literature has been on the experimental validation of conventional control strategies using cascade PI Controllers. The validation of more advanced and complex optimization-based control methods,

such as MPC, has not been investigated yet, in spite of promising results such those reported in [22], [23]. It should be underlined that all the cited works above rely on the three phases two-level VSC topology using average and switching model. However, some work attempts have considered the Modular Multilevel Converter (MMC), c.f., [24], [25]. In fact, regarding the frequency support between asynchronous AC systems through HVDC link, the MMCs behavior would be similar to a 2 Level PWM VSC. This claim was demonstrated by Hani Saad et al., in [26]. It was proved that using an Average Value Model (AVM) of MMC (Model Type 4) leads to the same behavior as 2-Level VSC when the converter is in normal operation. AC system dynamics can be accurately represented.

In this paper, a step-by-step methodology to conduct the experimental PHIL validation of the MPC-based frequency support scheme described in [12] is proposed. The procedure involves the implementation of a local MPC-based control in a conventional hardware development board (namely a classical micro-controller from Texas Instruments) of a VSC. The implementation of this type of control algorithm using a simple micro-controller revealed to be rather challenging. The use of a micro-controller as control hardware target instead of the FPGA (Field-Programmable Gate Array) technology is more suitable for iterative numerical optimization algorithm, requires shorter development for advanced control techniques and is cost-effective for the prototyping and research.

This paper is first focused on the hardware implementation of the MPC in a conventional hardware development 32-bit DSP micro controller. Two main technical problems have been identified and solved: the size of the optimization problem which may lead to computing time issues and the 32-bit floating-point precision available which may induce some errors in the solution of the optimization process. Such problems are presented in details, some solutions are proposed and implemented.

In second stage, the MPC is tested on a VSC embedded in a three-terminal MTDC setup in order to verify the validity of the proposed algorithm. Indeed, the experimental validation on a three-terminal MTDC setup, together with the verification of the physical constraints and the expected performances was the final challenge of this work. To carry out this purpose, a rigorous systematic procedure starting from the offline simulation and ending up in the experimental validation has been used to implement and test the MPC.

In this paper, a focus is proposed mainly on both HIL and PHIL steps as the offline and real-time simulation have already been discussed in [27]. According to the proposed accurate method, each validation step is described previously in [27] without details of technical problems. Nevertheless, the proposed work focus on the main issues related to the real-time operation of the advanced control strategy and the PHIL implementation complexity on a VSC controlled by a classical microcontroller.

The paper is organized as follows. Section II presents the studied MPC-based control strategy for AC frequency support. The first part of the third section gives a short description of the previously developed MPC-based algorithm that is going

to be implemented using HIL and PHIL approaches. In the second and third parts of Section III, the developed quadratic optimization solver at the heart of the MPC algorithm implementation is elaborated. The HIL and PHIL simulations of the MPC controller based on a small-scale MTDC setup as well as the experimental validation of the controller using PHIL, are reported in Section IV. Conclusions and future extensions are provided in Section V.

II. FREQUENCY SUPPORT SCHEME BASED ON MPC STRATEGY

A. Droop Control of VSC in a MTDC grid

In normal operation, within an MTDC grid, at least one VSC must participate in the power balancing in order to keep the DC grid stable. Droop control has been proposed in the literature [28] as a well-known strategy to control the VSC power without any internal communication inside the MTDC grid. It allows sharing the effort of restoring the power balance between several VSCs. The power P of VSC configured in droop control mode is adjusted according to the following characteristic (1).

$$P^{cmd} = P^{set} - K_v \left(V - V^{set} \right) \tag{1}$$

where P^{set} is the power reference, V^{set} the DC voltage reference and K_v is the droop gain. The control structure of a VSC is depicted with black colour in Fig. 1. The output of the droop controller P^{cmd}, along with the reactive power reference Q^{cmd}, are passed to the current controllers of the VSC. A Phase Locked Loop (PLL) is used to synchronize the VSC to the grid.
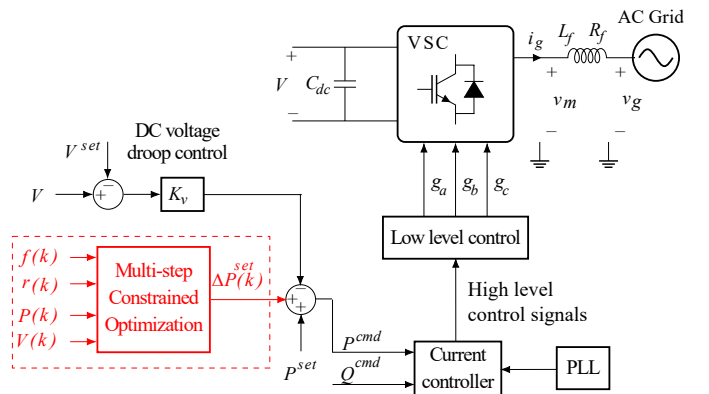

Fig. 1. Control structure of frequency support involving an optimization scheme

B. MPC based algorithm for frequency support

In this application, the MPC scheme proposed in [12] has been chosen for AC frequency support. It modifies the P^{cmd} reference by adding a ΔP^{set}, as shown in red colour in Fig. 1. The objective is to keep the AC frequency within secure limits while obeying physical constraints in the VSC. Internally, the controller relies on a simple model of the AC frequency and DC voltages evolutions. In the meantime, constraints on the VSC operation (i.e. voltage and power limits) are monitored and enforced if necessary.

MPC is suitable to solve this constrained optimization problem with anticipation capabilities over a prediction horizon. The prediction horizon has been chosen equal to the control horizon defined by N_c. This optimization relies on a model of the future system evolution. To that purpose, the controller collects at each discrete time k the following local measurements:

$P(k)$: the power calculated in AC side based on three phases voltages and currents;

$V(k)$: the measured voltage at its DC bus connexion;

$f(k)$: the frequency at its AC bus;

$r(k)$: the ROCOF (Rate of Change of Frequency).

Based on these measurements, the controller calculates at time k the control action $\Delta P^{set}(k+1)$ for the next time step by solving the following quadratic constraint optimization problem:

$$\min_{\Delta P^{set}, \epsilon, \zeta, V, P, f} w_1 . \sum_{j=0}^{N_c-1} \left[\Delta P^{set}(k+j)\right]^2 + \tag{2}$$

$$w_2 . \sum_{j=1}^{N_c} \epsilon^2(k+j) + w_3 . \sum_{j=1}^{N_c} \zeta^2(k+j)$$

Subject to the following linear constraints, for $j = 1, ..., N_c$:

$$\widehat{P}(k+j) = \widehat{P}(k+j-1) + \Delta P^{set}(k+j-1) - K_v\left(\widehat{V}(k+j) - \widehat{V}(k+j-1)\right) \tag{3}$$

$$\widehat{V}(k+j) = \widehat{V}(k+j-1) + s_v \Delta P^{set}(k+j-1) \tag{4}$$

$$\widehat{f}(k+j) = \widehat{f}(k+j-1) + r(k)T_s + \left[\widehat{P}(k) - \widehat{P}(k+j)\right]s_f T_s \tag{5}$$

$$V^{\min} - \epsilon(k+j) \le \widehat{V}(k+j) \le V^{\max} + \epsilon(k+j) \tag{6}$$

$$P^{\min} \le \widehat{P}(k+j) \le P^{\max} \tag{7}$$

$$f^{\min} - \zeta(k+j) \le \widehat{f}(k+j) \le f^{\max} + \zeta(k+j) \tag{8}$$

$$\epsilon(k+j), \zeta(k+j) \ge 0 \tag{9}$$

where $\widehat{P}(k+j)$, $\widehat{V}(k+j)$ and $\widehat{f}(k+j)$ are the predicted variables. N_c is the control horizon of MPC scheme, which has been chosen equal to the prediction horizon (i.e., $N_c=N_p$). The sample time of the controller is denoted as T_s, which point out the required time to update the output of optimal control scheme. The first term in the objective function (2) aims to minimize the total control effort. By minimizing the $\mathcal{L}_2$ norm, the overall control effort is distributed throughout the whole control horizon N_c and a smooth response is achieved. The last two terms in the objective function (2) allow to introduce two relaxation variables ϵ and ζ. The equality constraints (3)-(5) make up the prediction model on both AC and DC sides (i.e., MTDC grid and AC frequency response models). The model used for the DC grid is static, which is justified by the fast of action of power electronics compared to the sampling period of the discrete high-level controller. A simplified AC frequency model is used based on a extrapolation of the ROCOF. The parameter s_v is the sensitivity of DC voltage in response to control changes. Similarly, s_f is the expected change of

frequency in response to a VSC power change. Constraint (6) specifies that the DC voltage should remain within the security limits V^{min} and V^{max}. Similarly, constraint (7) specifies that the VSC power should be between the limits P^{min} and P^{max}, corresponding to the VSC rating. Constraint (8) aims at keeping the AC frequency inside the limits f^{min} and f^{max}. The non-negative slack variables ϵ, ζ are used to relax the voltage and frequency constraints in order to ensure feasibility of the optimization problem. Violations are kept as small as possible, by choosing large values for the weighting factors w_2 and w_3 in (2). By setting $w_2 >> w_3$, priority is given to satisfying the DC voltage constraint, which is critical to avoid VSC tripping or damage.

III. QUADRATIC OPTIMIZATION SOLVER FOR MPC ALGORITHM IMPLEMENTATION

A. MPC Scheme Hardware Implementation

In this section, the implementation of the proposed MPC strategy in a classical micro-controller is described. The chosen hardware is a TMS320F28379D, which is part of the C2000 family from Texas Instrument and is based on a dual-core architecture. The task distribution among the two cores is displayed in Fig.2. As shown, the MPC control algorithms and the low-level and high-level conventional controllers are handled separately. The first microcontroller core (i.e. CPU-1) is used for the classical inner and low level controls, whereas, the second core (i.e. CPU-2) is dedicated to MPC computation. The control action of the MPC (i.e. power set-point change) is calculated in CPU-2 and sent to CPU-1, in order to update the DC voltage droop power set-point.
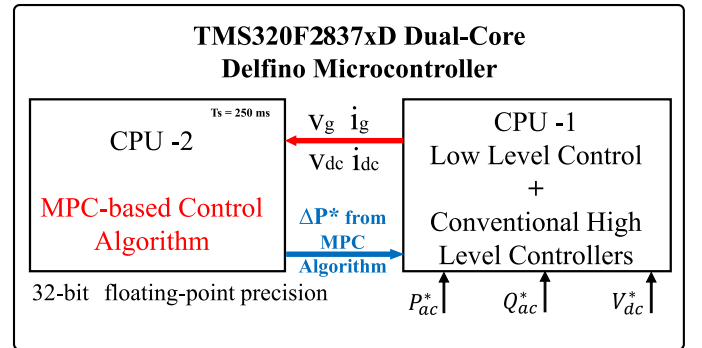

Fig. 2. Illustration of cores distribution inside the microcontroller.

As mentioned in Fig.2, 32-bit floating-point precision is used to implement the MPC scheme in order to use the inherent capability of the microcontroller. In addition, the computation times in both CPUs are not the same. The low-level and high-level control algorithms have sampling times below $100\,\mu s$. Solving the MPC optimization problem at the same sampling rate is impossible on this type of micro-controller. The targeted sampling time of the MPC part has been fixed to 250 ms in this application. The MPC is mainly focused on the frequency support, which is not extremely fast (generally the time response after an event is around 1 to 4 seconds). Updating the reference from the MPC output at a

time rate of 250 ms is a good value as it represents 4 to 16 faster than the frequency response.

B. Conception and development of the solver

The MPC formulation in Section II-B requires to solve a quadratic optimization problem (2) with linear constraints represented by (3)-(9). The optimization problem can be written in compact form as follows:

$$\min_{\boldsymbol{z}} \frac{1}{2}\boldsymbol{z}^T \boldsymbol{H} \boldsymbol{z} + \boldsymbol{h}^T \boldsymbol{z} \tag{10}$$

subject to:

$$\boldsymbol{C}_{ineq}\boldsymbol{z} - \boldsymbol{b}_{ineq} \leq \boldsymbol{0} \tag{11}$$

where $\boldsymbol{z}$ is the vector of decision variables, $\boldsymbol{H}$ is the Hessian matrix (or quadratic cost), and $\boldsymbol{h}$ is the linear cost. The matrix $\boldsymbol{C}_{ineq}$ and the vector $\boldsymbol{b}_{ineq}$ define the inequality constraints of the problem. In order to solve the performed optimization problem, a quadratic optimization solver is necessary. Aiming to reduce the complexity of the quadratic optimization algorithm and accelerate the solving of the convex optimization problem, only the inequalities constraints are taken into account (the equality constraints would be eliminated) as shown in (11). Thus, the developed quadratic optimization solver, detailed in the following, relies rigorously on the optimization problem (10)-(11). However, as shown in the sequel, the conception way of the solver where only the inequalities constraints are considered, guarantees the convergence towards the global optimum point. On the other hand, the main objective of this work is to implement the MPC algorithm in hardware targets (i.e., DSP - Digital Signal Processor), and interface them with real-time simulation tools. So, for technical compatibility reasons, it is important to design the quadratic optimization solver, in a way that will allow to ensure online optimization for experimental validation. Indeed, the development of the quadratic optimization solver as well as the MPC control scheme in the same framework by using C programming environment (an homogeneous development environment) allows to avoid the incompatibility problems that could come from the code generation, the acceleration of the code compilation on the hardware target and facilitate also the communication between the hardware controller and the real-time simulators during the HIL application. The adopted design is detailed in the following section.

If $\boldsymbol{H}$ is positive-definite and $\boldsymbol{C}_{ineq}$ define convex polytopes, the optimization problem is convex and can be solved using an interior point method [29] detailed in the following.

Classically, to solve (10) the augmented Lagrangian formulation is introduced:

$$L\left(\boldsymbol{z}, \boldsymbol{\lambda}, \boldsymbol{v}, \boldsymbol{s}\right) = \frac{1}{2}\boldsymbol{z}^T \boldsymbol{H} \boldsymbol{z} + \boldsymbol{h}^T \boldsymbol{z} + \boldsymbol{v}^T \left(\boldsymbol{C}_{ineq}\boldsymbol{z} - \boldsymbol{b}_{ineq} + \boldsymbol{s}\right) \tag{12}$$

where $\boldsymbol{v}$ represents the dual variables associated with the inequality constraints and $\boldsymbol{s}$ is the slack variable, also associated to the inequality constraints. $\boldsymbol{v}$ and $\boldsymbol{s}$ must be strictly positive and orthogonal. The optimal solution (z^*, v^*, s^*) is found by solving the equation $\dot{L}(\boldsymbol{z}, \boldsymbol{v}, \boldsymbol{s}) = 0$ (while holding the positivity and orthogonality conditions for $\boldsymbol{v}$ and $\boldsymbol{s}$). The

optimal solution can be found by solving the following system of equations:

$$\boldsymbol{H}\boldsymbol{z} + \boldsymbol{h} + \boldsymbol{C}_{ineq}^T\boldsymbol{v} = \boldsymbol{0} \tag{13}$$

$$\boldsymbol{C}_{ineq}\boldsymbol{z} - \boldsymbol{b}_{ineq} + \boldsymbol{s} = \boldsymbol{0} \tag{14}$$

$$\boldsymbol{v}^T\boldsymbol{s} = 0 \tag{15}$$

$$\boldsymbol{s} > \boldsymbol{0} \tag{16}$$

$$\boldsymbol{v} > \boldsymbol{0} \tag{17}$$

The Newton-Raphson method can be used to iteratively approach the solution:

$$\begin{vmatrix} \boldsymbol{H} & \boldsymbol{C}_{ineq}^T & \boldsymbol{0} \\ \boldsymbol{C}_{ineq} & \boldsymbol{0} & \boldsymbol{I} \\ \boldsymbol{0} & \boldsymbol{S} & \boldsymbol{\Lambda} \end{vmatrix} \begin{vmatrix} \Delta\boldsymbol{z} \\ \Delta\boldsymbol{v} \\ \Delta\boldsymbol{s} \end{vmatrix} = \begin{vmatrix} \boldsymbol{D} \\ -\boldsymbol{C}_{ineq}\boldsymbol{z} + \boldsymbol{b}_{ineq} \\ -\boldsymbol{v}^T\boldsymbol{s} \end{vmatrix} \tag{18}$$

where $\boldsymbol{D} = -\boldsymbol{H}\boldsymbol{z} - \boldsymbol{C}_{ineq}^T\boldsymbol{v}$ and $\boldsymbol{\Lambda} = diag(\boldsymbol{v})$, $\boldsymbol{S} = diag(\boldsymbol{s})$ are matrices with appropriate dimensions. A linear search must be performed at each iteration to ensure that the strict positivity constraints of $\boldsymbol{v}$ and $\boldsymbol{s}$ are held. If all the matrices on the left-hand side of (18) are constant, then this system can be further simplified into:

$$\left(\boldsymbol{H} + \boldsymbol{C}_{ineq}^T\boldsymbol{W}\boldsymbol{C}_{ineq}\right)\Delta\boldsymbol{z} = \boldsymbol{m}_1\left(\boldsymbol{z}, \boldsymbol{v}, \boldsymbol{s}\right) \tag{19}$$

$$\Delta\boldsymbol{v} = \boldsymbol{m}_2\left(\boldsymbol{z}, \boldsymbol{v}, \boldsymbol{s}\right) \tag{20}$$

$$\Delta\boldsymbol{s} = \boldsymbol{m}_3\left(\boldsymbol{z}, \boldsymbol{v}, \boldsymbol{s}\right) \tag{21}$$

Matrix $\boldsymbol{W} = \boldsymbol{S}\boldsymbol{\Lambda}^{-1}$ is a function of $\boldsymbol{v}$ and $\boldsymbol{s}$. Functions $\boldsymbol{m}_1$, $\boldsymbol{m}_2$ and $\boldsymbol{m}_3$ are linear and depend on $\boldsymbol{z}$, $\boldsymbol{v}$, $\boldsymbol{s}$ and $\boldsymbol{W}$ at the previous iteration. The sum $\left(\boldsymbol{H} + \boldsymbol{C}_{ineq}^T\boldsymbol{W}\boldsymbol{C}_{ineq}\right)$ is guaranteed to be positive-definite, symmetric and the system of equations can be solved using the LDL factorisation algorithm described, for instance in [30].

In order to solve the quadratic optimization problem, in the DSP, the algorithm has been implemented in C language using floating point operations and standard BLAS routine. The LDL factorisation and the solver of the linear system of equations are custom and based on the same linear algebra library. The solver is split into two steps:

1) Initialization of the optimization problem and generation of pre-computed matrices $\boldsymbol{H}$, $\boldsymbol{C_{ineq}}$ and linear functions $\boldsymbol{m}_1$, $\boldsymbol{m}_2$ and $\boldsymbol{m}_3$.
2) Real time control, where the pre-computed information is used to solve the optimization problem according to (19), (20) and (21).

The solver is expected to be efficient and the convergence to be fast compared to general-purpose convex optimization solvers thanks to offline pre-computing and capitalizing on the structure of the optimization problem. However, to further increase computational efficiency of the optimization solver and especially facilitate its hardware implementation, additional improvements have been performed, detailed in the next section.

C. Implementation process and optimization

1) MPC problem reformulation to reduce computational burden: While appropriate for off-line simulations [12], the initial formulation (2)-(9) involves quite a number of decision variables and constraints. Specifically, a control horizon

$N_c = 4$ results in a total of 18 decision variables and 42 constraints[1]. The complexity of the optimization problem increases significantly with the number of decision variables and constraints. It becomes difficult to solve such a problem in a conventional hardware equipment and to remain below a reasonable computation time of the controller (i.e. below 250 ms in our application). Therefore, the first step is to decrease the size of the problem by removing some variables and some constraints. This is achieved by expressing $\widehat{P}(k+j)$, $\widehat{V}(k+j)$ and $\widehat{f}(k+j)$ as a function of $\Delta P^{set}(k+j)$ using (3)-(5), and integrating the resulting expressions in (6)-(8), which leads to eliminating the equality constraints. This results in the following simplified formulation:

$$\min_{\Delta P^{set}, \epsilon, \zeta} w_1 . \sum_{j=0}^{N_c-1} \left[\Delta P^{set}(k+j) \right]^2 \\ + w_2 . \sum_{j=1}^{N_c} \epsilon^2(k+j) + w_3 . \sum_{j=1}^{N_c} \zeta^2(k+j) \tag{22}$$

subject to the following linear constraints, for j=1,..., N_c:

$$V^{\min} - \epsilon(k+j) \le \widehat{V}(k) + s_v \sum_{i=0}^{j-1} \Delta P^{set}(k+i) \\ \le V^{\max} + \epsilon(k+j) \tag{23}$$

$$P^{\min} \le \widehat{P}(k) - A \sum_{i=0}^{j-1} \Delta P^{set}(k+i) \le P^{\max} \tag{24}$$

$$f^{\min} - \zeta(k+j) \le \\ \widehat{f}(k) + T_s r(k) + A s_f T_s \sum_{i=0}^{j-1} (j-i) \Delta P^{set}(k+i) \quad (25) \\ \le f^{\max} + \zeta(k+j)$$

$$\epsilon(k+j), \ \zeta(k+j) \ge 0 \tag{26}$$

where $A = K_v s_v - 1$. For $N_c = 3$, the updated formulation results in a total of 9 decision variables and 24 constraints, reducing significantly the computational burden.

It is important to point out that there are few works in literature, that addressed the optimization issue of computational burden [25]. For instance, in [25], a Linear Time-Varying (LTV) strategy is proposed in order to reduce the burden of the optimization while retaining the main dynamics of the system, based only on offline simulation study. However, the proposed contribution relies on HIL and experimental PHIL implementations dealing with the required computation time, within the CPU of hardware target. The main proposed numerical improvements will be discussed in the following sections.

2) Numerical improvements based on error compensation:
An actual digital micro-controller is generally restricted in computational capacity. In our case, floating point operation are optimized for IEEE 32-bit format. Round-off error accumulation could easily lead to numerical issues when iterative algorithms are used. This is further problematic if the optimization problem to solve is not well-conditioned. A solution is to increase the variable precision using 64-bit instead of

[1]equality constraints are represented by two inequality ones

32-floating point arithmetic. However, this will dramatically increase the overall computation time. As an illustration, the chosen C2000 digital micro-controller can compute ten times faster if 32-floating point is used instead of 64-bit. Now, there are two critical features of the optimization algorithm that are impacted by computation accuracy.

The first one is linked to linear search step for variables update and the conditioning of the Hessian matrix. More precisely, the matrix $\boldsymbol{W} = \boldsymbol{S}\boldsymbol{\Lambda}^{-1}$ is involved in the Hessian matrix calculation and impacts the iterative update of the variables. At the optimum, the vectors $\boldsymbol{s}$ and $\boldsymbol{v}$ will contain some null elements corresponding to active and non-active constraint. Hence, near the optimal solution, the matrix $\boldsymbol{W}$ becomes ill-conditioned or even has infinite entries. To avoid this during the line search, step α is chosen to ensure (27) and (28).

$$\boldsymbol{v}_{k+1} = \boldsymbol{v}_k + \alpha \Delta \boldsymbol{v}_k \ge \delta \tag{27}$$
$$\boldsymbol{s}_{k+1} = \boldsymbol{s}_k + \alpha \Delta \boldsymbol{s}_k \ge \delta \tag{28}$$

were δ is some positive sufficiently small value to allow getting out from the Newton-Raphson iterations but sufficiently large to avoid infinite values in $\boldsymbol{W}$ matrix.

The second problem is associated with round-off error during the iterative update of the primal, dual and slack variables. This problem also shows up when approaching the optimum point laying on the constraint boundary and global unconstrained solution laying outside this boundary. Solving the system (19) will tend to move the optimization variables outside the feasible region, thereby, making some of $\boldsymbol{s}$ and $\boldsymbol{v}$ values negative. This is normally dealt by the line search but for some constraint configurations the current point will have to slide along the constraint boundary, leading to line search step α approaching zero value. If a dual or slack variable value is much larger than the line search step value, the numerical computation is rounded-off and the variable is stuck at the same value, as expressed by:

$$\boldsymbol{x}_{k+1} = \boldsymbol{x}_k + \alpha \Delta \boldsymbol{x}_k \tag{29}$$
$$If \quad \boldsymbol{x}_k \gg \alpha \Delta \boldsymbol{x}_k$$
$$then \ \boldsymbol{x}_{k+1} = \boldsymbol{x}_k \tag{30}$$

This leads to infinite iterations. In practice, the maximum value of iterations is limited, and the loop will be stopped prematurely, which leads to a suboptimal solution and a long optimization process. The algorithmic correction is as follows. The optimal solution can be represented as the sum of the initial value and all the line search steps performed during the iterations:

$$\boldsymbol{x}^* = \boldsymbol{x}_0 + \sum_{k=0}^{N^*} \alpha_k \Delta \boldsymbol{x}_k \tag{31}$$

To avoid the round-off errors, the Kahan summation algorithm [31] is used:

$$\boldsymbol{x}_{k+1} = \boldsymbol{x}_k + (\alpha_k \Delta \boldsymbol{x}_k - \boldsymbol{e}_k) \tag{32}$$
$$\boldsymbol{e}_{k+1} = \boldsymbol{e}_k + (\boldsymbol{x}_{k+1} - \boldsymbol{x}_k) - \alpha_k \Delta \boldsymbol{x}_k \tag{33}$$

Where $\boldsymbol{e}_k$ is the running summation error. Applying this algorithm to Newton-Raphson iterations means that in addition

to the dual and slack vectors $\boldsymbol{s}$ and $\boldsymbol{v}$ two corresponding running error vectors e_v and e_s must be updated and used during the variables step:

$$\boldsymbol{v}_{k+1} = \boldsymbol{v}_k + (\alpha_k \Delta \boldsymbol{v}_k - \boldsymbol{e}_{v|k}) \tag{34}$$

$$\boldsymbol{s}_{k+1} = \boldsymbol{s}_k + (\alpha_k \Delta \boldsymbol{s}_k - \boldsymbol{e}_{s|k}) \tag{35}$$

$$\boldsymbol{e}_{v|k+1} = \boldsymbol{e}_{v|k} + (\boldsymbol{v}_{k+1} - \boldsymbol{v}_k) - \alpha_k \Delta \boldsymbol{v}_k \tag{36}$$

$$\boldsymbol{e}_{s|k+1} = \boldsymbol{e}_{s|k} + (\boldsymbol{s}_{k+1} - \boldsymbol{s}_k) - \alpha_k \Delta \boldsymbol{s}_k \tag{37}$$

Appling this procedure also improves numerical performance by reducing the number of iterations required to reach the optimum.

IV. HIL AND PHIL IMPLEMENTATION OF MPC CONTROLLER

A. Description of the experimental setup and disturbance event

To support the validation of the tested MPC algorithm and its implementation, experimentations have been made on the actual setup. Real pictures of the actual experimental setup are depicted in Fig. 3 to highlight the different components of the Test-bed. Fig. 4 illustrates the three-terminals VSC-MTDC experimental setup and points out the PHIL test that will be discussed later. This experimental setup includes two main parts:

(i). The physical part is made up of a small-scale DC grid together with two actual 3 kW PWM (Pulse Width Modulation) VSCs (c.f., the middle of Fig. 4). The Fig. 3 details the hardware components as: The VSCs are 2-level converters with LCL filters and IGBT Switches, shown in Fig. 3-a and Fig. 3-c. The controller is implemented on a F28379D Dual core delfino micro-controller from Texas instrument. This micro-controller is connected through a field bus to a PLC which acts as a gateway to a SCADA system illustrated in Fig. 3-e. The VSC 1 and 2 are respectively connected through a power amplifier to AC grid 1 and 2 (c.f., Fig. 3-d). The cables used to represent the DC grid are a laboratory scale technology of the actual DC cables. The cables are kept on their cable drums to increase their linear inductance and boost the propagation speed, as shown in Fig. 3-b.

(ii). The virtual part is implemented in the real-time simulation environment using OPAL-RT real-time simulator (the OPAL-RT simulator is displayed in Fig. 3-f) with a $35\,\mu s$ as sampling time. The simulation area is highlighted with purple in Fig. 4. The simulated components correspond to an ideal AC source (infinite bus AC grid 1) and a small four-machine power Kundur system as an AC grid 2. This is the well-known Kundur power system, widely discussed in literature [32]). The AC grid 2 consists of two areas connected through two long AC lines. Each generator has a rating of 900 MVA. More details can be found in [20], [21]. The third station emulates the offshore station connected to the wind farm. Since the time lapse of this study is small, the power output of the wind farm can be supposed constant and VSC 3 acts like a constant power injector. The control systems of VSC 1 and 2 are configured in droop voltage control mode. In addition, VSC 2 is equipped with the previously described MPC to support the frequency of

AC grid 2. It should be noted that the AC grid 1 is considered as an infinite bus in order to simplify the interpretation of the obtained results. Therefore, no frequency deviation will take place in this grid, then the implementation of MPC on VSC 1 connected to infinite AC bus will react as a classical droop controller. Thus, only the VSC 2 is equipped with MPC. The MPC task is distributed with the same core distribution as described in Fig.2. The control parameters of the MPC algorithm are enumerated in Table I. The controller will start taking actions to support the AC frequency when the predicted frequency exceeds the under-frequency threshold f_{min}. The large weighting factors aim to keep both ϵ and ζ at small values. In addition, since the DC voltage constraint is critical (to avoid VSC tripping or damage), the weighting factors are chosen such that $w_2 > w_3 > w_1$. The considered event is the loss of the synchronous generator G4, which causes a significant frequency deviation in AC grid 2, thus triggering frequency support by VSC 2. The DC and AC operating points of the studied system are detailed in Tables II and III, respectively.
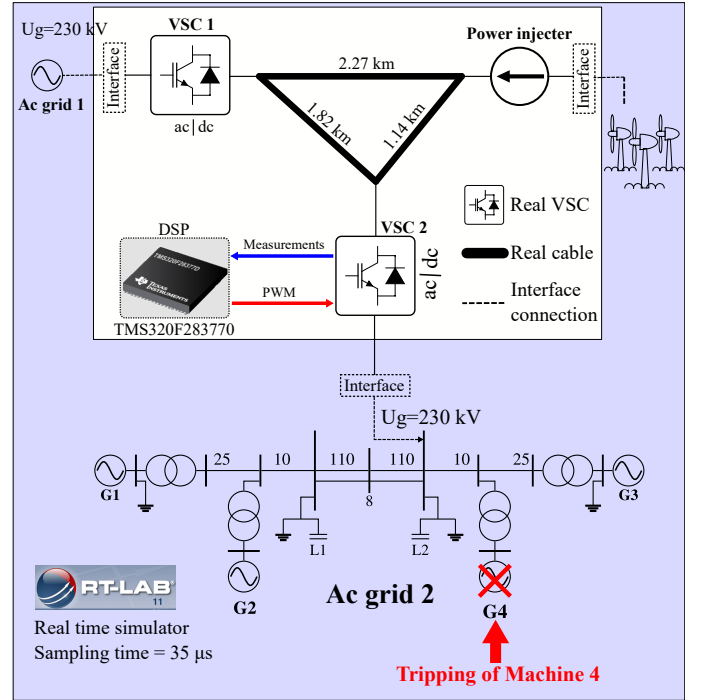

Fig. 4. Three terminals VSC-MTDC Setup.

TABLE I
CONTROL PARAMETERS OF MPC

P_{min} [p.u]	V_{min} [p.u]	f_{min} [p.u]	K_v [p.u]	s_v, s_f [p.u]
-1	0.9	0.995	0.82	0.4365, 0.0018
P_{max} [p.u]	V_{max} [p.u]	f_{max} [p.u]	K_f [p.u]	T_s [ms]
1	1.1	1.015	0.05	250
N_c	N_p	w_1	w_2	w_3
3	3	1	10^6	10^4

Fig. 3.   Actual experimental setup.

TABLE II
OPERATING POINT OF DC GRID

Converter	VSC1	VSC2	VSC3
DC Power [W]	1000	1000	-2100
DC Voltage [V]	400	400	400

TABLE III
OPERATING POINT OF AC GRID (4 MACHINE - KUNDUR POWER SYSTEM)

Machines	G1	G2	G3	G4
P_n [MW]	900	900	900	900
P [MW]	615	615	615	315
Droop [pu/pu]	—	0.04	0.04	—
Load [MW]	1463 (Area 1)	—	986 (Area 2)	—

B. HIL Validation

Before carrying out the MPC controller tests, some preliminary steps have been considered to validate the expected performance. The first step concerns the validation of the investigated controller using offline and full real-time simulations. This step has been detailed in [27]. A valuable additional step (particularly when non conventional control methods are used) consists of testing the MPC in a Hardware In the Loop (HIL) simulation. HIL simulation is a setup that prototypes the hardware of some part of a given system and emulates the rest while maintaining information exchange between these physical and virtual subsystems [33]. Figure 5 depicts the HIL configuration of the system described in Section IV-A.
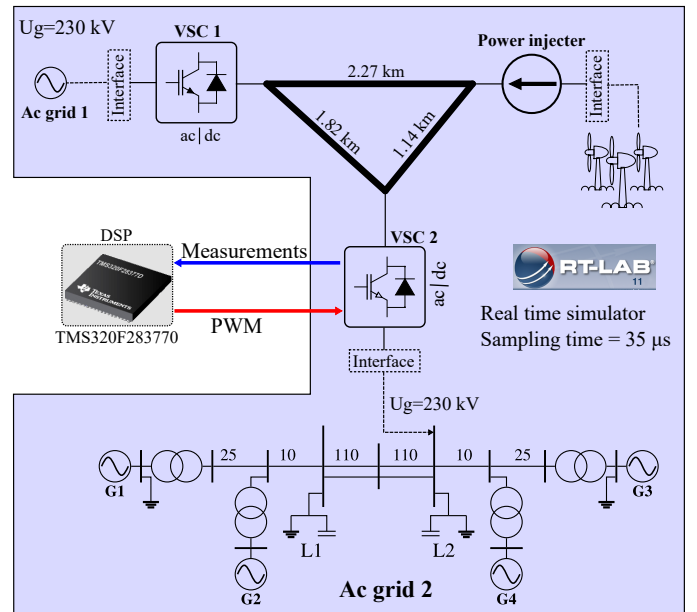

Fig. 5.   HIL simulation of the control system based on three terminal DC grid.

An RT-LAB environment is used to emulate the power system behaviour and the controller is linked to this emulated system through various inputs and outputs. The motivation of using HIL is to validate the control algorithm within hardware target and assess the interaction between the virtual and real parts in terms of communication and time delay. The AC grid 2 is simulated in real-time and detailed models of the VSCs are considered. It is of interest to mention that during HIL

tests, the first attempts to implement the MPC have failed to run with the chosen time step (i.e. 250 ms). This was the main reason that a simplification of the optimization problem described in Section III-C was needed. On the other hand, applying the optimization algorithm detailed in Section III-C enabled to calculate the optimal solution within the hardware target in a average time of 40 ms. The remaining time (i.e. 210 ms = 250 ms (time-step) - 40 ms (computation time)) has been considered large enough in case of a slower iterative execution of the optimization solver. The obtained HIL results are presented in Fig. 6. The rotor speed of machine G1, the generators active powers, the DC powers of VSC 1 and VSC 2 and the DC voltages at their respective DC buses are illustrated. The sudden event in AC grid 2 (i.e., tripping of Machine 4) corresponds at a loss of 252 MW, which must be compensated by the control systems relating to the production units and the converter connected to the perturbed AC grid. Only the generators G2 and G3 of Kundur power system participate to frequency regulation respect to 4% of frequency droop parameter. After the activation of the frequency support controller, VSC2 decreases its power (i.e., injects more power into the AC grid 2) to correct the frequency deviation. This is covered by VSC1, which increases its power (i.e. it draws more power from AC grid 1) under the effect of voltage droop control. It can be seen that the DC voltage at station 1 and 2 reach their minimal values, i.e., the constraints (DC voltage constraints) become active. One can notice, a small under-frequency below the minimal specified limit. Note that, the HIL test is performed using an instantaneous model of the VSC converter with a 10 kHz switching frequency of the PWM.

C. Validation on a Three-terminal MTDC Setup

As described in [20], [21], the test rig detailed in Fig. 4 mainly relies on the PHIL principle. A power amplifier is used to interconnect VSC2 to the real-time simulation of the 4-machine system of AC grid 2. A scaling gain has been used to adapt the interaction between software (high voltage simulated part) and hardware (scale-down DC grid) parts. In AC-PCC point of common coupling of VSC2, an AC power amplifier receives its AC voltage references from the real time simulation and generates the AC voltages on the power system. An appropriate scaling of the measured AC voltage from node 9 (high voltage simulated part) is carried out. In the same way, the current is measured in the AC side of physical VSC2 and sent back to the real-time simulator, and then, scaled in order to be injected in node 9 of the simulated AC grid 2 using controlled current sources. The same event as in Section IV.B is considered. The experimental results, shown in Figure 7, depict the rotor speed of machine G1, the DC powers of VSC 1 and VSC 2, the DC voltages in the MTDC grid and the active power of the remaining synchronous machines in AC grid 2 are illustrated in Fig.7. It can be verified that the HIL and PHIL results are quite similar which confirms the effectiveness of the step-by-step validation process. So, focus on the obtained results, mainly on the DC side, the transient and steady state behaviours (e.g.,frequency nadir around $49.51\,Hz$ and steady-state behaviour equal to $49.74\,Hz$) are quite similar and the

same expected performances are derived from both HIL and PHIL tests. Furthermore, the same physical interpretations as HIL results (c.f., Section IV.B) are obtained, which confirms the effectiveness of the proposed step-by-step strategy.

V. CONCLUSION

In this paper, a methodology to perform experimentations of an advanced controller based on a MPC algorithm has been proposed. The investigated advanced control approach allows the frequency support between asynchronous AC power systems through a High Voltage Direct Current grid. This kind of control is based on simplified DC and AC power system models and is able to consider physical constraints with anticipation. The main contribution of this work relies on the HIL and PHIL implementations. HIL simulation has been used for the control validation and two practical problems have been reported and handled during the implementation of MPC-based control algorithm, i.e., :
1. Prohibitive computation time of the optimal solution, and;
2. round-off errors linked to 32-bit floating-point precision on DSP.
The first issue was tackled by reformulating the optimization at the heart of the MPC scheme as well as the reduction of the prediction horizon. Based on this simplified formulation, the computing time has dropped to 40 ms, far below the requested interrupt time imposed by the timer for sending the control references to the high level controllers. The second issue is related to the numerical conditioning, which has been tackled by improving the quadratic optimization solver based on error compensation. Two major improvements have been made in the quadratic optimization solver such as the choice of the linear search step for variables update and conditioning of the Hessian matrix, and the use of Kahan summation algorithm to Newton-Raphson iteration in order to avoid the round-off errors.The investigated MPC-based control scheme has been implemented and validated on a scaled-down setup using PHIL approach. Finally, as the MMC is the dominant topology for HVDC applications, the proposed controller should be implemented in such structure. The extension of this contribution to MMC could be positioned as an interesting perspective. Indeed, the behaviour of an MMC would be similar to a two level PWM VSC for this type of application, since the internal dynamics of the converter do not appear anywhere in the MPC formulation.

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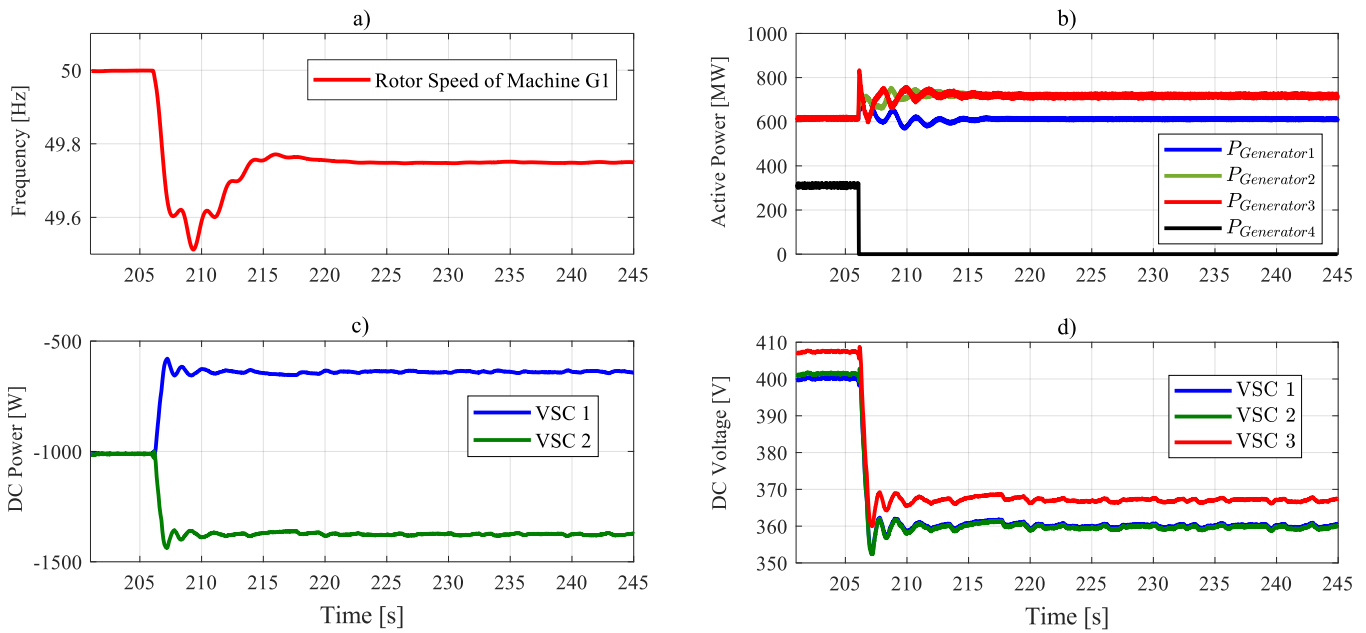
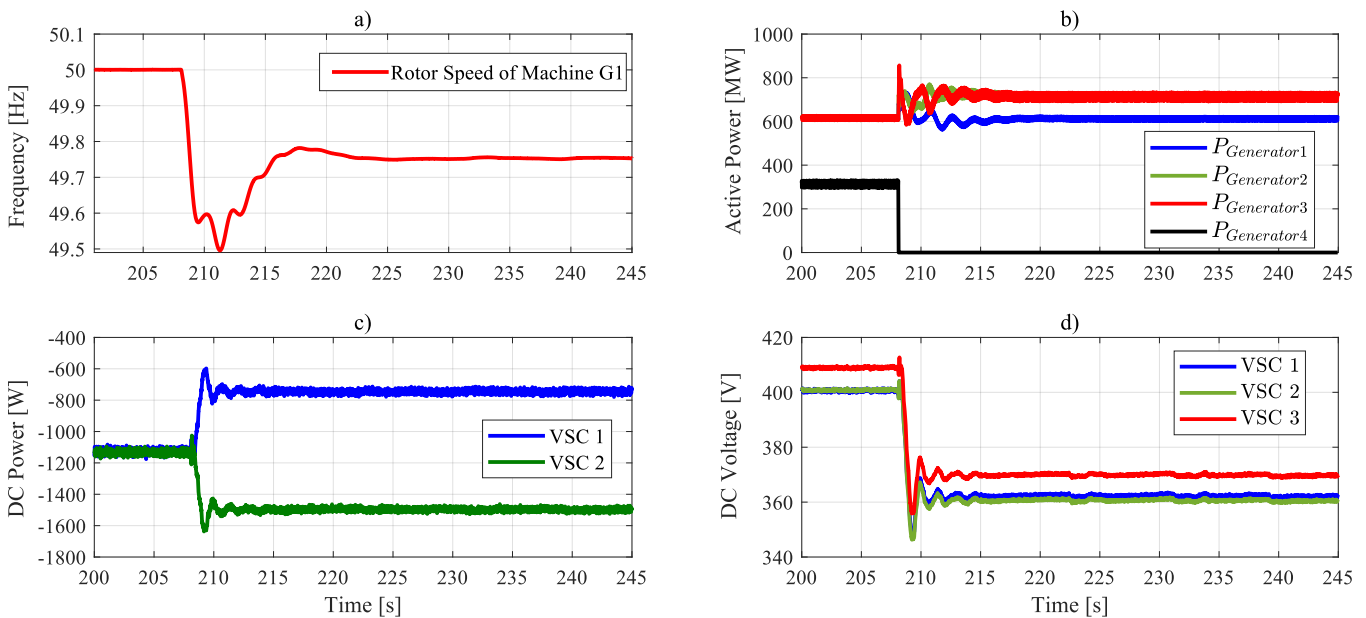Fig. 6. HIL simulation results based on MPC, following the trip of Generator 4 in AC grid 2.

Fig. 7. Experimental results (PHIL) based on MPC, following the trip of Generator 4 in AC grid 2.

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