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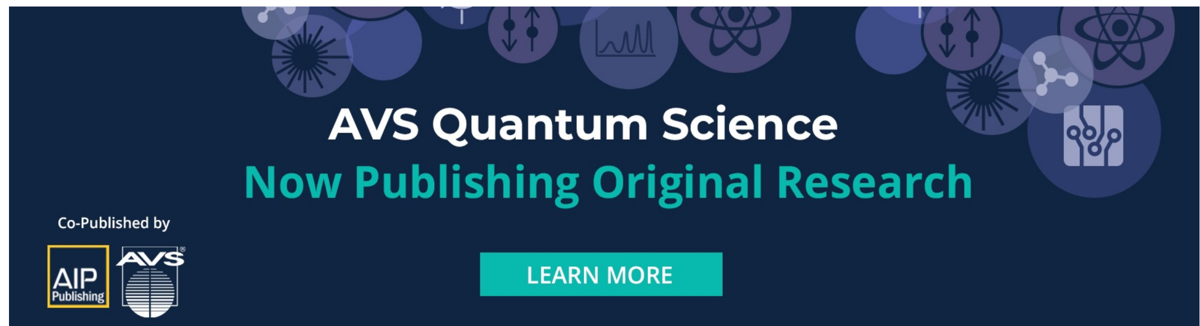

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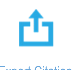
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ABSTRACT

Functional oxides on silicon have been the subject of in-depth research for more than 20 years. Much of this research has been focused on the quality of the integration of materials due to their intrinsic thermodynamic incompatibility, which has hindered the flourishing of the field of research. Nevertheless, growth of epitaxial transition metal oxides on silicon with a sharp interface has been achieved by elaborated kinetically controlled sequential deposition while the crystalline quality of different functional oxides has been considerably improved. In this Research Update, we focus on three applications in which epitaxial ferroelectric oxides on silicon are at the forefront, and in each of these applications, other aspects of the integration of materials play an important role. These are the fields of piezoelectric microelectromechanical system devices, electro-optical components, and catalysis. The overview is supported by a brief analysis of the synthesis processes that enable epitaxial growth of oxides on silicon. This Research Update concludes with a theoretical description of the interfaces and the possibility of manipulating their electronic structure to achieve the desired coupling between (ferroelectric) oxides and semiconductors, which opens up a remarkable perspective for many advanced applications.

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I. INTRODUCTION

A prerequisite for the state-of-the-art study and applications of ferroelectric materials in the form of thin films is their defined and atomically controlled growth, which can be achieved by a number of thin-film deposition techniques, such as molecular beam epitaxy (MBE), pulsed laser deposition (PLD), and atomic layer deposition (ALD). Such growth normally proceeds from atomically flat surfaces on single-crystal substrates with unit-cell dimensions that are commensurate to ferroelectric materials. The most commonly used substrate is $SrTiO_3$ (STO) with a cubic perovskite crystal structure at room temperature and unit cell parameter $a = 3.905$ Å, which is close to a large number of other ferroelectric perovskite materials.[1] In order to adjust the effect of strain on the thin films, other oxide single-crystal substrates are also often used, such as $LaAlO_3$, $(LaAlO_3)_{0.3}$-$(SrAl_{0.5}Ta_{0.5}O_3)_{0.7}$, $ReScO_3$ (Re = Dy, Gd, Sm, and Nd),

MgO, Al_2O_3, and TiO_2. However, it soon became clear that oxide substrate technology greatly limits the scope of applications due to high cost, small size, and poor quality of these substrates. In addition, many of the most advanced processing tools, such as lithography, are developed specifically for the silicon industry, and oxide substrates often cannot be processed on these tools because of the incompatibilities, either with the substrate size or their mechanical, electrical, and thermal properties. As a result, direct integration of various oxides, including dielectric, piezoelectric, ferroelectric, ferromagnetic, optical, catalytic, and superconducting materials with silicon substrates has been proposed to bring a wide range of attractive properties of oxide materials to the well-established fabrication processes of Si wafers, and has attracted considerable attention for more than two decades. Emphasis has been placed on the integration of single-crystalline oxides with Si since the properties of epitaxial films are in many cases superior to those of the same material in amorphous or polycrystalline form. Successful heteroepitaxial growth of oxides on Si has thus opened the door to a wide range of novel device applications with enhanced functionality and flexibility.[2]

However, the union of such dissimilar materials such as transition metal oxides and silicon presents a considerable challenge to heteroepitaxial growth, as a consequence of their very different chemical and structural nature. Consequently, not many oxides have been successfully integrated with Si(001) in the epitaxial form.[3] The most extensively studied epitaxial oxide on Si(001), both experimentally and theoretically, is STO. Such an interest in the epitaxial growth of STO on Si started during the late "1990s" and was primarily attributed to the search of an alternative high-k dielectric for the replacement of gate SiO_2 in metal–oxide–semiconductor field-effect transistors (MOSFETs).[4,5] At that time, the semiconductor industry was facing the challenge to continue the scaling of MOSFETs in order to maintain the trend predicted by Moore's law. In addition to the possibility of STO behaving as a dielectric, ferroelectric functionality was also shown for STO on Si.[6] Although bulk STO is not ferroelectric at any temperature, the ferroelectricity of thin films can be induced by epitaxial strain, which is formed as a result of ~1.7% lattice mismatch between STO and Si. To make this possible, the coherently strained STO film needs to be grown directly on Si with no interfacial SiO_2 layer because it can easily release the required strain. As-prepared epitaxial STO on Si can also be used as a template layer or pseudo-substrate for the integration of other transition metal oxides with the Si platform. Besides, there are many oxides that cannot be epitaxially grown directly on Si. Yet, their epitaxial integration with Si is possible if the thin epitaxial STO layer is grown on Si first. A very thin STO layer with the thickness of four unit cells is already sufficient to ensure further high-quality crystal growth of functional oxides. Materials that are ferroelectric, ferromagnetic, electro-optic (EO), photocatalytic, high-k dielectric, multiferroic, and piezoelectric have already been integrated with Si and could be used in various applications, including temperature or pressure sensors,[7] non-volatile memories,[8] and ferroelectric field-effect transistors (FETs).[6] A good review of some of these applications is given in Refs. 9 and 10, while the integration of ferroelectrics with Si for the piezoelectric microelectromechanical system (piezo-MEMS), optical devices, and catalysts is in the focus of the present Research Update.

II. SYNTHESIS

This section provides a brief overview of achievements obtained by two different deposition methods, i.e., MBE and PLD, mainly in terms of epitaxial growth of STO on Si(001). To date, MBE has been the most extensively used method for the growth of STO on Si, in particular, due to its ability to control the deposition on the atomic level. Before the growth of STO is initiated, the native SiO_2 layer has to be removed from the Si surface since its amorphous structure prevents the epitaxial growth of the deposited material. The resulting reconstructed Si surface is extremely reactive, and high quality epitaxial growth is not possible because STO reacts with Si in the initial stage of the film growth and forms an amorphous transition layer at the interface before epitaxy occurs. Therefore, an appropriate buffer layer should be used that prevents Si from being oxidized. This buffer layer must be thermodynamically stable with Si and should also structurally match with Si as well as STO. First epitaxial growth of STO on Si by MBE was reported by Tambo *et al.* in 1998.[11] However, the growth process they developed is not considered as direct epitaxy of STO on Si due to the relatively thick SrO buffer layer (10 nm), which was grown on the Si(001) surface first. A significant breakthrough in the direct epitaxial growth of single crystal STO on Si(001) by MBE was achieved by McKee and co-workers.[12] They reported the use of sub-monolayer Sr on the clean Si(001) surface, which resulted in the formation of a buffer layer with the 1×2 reconstructed surface. The MBE growth process has been further studied and optimized by several research groups: Schlom's group at Cornell University,[13] Ahn's group at Yale University,[14] IBM Zürich,[15,16] Motorola,[17,18] Saint-Giron's group at Ecole Centrale de Lyon,[19,20] and Demkov's group at the University of Texas at Austin.[21] The result of such an effort was reflected in the abrupt interface between the materials, as well as in the achieved crystallinity of the STO layer. STO layers with the highest crystallinity exhibit the full width at half maximum (FWHM) of 0.006° in the ω direction for the (002) STO reflection,[22] which is much lower than that of STO bulk single crystals (0.035°–0.108°). In addition, an MBE process for the epitaxial growth of high quality STO films on Si substrates with diameter up to 8 in. was developed.[23,24] Apart from Sr, other divalent metals such as Ba and Eu have also been used to achieve corresponding reconstruction of the Si(001) surface.[25,26] Furthermore, it was recently shown that in comparison to the Eu/Si(001) (1×2), which is isomorphic to the Sr/Si(001) (1×2) structure, the Eu/Si(001) (1×5) surface structure is a better choice when growing EuO on Si since it eases the formation of a sharp interface.[27] Alternatively, the PLD technique has also been used for the synthesis of an epitaxial STO layer on Si(001). Table I gives an overview of materials used as buffer layers when PLD was used for the STO deposition.

When STO is deposited on Si(001) without any buffer layer, preferentially oriented or textured films are commonly obtained.[28,29] Sánchez *et al.*[28] demonstrated that the intensity ratio between (002) and (110) STO peaks can be tuned with oxygen pressure and temperature. However, throughout the whole range of investigated pressures (10^{-5}–10^{-3} mbar) and temperatures (400–750 °C), samples exhibited more than one out-of-plane orientation. All other PLD approaches are based on using buffer layers, which are presented in Table I. The best reported properties correspond to STO films deposited on the TiN buffer layer. The narrowest FWHM of the ω-rocking curve measured on STO(002) reflection for STO films

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TABLE I. Survey of buffer layers that have been used for the growth of STO on Si(001) using the PLD technique.

Buffer layer	References	Buffer layer	References
Without buffer	28–31	$YSZ/Y_2O_3/YBa_2Cu_3O_7$	29
YSZ	32	$CoSi_2$	29
TiN/YSZ	32	CaF_2	29
TiN	33–36	H-terminated Si	37
CeO_2/YSZ	32, 38, and 39	SrO	29, 37, 40, and 41
CeO_2	29	Sr	42–46
$Ce_{0.12}Zr_{0.88}O_2$	47	Nanosheets	48 and 49

grown on epitaxial TiN/Si(100) was 0.8°.[34] Another relatively often used buffer layer is yttria-stabilized zirconia (YSZ)/CeO_2. YSZ has the advantage that it can be deposited directly on the natively oxidized Si(001) substrate because it activates the decomposition of the native SiO_2 to SiO.[50] The reducing atmosphere in the initial stage of growth promotes the reaction Zr +2SiO_2 → ZrO_2 + 2SiO. Once the amorphous SiO_2 layer is removed, YSZ grows epitaxially with the following epitaxial relationships: YSZ(001)||Si(001) along the out-of-plane direction and YSZ[100]||Si[100] along the in-plane direction.[51] STO films deposited on YSZ/Si(001) are (0hh) oriented. In order to change the STO growth direction to (001), an additional layer of CeO_2 needs to be deposited on YSZ. Rocking curves of the (002) peak of STO grown on the YSZ/CeO_2 double buffer layer are around 1.2° wide.[32] Besides, $Ca_2Nb_3O_{10}$ and $Ti_{0.87}O_2$ nanosheets have also been used as buffer layers for growth of highly oriented piezoelectric films on Si and Pt/Si substrates, demonstrating a route toward the fabrication of high-quality devices on non-perovskite and even non-crystalline substrates such as glass or polished metal surfaces.[52–54] Elemental Sr for the preparation of the buffer layer in the PLD process of STO growth on Si(001) has been used by two research groups only. In the studies by Zhou *et al.*,[42,43] a relatively thick Sr layer (1.2–1.9 nm) was deposited on the Si(001) surface free of native SiO_2 prior to STO deposition, while in the study by Spreitzer *et al.*,[55] the procedure followed the protocol, determined for MBE growth of STO on 1/2 ML of Sr on Si(001),[6] which was nevertheless modified for peculiarities of the PLD technique.

Yet another methodology for the integration of single-crystal functional oxides with silicon involves their epitaxial transfer at room temperature. PLD growth of PZT on $La_{0.7}Sr_{0.3}MnO_3$ (LSMO) coated $SrTiO_3$ demonstrates an example, where after the growth, LSMO was wet etched, while the released layer was then carried by a transfer stamp on the target substrate such as Si, keeping the overall film quality intact.[56] Alternatively, $Sr_3Al_2O_6$ has been used as a water-soluble sacrificial layer for the epitaxial transfer of functional layers to arbitrary substrates, including Si.[57]

Integration of certain ferroelectric perovskites with silicon can lead to realization of a new kind of nonvolatile transistors that can perform both logic and memory functions, as an example. Such ferroelectric transistors have two main requirements: in addition to the epitaxial growth, the ferroelectric polarization must have a component normal to the interface. $Pb_xZr_{1-x}TiO_3$ (PZT) was the first epitaxial ferroelectric grown on Si(001) through the utilization of an insulating, single-crystalline STO transition layer.[58,59] Another material widely studied for this purpose was $BaTiO_3$ (BTO). Niu *et al.*[60] demonstrated the epitaxial growth of (001)-oriented BTO films on the Si(001) substrate buffered by the thin STO layer using both MBE and PLD techniques. It was shown that due to the limited oxygen pressure during the growth, the BTO layers grown by MBE exhibit no ferroelectric properties, but only typical dielectric behavior despite post deposition annealing being performed. In contrast, a ferroelectric BTO layer was obtained using the PLD method, which permits much higher oxygen pressure. Another successful attempt at growing epitaxial BTO films with a polarization pointing perpendicular to the silicon substrate on STO-buffered silicon has been reported by Dubourdieu *et al.*, demonstrating ferroelectric switching of 8-nm- to 40-nm-thick BTO films in the metal–ferroelectric–semiconductor structure.[61] On the other hand, Abel and co-workers[62] focused on BTO films with polarization parallel to the silicon surface for silicon photonics technology, which is detailed in Sec. IV below.

III. PIEZOELECTRIC MICROCANTILEVERS

Piezoelectric thin films are used in a wide variety of applications, both in industry and piezoMEMS foundries, and by different device developing research groups.[63–67] The used materials are mainly sputtered AlN, AlScN thin films, as well as PZT, mostly at the morphotropic phase boundary ($PbZr_{0.52}Ti_{0.48}O_3$), which is often produced by chemical solution deposition (CSD). Academic groups usually use PLD for growing perovskite ferroelectrics, mainly PZT, with near epitaxial quality for Si-piezoMEMS applications,[52,68–71] as well as materials, such as lead-free and relaxor materials. A lot of systematic work on piezoelectric materials over the last decade is from the Twente group, among others investigating the effect of different nucleation layers on Si on the ferro- and piezoelectric properties of PZT films (Table II).[52,69–71]

The basic, and in research mostly used, piezoMEMS device is the bimorph cantilever, consisting of a relatively thick Si cantilever beam (usually 1–10 μm thick) as the passive (supporting) beam and a piezoelectric layer (few 100 nm to 1 μm) for actuation. Usually, the piezoelectric material is sandwiched between top and bottom electrodes. The applied field, E_3, causes lateral contraction (compressive strain) of the piezoelectric layer by the converse piezoelectric effect, $\Delta x = d_{31}E_3$, that results in the bending (curvature) of the cantilever. This activation mode is called the d_{31} mode because it depends on the d_{31} piezoelectric parameter (which has a negative sign).[166] When interdigitated (IDT) electrodes are used, the device

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TABLE II. Structure and piezoelectric properties of PZT on Si with different nucleation layers.

	SRO top electrode/PZT/SRO-bottom electrode on					Pt-top electrode/PZT on				STO single crystal[a]
References	52	52	52	52	52	52	71	52	52	
Nucl. layer on Si	YSZ	TiOns[b]	CeO_2/YSZ	STO[c]	CNOns[b]	LNO/Pt/Ti/SiO_2		TiOns[b]/Pt	CNOns[b]/Pt	
PZT orientation	(110)	(110)	(001)	(001)	(001)	Mixed	Mixed	(110)	(001)	
Structure	Epitaxial	Textured	Epitaxial	Epitaxial	Textured	Textured	Columns[d]	Textured	Textured	
FWHM (deg.) of PZT	1.42	0.78	0.96	0.56	0.58	4.2		2.6	1.2	
$d_{33,\mathrm{eff}}^{cl}$ (pm V^{-1})	100	122	92	88	110	124	100–600[e]	132	112	327
$d_{31,\mathrm{eff}}^{cl}$ (pm V^{-1})	−90	−86	−116	−130	−120	−80		−84	−102	−156

[a]Single-crystal values are for a single-domain polarization state, thus excluding extrinsic effects, such as domain wall motion and clamping.[81] For a polydomain, single crystal modeling gives a value of the order of $d_{33,\mathrm{eff}}$ = 600 pm/V.[82]
[b]CNOns, TiOns: a few monolayers of $Ca_2Nb_3O_{10}$ (TiO_2) nanosheets, lateral dimensions of a few μm, thickness 1–3 nm.
[c]Thin STO buffer layer was grown on Si by MBE.
[d]Predominantly (001) oriented and largely freestanding, disconnected grains.
[e]Local value, depending on vertical position in the thickest films.

is said to operate in the so-called d_{33} mode.[167] Here, we will not further consider this mode of operation. Although the piezoelectric parameters are usually treated as material parameters, in practice, their values depend significantly on the device structure, in which they are measured. Hence, it is not straightforward to compare values from different devices and groups and draw conclusions about the material properties.

In thin films, d_{33} values are usually obtained from capacitor structures (not to be confused with the d_{33} mode described above), in which the out-of-plane displacement, $\Delta z = d_{33}E_3$, of the top electrode is measured as a function of the applied field (for example, with a double beam interferometer to compensate for substrate bending). Although this on first sight seems straightforward, there are a few factors that change the piezoelectric coefficient from its bulk, unstrained value, as deduced from single-crystal measurements. First, there is the clamping of the substrate that hinders lateral contraction of the piezoelectric film, when the film extends in the normal direction.[72] Second, the ferroelectric domain structure (especially in tetragonal films) is very sensitive to the stress in the film, and the actual structure is determined by the minimization of the elastic energy in the film. For the piezoelectric effect, it is important to realize that the value of the d_{33} parameter can depend significantly on the combined effects of substrate clamping and this domain structure formation.[73,74] A third and often overlooked factor is the role of the elastic properties of the substrate. For hard substrates (large Young's modulus), such as most perovskites, there is little deformation of the substrate, and the effect of the ("hard") clamping can be described in terms of the elastic parameters of the ferroelectric film only, as done in Refs. 72–75. However, for "soft" substrates with relatively low Young's modulus, such as Si or glass, the substrate can bend significantly[76] or the capacitor structure can indent or pull-out the substrate significantly, depending on the capacitor and substrate dimensions. The latter phenomenon is called the "indentation" effect, and because of substrate deformation, it will affect the measured Δz_3.[77] Fourth, there is the crystalline quality of the piezoelectric film that may change the ferro- and piezoelectric parameters, as well as its elastic properties. This aspect is discussed further here.

The d_{31} parameter is usually obtained from the bending of bimorph Si cantilevers with d_{31}-mode actuation. There are also few examples of the so-called freestanding cantilevers (the ferroelectric layer not supported by a substrate), in which an asymmetry of the top and bottom electrodes functions as the bimorph.[78,79] The value of d_{31} is extracted from a more or less detailed mechanical model of the cantilever and requires the knowledge of many elastic parameters and dimensions of all considered layers in the device stack, for example, that used systematically by the Twente group.[75,80] Such usually two-dimensional analytical models (that only consider the curvature of the cantilever in a plane perpendicular to and along the length of the cantilever), neglect the induced bending by the piezoelectric effect over the cantilever width. This causes the cantilever to become stiffer with increased width and applied field, leading to a lower deduced effective d_{31} value. Furthermore, such models are fairly sensitive for the used material properties and dimensions. On the other hand, they take explicitly account of the clamping.[168]

All the secondary effects and modeling complications make it difficult to compare experimentally determined d_{31} and d_{33} values with the bulk value and to compare values obtained from different groups, for example, to study the effect of different nucleation layers, electrode materials, growth orientation, and growth conditions. For this reason, we have collected and present here an overview of the results of the Twente group on cantilevers and capacitors in/on Si, which were fabricated using the same designs and dimensions/thicknesses,[169] and cantilever model[75,80] to extract the effective values of d_{31} and d_{33}. This allows the comparison of piezoelectric parameter values as a function of the effect of different nucleation layers and electrodes and eliminates variations in PZT quality from

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different deposition techniques and conditions used by different groups.

The tabulated devices have either perovskite $SrRuO_3$ (SRO) or Pt the top and bottom electrodes. In combination with a thin CeO_2 layer on the YSZ nucleation layer, the growth direction of the subsequent perovskite layers is changed from (110) to (001).[83] Further two types of nanosheets were used that cause (110) growth for TiOns and (100) growth for CNOns. The main difference is in the crystalline structure. There is nearly epitaxial growth on STO/Si and CeO_2/YSZ/Si with in-plane and out-of-plane (nearly) parallel alignment of the lattice in the grains, thus with low-angle grain boundaries. There is local epitaxial growth on CNOns/Si (on the scale of a few μm) but with random in-plane alignment, thus with high-angle grain boundaries between the nanosheets, albeit with a relatively low grain boundary density. For CNOns/Pt/Si, one observes also increased out-of-plane misalignment (larger FWHM of the rocking curves), which for these films is caused by the relatively rough Pt-film underneath the nanosheets. The (110)-oriented films show a second type of in-plane misalignment due to the two possible in-plane orientations of the pseudo-cubic, 45° tilted unit cell. Finally, the films on LNO/Pt/Si contain, in addition, (001)/(110) grain boundaries.

To see the effect of the crystalline quality of the ferroelectric film on the piezoelectric coefficients, consider the effective coefficients due to clamping of a capacitor and a cantilever structure in the d_{31} mode,[72,75]

$$d^{cl}_{33,\mathrm{eff}} = d_{33,\mathrm{eff}} - d_{31,\mathrm{eff}} 2s_{12}/(s_{11}+s_{12}) = d_{33,\mathrm{eff}} + d_{31,\mathrm{eff}} 2\nu/(1-\nu),$$

$$\sigma_{gen} = d_{31,\mathrm{eff}}/(s_{11}+s_{12})E = d_{31,\mathrm{eff}} Y/(1-\nu),$$

where $d_{33,\mathrm{eff}}$, $d_{31,\mathrm{eff}}$, s_{ij}, Y, and ν are the effective piezoelectric coefficients (as a result of the domain structure, possible polarization screening, and the substrate indentation effect), the elastic compliances, Youngs modulus (in the relevant direction), and Poisson ratio of the ferroelectric film, respectively. Y and ν decrease in value from those of the single crystal with increasing porosity, i.e., grain boundary density and separation between grains. These grain boundaries could be pictured as a more elastic medium in between the grains. Hence, one expects that $d^{cl}_{33,\mathrm{eff}}$ increases with increasing porosity, while the curvature of the cantilever, proportional to the generated stress in the ferroelectric layer, σ_{gen}, decreases with decreasing Y and ν. For films with largely disconnected columnar grains, $\nu \approx 0$, and hence $d^{cl}_{33,\mathrm{eff}} \approx d_{33,\mathrm{eff}}$, which depends on the intrinsic piezoelectric effect and domain wall motion, amounting to effective values in the range of 600 pm/V, as predicted theoretically[82] and measured experimentally.[71]

For the tabulated films, one may assume in good approximation the same material quality within the film grains. Because of the fixed substrate type, the domain structure and the indentation effect are also expected to be very similar, hence the $d_{33,\mathrm{eff}}$ and also $d_{31,\mathrm{eff}}$ values are approximately the same[170] (except for the films of Ref. 71). Now, one can explain the difference in piezoelectric properties in terms of differences in porosity arising from the in-plane misalignment from the lattice in adjacent grains and the size of the grains. The film on STO/Si has the highest crystalline quality (lowest FWHM and in-plane alignment, thus lowest porosity and highest density) and shows the lowest $d^{cl}_{33,\mathrm{eff}}$ value. The elastic properties are closest to those of defect-free PZT so that this film "suffers" most from the substrate clamping and the indentation effect. $d^{cl}_{33,\mathrm{eff}}$ increases slightly with the decreasing crystalline quality: for the film on CeO_2/YSZ, the in-plane orientation uniformity is still high, whereas for the film on CNOns, it is uniform within the dimensions of a single nanosheets, but the PZT in-plane orientation varies arbitrarily from nanosheet to nanosheet. The opposite trend is observed in the measured $d^{cl}_{31,\mathrm{eff}}$ values: with fewer grain boundaries, the generated stress and thus the cantilever curvature increase, resulting in higher $d^{cl}_{31,\mathrm{eff}}$. There is a significant increase in $d^{cl}_{33,\mathrm{eff}}$ and decrease in $d^{cl}_{31,\mathrm{eff}}$ for the (110) films as expected from the increased porosity.

IV. ELECTRO-OPTICS

Our daily life depends on our capabilities to transmit digital information across millimeters or over thousands of kilometers. In this context, optical communication has become the backbone of digital information technologies, and its evolution has dramatically accelerated. A striking example is Photonic Integrated Circuit (PIC) technology, used to build all the important electro-optic functionalities on semiconductor chips either made of III–V materials or silicon. Such functionalities (light emitters, detectors, waveguides, and modulators) are used to convert electrical into optical signals and vice-versa, e.g., in modules called transceivers. Among the different technology platforms, silicon photonics (Si-PIC) is becoming the leading option because of its low cost. For Si-PIC, silicon-on-insulator is used as the starting substrate, with a 200-nm thick silicon film separated from a silicon substrate by a 2–3 μm thick SiO_2 film. Once waveguides are etched in the top silicon film and cladded with a deposited SiO_2 film, the light is confined in the silicon core. For the wavelength of interest (1.3–1.55 μm), the difference in the refractive index between silicon (3.4) and silica (1.6) is such that a strong confinement is obtained, and tight bends can be realized. Si-PIC is therefore very attractive because of its simplicity, cost, as well as its compactness. Its use is broadening beyond digital communication and impacts very different application areas. Most of the required functionalities for PIC can be implemented in Si-PIC, except light emission.[171] The most important functionality is to control the phase and the amplitude of the optical signal. It is used to modulate it in high-speed transceivers, or more generally to control light in optical switches, in optically based computers and in optical sensors, to give a few examples. In Si-PIC, it is achieved using the modulation of the refractive index across a p–n junction under bias using the so-called plasma dispersion effect. Although the fabrication is simple, the performances are intrinsically limited. The maximum bandwidth is, e.g., too low for future high-speed transceivers, it is not possible to separately modulate the phase and the amplitude of light, and the absorption coming from the doped regions in silicon generate high optical losses in the device itself (defined as insertion losses). There is a clear opportunity for technologies compatible with Si-PIC that would alleviate such limitations.

The history of the microelectronics industry shows us that novel materials have always been a powerful innovation engine.

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Introducing Cu, Ge, or HfO_2 was a major innovation that enabled a whole industry to deliver an impressive doubling of performance every 18 months for 50 years. For Si-PIC technology, a similar strategy can be envisioned. In this context, ferroelectric oxides are known for decades as materials with very interesting electro-optic properties. For long-haul communication, discrete modulators are using cm-sized, large crystals of $LiNbO_3$ (LNO) for more than 40 years and support the internet today. The electro-optic properties of LNO are described by the Pockels effect, which relates the change in the optical refractive index n for a material upon application of a (quasi-)static electric field E through $\Delta n(\frac{1}{n^2})_{ij} = \sum_k r_{ijk} E_k$.[84] The Pockels coefficient "r" vanishes for centro-symmetric crystals, and this effect is therefore only non-zero in materials whose crystalline structure is non-centrosymmetric, such as ferroelectric oxides. Interestingly, the electro-optic response is not only allowed but can be typically large in such ferroelectrics due to the presence of highly polar and Raman active soft modes[85] and even diverges around the ferroelectric phase transition[86] due to polar mode softening. Using the Pockels effect as in ferroelectric LNO has many advantages that exactly compensate for the weaknesses of Si-PIC. The change in the refractive index is ultrafast, and the electric field modifies only the phase of the optical signal without altering its amplitude. In addition, materials such as LNO are transparent, and devices have very low insertion losses. Merging Si-PIC and Pockels technology is the grand challenge for the next generation Si-PIC technology.

Integrating Pockels materials in Si-PIC obviously requires such materials to be available in thin films on full wafers. Because the Pockels effect is a tensorial property, the structural and microstructural properties of thin films (density, grain size, and crystal structure) have a major impact on their EO properties. Ideally, thin films should have large crystal grains and have a well-defined structural orientation, which is a configuration obtained in epitaxial thin films.[88] Among the known Pockels materials, ferroelectric oxides have the largest Pockels coefficient (measured in pm/V). LNO—the gold standard—has a Pockels coefficient of 30 pm/V. For PZT—the industrially most relevant ferroelectric ceramics—it reaches 200–300 pm/V, and for BTO—the prototype ferroelectric perovskite—it can be as large as 1000 pm/V. The three selected examples illustrate different strategies explored to integrate

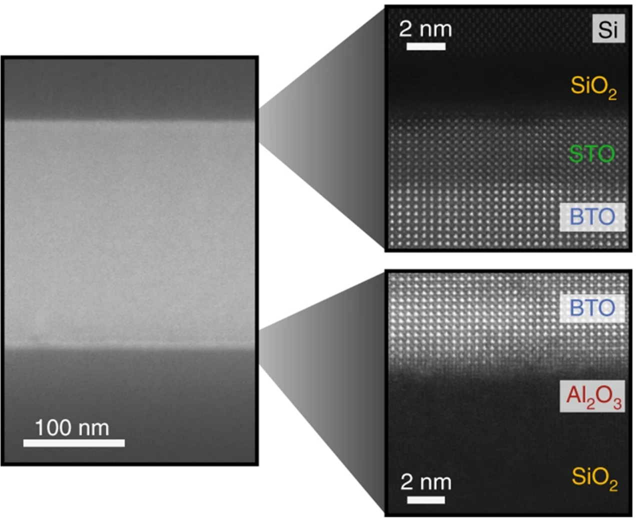

FIG. 1. Low (left) and high (right) resolution cross-sectional image of BTO/Si (top) bonded onto SiO_2/Si (bottom).[87]

ferroelectric oxides in Si-PIC. The most successful approach to obtain LNO on silicon is to slice LNO single crystals and bond it onto the silicon wafer. The technology to grow large LNO crystals is mature since it has been used for 40 years to grow the discrete crystals for bulk modulators. The wafer bonding and layer transfer technologies are also available industrially, and LNO-on-Si are available commercially as full wafers.[89] The inherently good properties of thin film LNO-on-Si could be harnessed to achieve 70 Gbit/s modulation and with phase-shifter losses below 0.5 dB. Despite such impressive device metrics,[90] the LNO supply is, however, limited in wafer size to 100–150 mm diameter. In the case of electro-optical high-speed modulators, the dimensions of the optical devices remain large because of the moderate value of the Pockels coefficient. A different approach has been proposed to integrate PZT in Si-PIC. It relies on the deposition of PZT thin films with sol–gel using a dedicated template to promote a well-defined

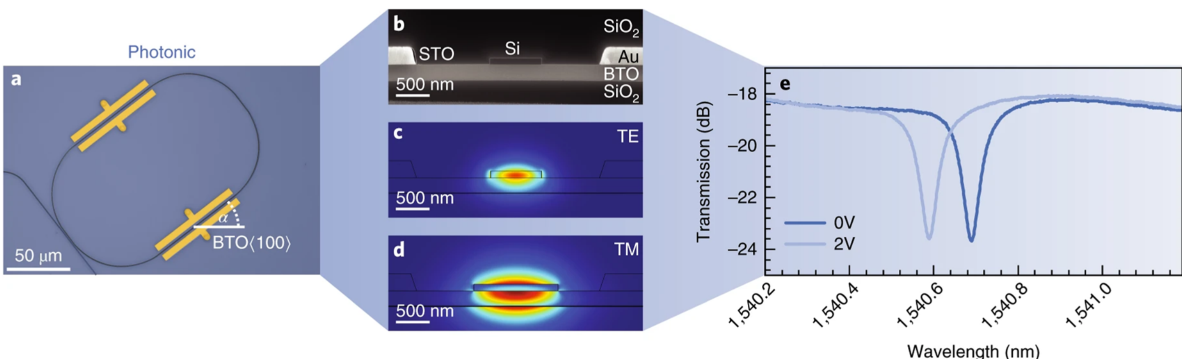

FIG. 2. (a) Optical microscopy image of a photonic ring resonator. (b) Scanning electron microscopy (SEM) cross-sectional image of the photonic devices between the electrodes. [(c) and (d)] Simulated mode profiles of the photonic transverse electric and transverse magnetic modes, respectively. (e) Transmission spectra of a photonic racetrack resonator for two different bias voltages.[87]

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crystalline orientation. PZT has been used to demonstrate Pockels based modulation,[91] with SiN-based ring resonator modulator showing 33 GHz bandwidth and a modulation efficiency of 3.2 Vcm. The fabrication method is attractive because of its simplicity, but the measured effective Pockels coefficient (67 pm/V) is moderate. The third and most promising approach is enabled by the integration in Si-PIC of thin crystals of BTO. BTO exhibits one of the largest room temperature Pockels coefficient[92]—30× larger than LNO—and its use in modulators has been already identified using exotic oxide substrates.[93] In the last 10 years, however, novel methods and processes enabled the growth of epitaxial perovskites such as BTO on silicon substrates.[62,94,95] Using a STO nucleation layer, films with a higher structural quality can be obtained than using YSZ buffers. The availability of high quality BTO thin films on silicon enabled direct wafer bonding on SiO_2/Si to fabricate stacks suitable for integrated photonics devices. Using such BTO/SiO_2/Si stacks, a key proof of concepts has been realized (Fig. 1).[87] Today, it is established that low-loss waveguides can be obtained with BTO[96] and that BTO thin films retain their unique electro-optic properties and a very large Pockels coefficient (Fig. 2).[87,95] This recent work has been the starting point for several demonstrators showing the potential for monolithic electronic–photonic integration, cryogenic operation,[97] and low-power switching.[87,98]

V. CATALYSIS

A. New possibilities for ferroelectrics

Ferroelectrics present unique possibilities for catalysis because their surface chemistry and interaction with adsorbates depend on their polarization state.[99,100] This tunable electronic modification creates new opportunities relative to standard oxide surfaces to change the binding energy of adsorbates, including CO_2 and H_2O (relevant to CO_2 sequestration, reduction reactions, and water splitting[99]), and drive reduction or oxidation reactions that are relevant to heterogeneous catalysis and electrocatalysis. In general, poling upward toward the surface promotes an electron-rich surface, while poling downward creates a hole-rich surface.[101,102] A downward polarization thus tends to facilitate oxidation reactions (and vice versa), though the interaction will be surface and species dependent.

Experimental realization of these effects has proven challenging, in no small part because it is difficult to control the polarization state of an ensemble of typical nanoparticulate catalysts. However, corona charging has recently been shown to change the polarization of $Bi_{0.5}Na_{0.5}TiO_3$ pellets[103] and $BiCoFeO_3$ powders[104] used as catalysts for the oxygen evolution reaction. In both of these studies, an enhancement was seen in the key figure of merit for catalyst activity, the exchange current density. In the case of the $BiCoFeO_3$ nanoplate powders, a reduction in overpotential of almost 60 mV was seen, enabling the ferroelectric catalyst to surpass state-of-the-art IrO_2 catalysts in activity, without the use of precious metals.

Adding a catalyst layer atop the ferroelectric can increase the impact of the underlying polarization, resulting in dramatic changes in the catalyst properties as a function of polarization direction. For example, in a computational study of TiO_2/STO heterostructures, a work function difference up to 2.5 eV was seen in the TiO_2 depending on the polarization direction induced in the STO via strain.[105] For Pt monolayers on ferroelectric $PbTiO_3$, the binding energy of CO, C, O, and N changed between 0.4 eV and 0.8 eV. In fact, first-principles studies suggest that the structural and electronic modification of the surface in response to the depolarizing field can change entirely the catalytic reaction pathway.[106] A critical design parameter is that the thickness of the catalytic overlayer must be less than its Debye length in order to avoid screening of the polarization's effects at the surface. Dewetting of ultrathin metal catalyst overlayers into three-dimensional aggregates larger than the screening length resulted in little observable enhancement from a ferroelectric effect but instead led to cluster-size effects.[107–109]

Beyond static changes in the catalytic surface affected by the ferroelectric polarization, dynamic enhancements can, in principle, be induced accordingly in reaction cycles that vary the polarization; examples include cycling of the temperature or external magnetic fields.[101] Kakekhani and Ismail-Beigi proposed a thermal reaction cycle for water splitting on $PbTiO_3$, leveraging its pyroelectric properties to reduce all activation energy barriers below ~0.4 eV.[110] Reaction cycles on $PbTiO_3$ can also be designed based on switching between up and down polarization states below the Curie temperature, for example, to directly reduce NO_x or oxidize CO.[101] The ferroelectric polarization thus offers the enticing potential of an additional and dynamic dimension to modulate the electronic structure at the surface of catalysts, change reaction pathways, or develop new reaction mechanisms.

B. Semiconductors, ferroelectrics, and photocatalysis

The ferroelectric's internal field is also attractive for photo(electro)catalysis as an intrinsic charge-separating mechanism. This internal polarization field may be especially useful in nanometric ferroelectrics where the full thickness may be depleted of mobile carriers. Most previous experimental work has thus focused on ferroelectric-enhanced charge separation in photocatalysts.[111–113] Recent reports of ferroelectric epitaxial[114] and polycrystalline oxide[115] photocatalysts have emerged, indicating a clear benefit of maintaining a poled ferroelectric for supporting charge separation and transport. However, ferroelectrics are generally wide bandgap oxides, limiting their efficiency potential under terrestrial sunlight. Novel narrow-gap "ferrophotovoltaic" materials are of emerging interest but still require significant development.[116]

Pairing ferroelectric layers with mature semiconductor technology provides an alternative path to circumvent the limits on solar absorption that results from the wide bandgap of conventional ferroelectrics. Moreover, since many semiconductors are unstable in the extreme pH and either the highly oxidizing or reducing chemical environments necessary for important catalytic schemes,[117] a protective oxide overlayer can be extremely beneficial. Beyond protection of the semiconductor, an oxide overlayer can also serve as a tunable template for the catalytic design. A major step toward the oxide-semiconductor photoelectrochemical cell (PEC) was demonstrated by Hu *et al.*, achieving encouraging efficiencies for amorphous TiO_2 layers on Si prepared with ALD[118] (and on GaAs and GaP). Soon thereafter, this team has shown considerable improvement by applying this technique on tandem solar cells composed of GaAs/InGaP.[119] While these exciting developments constitute major advantages, from the perspective of harnessing ferroelectrics for catalysis, the amorphous oxide produced by ALD constitutes a disadvantage. Typically, high-quality

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ferroelectrics require a crystalline substrate to induce the desired out-of-plane orientation and lower interface depolarization. Crystalline oxide catalysts are widely developed for the oxygen reduction and evolution reactions,[120,121] particularly those adopting the perovskite structure.[122,123]

As such, epitaxial oxide-semiconductor PEC implementations[2] provide an attractive route toward ferroelectric integration, but the growth of a ferroelectric atop semiconductors presents a significant challenge. A key milestone in this regard was demonstrated by Ji *et al.*, who integrated epitaxial (but centrosymmetric) STO on Si to produce a photocathode [Fig. 3(a)], stable during 35 h of photoelectrochemical H_2 production.[124] When a nanopatterned Pt/Ti catalyst was added to the surface, the resulting photocathode achieved 4.9% light-to-hydrogen power conversion efficiency. The small conduction band offset between the Si and the STO was critical to achieving low loss performance [Fig. 3(b)]. This approach inspired the integration of STO on a direct-bandgap GaAs n–p junction solar cell, achieving stable hydrogen production at neutral pH and a similar incident photon-to-current efficiency without any additional catalyst atop the STO.[125] However, the large (~0.7 eV) conduction band offset at the STO/GaAs interface led to significant voltage losses, resulting in a light-to-hydrogen efficiency of only 0.55%. These preliminary epitaxial STO/semiconductor structures can serve as a template for epitaxially integrating many additional oxides,[2] including the common ferroelectrics BTO and lead zirconate-titanate (PZT). Interestingly, both materials have already been integrated on Si, Ge, and on GaAs,[126–129] albeit not for catalysis purposes.

The well-known pros-and-cons of the indirect gap Si vs the direct (albeit larger) gap GaAs have an additional facet when considering epitaxial integration of oxides on top. Oxide epitaxy on Si is far easier compared to GaAs,[2] affording a wider temperature window for the growth of ferroelectrics. However, despite the higher (relative) stability of the oxide/Si interface, even nanometer-scale interface layers, which are very hard to completely avoid, can be quite insulating and block currents between the substrate and ferroelectric, with detrimental consequences for (photo)electrocatalysis applications. Finally, Si has a lower lattice parameter, which may provide an advantage in orienting the (larger) c-axis polarization to the desired out-of-plane orientation, for BTO and related ferroelectrics. As such, the choice of semiconductor for ferroelectric (photo)electrocatalysis may mirror that for terrestrial photovoltaics, where Si has emerged dominant—the lower cost and growth complexity for Si may triumph over the direct bandgap and optoelectronic quality of GaAs. However, we highlight insulating oxide-Si interface layers to be a crucial aspect during growth and perhaps even during long term operation of devices.

We now briefly consider the gaps between existing capabilities and the realization of efficient ferroelectric/semiconductor implementations for catalysis. We consider the key issues to be (1) the formation of undesirable interfacial layers at the oxide-semiconductor contact, (2) understanding and engineering of the ferroelectric/semiconductor band structure to facilitate efficient carrier transport from the semiconductor to the ferroelectric surface, and (3) the likely need to integrate a co-catalyst atop the ferroelectric. These are all strongly interrelated issues, deeply involved with the growth method and conditions.

Reducing and avoiding interface layers at oxide-semiconductor epitaxy is a major challenge,[2] often dictating significant limits to the growth conditions (temperature, oxygen pressure). Oxidation at the interface can, for example, introduce interface states and traps in the bandgap or produce counterproductive band bending. In more severe cases, surface oxidation results in an insulating interface layer that inhibits current flow. Relatedly, any internal band offsets, whether due to an interfacial reaction or simply the pristine ferroelectric/semiconductor interface, must be minimized when considering the ultimate energy efficiency of the electrochemical energy conversion. Beyond chemical tuning, manipulating the thickness of an epitaxial $LaFeO_3$ catalyst on Nb:STO from 2 nm to 10 nm was demonstrated to shift the valence band offset by more than 200 mV, altering the (photo-)electrochemical activity for the oxygen evolution reaction.[130] Focusing on the interface by design may

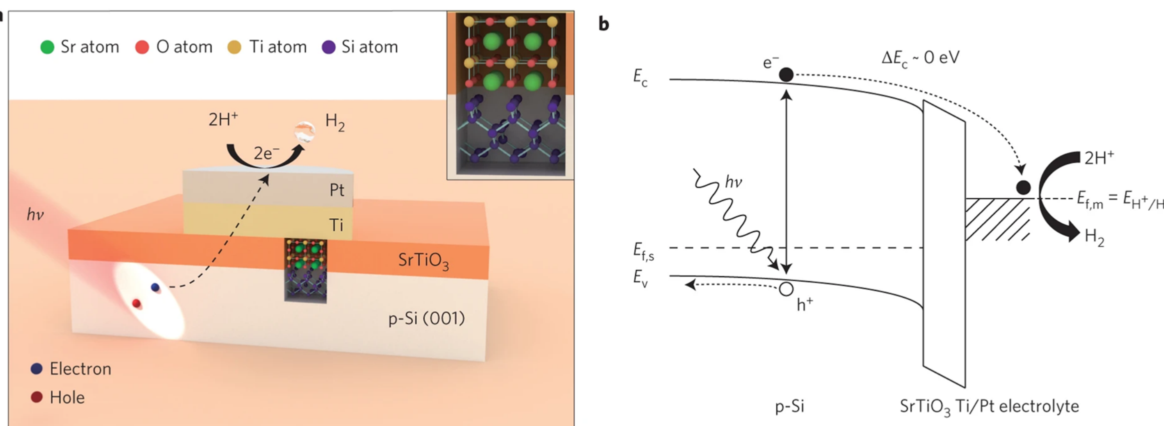

FIG. 3. (a) Schematic of the operation of the STO/p–Si photoelectrocatalytic device in the hydrogen evolution reaction. Such structures can be used as a template to integrate ferroelectrics on top of STO. Photogenerated electron–hole pairs are separated by the built-in field, and the (b) band alignment drives electrons to the overlaying metal catalyst.[124]

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provide a path to address these challenges to achieve the stability and electronic structure necessary.

Finally, although many successful catalysts have been developed for energy-relevant electrochemical conversion reactions, such as hydrogen evolution (electrolyzers) and oxygen reduction (fuel cells), their integration as co-catalysts atop the ferroelectric is non-trivial if the advantages of the ferroelectric are to be maintained. Clearly, the use of fabrication approaches capable of single-nanometer-level control is required. Beyond flexible and mature approaches such as MBE, PLD, or ALD, one potentially promising pathway may be the use of soft-landing deposition or wet-chemistry to achieve single-atom catalysts, which have demonstrated exciting prospects across catalysis and potential scalability.[131,132]

VI. THE ABO_3/Si INTERFACE—A FIRST-PRINCIPLES THEORETICAL PERSPECTIVE

Since the pioneering work of McKee *et al.* in 1998,[12] the crystalline Si/ABO_3 perovskite interface has also attracted continuous theoretical interest. From the early stages,[133] first-principles calculations were considered as a promising tool to get insight at the atomic scale on the interface and to help interpreting experimental data (see Refs. 134 and 135 and references therein). However, modeling such a stack remains very challenging due to both its own intrinsic complexity and some limitations of the theoretical methods. At this stage, significant advances have been reported, but some issues remain open.

A. Technical details and related limitations

Theoretical investigations of Si/ABO_3 interfaces are typically performed in the framework of density functional theory (DFT) using implementations that make use of periodic boundary conditions (i.e., repeating a cell or supercell along the three directions of space).[136] The modeled system then consists of a Si substrate covered by an ABO_3 film, exposed to vacuum or eventually capped with a metallic electrode. While Si is sometimes replaced by Ge[137,138] and different perovskites (STO,[133] BTO,[139] and $LaAlO_3$[140,141]) have been considered as a top layer, most studies concern Si/STO.[134] In the simulation, the substrate part is typically restricted to only few Si layers with dangling bonds of bottom Si atoms passivated with hydrogens and a top ($n \times 1$) reconstructed Si(001) surface. Depositing a STO film on such a Si surface then requires making specific choices regarding first the eventual presence of an interface layer (e.g., a monolayer or half-monolayer of Sr, additional O) and second the first oxide layer (i.e., either SrO or TiO_2). A vacuum region (typically 12–15 Å) is then added on top of the stack to avoid spurious interactions between periodic replica, and a dipole correction is required to compensate for the appearance of fake electric fields inherent to the modeling of asymmetric systems with periodic boundary conditions. In-plane, most calculations are usually restricted to a (2×1) Si reconstruction and supercell; this is compatible with the formation of Si dimers at the Si surface but cannot accommodate eventual antiferrodistortive motions in the perovskite, which would at least require a (2×2) supercell. It also implies ideal interfaces without any kind of defect. The in-plane lattice constant of the supercell is fixed, in practice, to that of bulk Si, a_{Si}, in order to impose an epitaxial strain $\varepsilon = (a_{Si} - a_{STO})/a_{STO}$ on the perovskite. Such a strain on Si is about −1.5% for STO but close to −4% for BTO. Hence, the latter grows better on Ge and requires the inclusion of an appropriate buffer layer on Si.

Calculations are typically performed using conventional local-density approximation (LDA) or generalized gradient approximation (GGA) exchange–correlation functionals, which provide self-consistent treatment of electronic and structural degrees of freedom at reasonable computational costs.[136] Despite their success, these approximate functionals have, however, their own limitations. They show small errors on lattice constants (typically ~1%–3%) that can be different for different classes of compounds. This means that they qualitatively but not always exactly nor similarly reproduce the epitaxial strain condition. Calculations are, moreover, restricted to zero Kelvin so that they neglect the eventual structural phase transition of the perovskite with temperature and do not include thermal expansion and concomitant evolution of strain conditions. LDA and GGA also systemically underestimate bandgaps,[142] which is sometimes problematic for estimating band alignment.[143] These points are further addressed below. Although many studies of the Si/STO interface have been reported, the comparison between them and with experiment should always be taken with care since many distinct atomistic models of the interface can be considered and properties strongly depend on the specific choices.

B. Structural and functional properties

One of the main goals of the Si/ABO_3 interface is to achieve direct integration of the multifunctional properties of oxides into electronic devices. As mentioned before, STO being one of the most popular substrates for the growth of perovskite films, the Si/STO system can be considered as an ideal passive prototypical template for the further growth of other functional perovskites.

However, STO is already active by itself. It is antiferrodistorted below 105 K. It also shows a large dielectric constant related to an incipient ferroelectric behavior. Its ferroelectric transition is suppressed at the bulk level by both the appearance of competitive antiferro-distortive motions[144] and quantum fluctuations,[145] but it can eventually be made ferroelectric under epitaxial strains. *A priori*, the compressive epitaxial strain imposed by Si (~−1.5%) is large enough to put STO into the ferroelectric regime.[146] This was, for instance, supported experimentally by Woicik *et al.*[147] who reported a *c/a* ratio in STO compatible with an out-of-plane polarization or Warusawithana *et al.*[6] who reported piezo-force microscopy (PFM) contrasts in line with the presence of ferroelectric domains in Si/STO films. However, theoretical investigations by Kolpak *et al.*[148] suggest that although STO on Si is polar, ferroelectricity (i.e., polarization switching) is suppressed by interfacial effects.

In their works, Kolpak *et al.*[148,149] investigated various models of the Si/STO interface, varying both the interface layer and first oxide layer and reported some rather universal properties. First, there is a transfer of electrons from the more electropositive Si and Sr interfacial atoms to the more electronegative O atoms of the first oxide layer so that the interface bonding is primarily ionic in nature. Then, this electron transfer gives rise to a robust rumpling in the first oxide layer with cations and O atoms repulsed from and attracted by the positive interface, respectively, giving rise to a polarization

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oriented from the Si substrate to the top surface. The energetics of this interface effect is much larger than that of the ferroelectric instability so that it produces a strong pinning of the polarization inside the STO film and prevents further ferroelectric switching. This interface pinning should progressively weaken as the film thickness increases. Using a Landau–Ginzburg–Devonshire model, Kolpak *et al.*[148] predicted that ferroelectric switching would only become possible above a critical thickness of about 20 nm, at which STO films grown epitaxially on Si are, however, no longer under compressive strain and so no more ferroelectric. Hence, no ferroelectric regime is *a priori* expected. In a further study, Yu *et al.*[150] confirmed that predominantly ionic interfaces prevent polarization switching but predicted that in alternative atomic arrangements promoting a more covalent bonding, a ferroelectric behavior can reappear. Similar predictions were made at the Si/BTO interface.[139] We note that those studies neglected the competition of ferroelectricity with oxygen rotation motions.

In practice, DFT calculations allow to explore and relax various hypothetical atomistic models of the interface and to provide images that can be directly compared to scanning transmission electron microscope (STEM)[138,148] or scanning tunneling microscope (STM)[151] images. As such, they also play a key role to help interpreting experimental observations and determine the atomic structure of the considered interface.

C. Electronic properties and band-offsets

A key feature of the interface for device applications is the band alignment between Si (E_g = 1.1 eV) and STO (E_g = 3.2 eV)[149] that governs the electronic properties of the heterostructure and the possible injection of carriers from one material to the other. The band-offset at interfaces is sometimes roughly estimated from the difference of electron affinities of both related bulk materials, but, in practice, it also strongly depends on the chemistry of the interface and, in particular, of the interface dipole. Theoretical determination of band-offsets thus mandatorily requires proper quantum modeling of the interface at the atomic scale. This can be practically achieved from DFT calculations but with the shortcoming that usual local approximations (LDA and GGA) strongly underestimate bandgaps (typically by 30%–50%), which can sometimes lead to pathological situations.[143,152] In practice, the bandgap problem is often empirically corrected by shifting up rigidly the conduction bands to reproduce the correct bandgap.[149,153] This implicitly assumes, however, that DFT errors on valence band edges are the same in both materials, which might be true, but it is not guaranteed when considering dissimilar materials such as Si and $SrTiO_3$ with distinct valence states. A better estimate would require the use of computationally more intensive approaches such as hybrid functionals[154] or GW corrections.[155]

Kolpak and Ismail-Beigi[149] compared the band offsets at the Si/STO interface associated with various atomic arrangements. On the one hand, for arrangements with 1 ML Sr atom interface layers that are in line with experimental observations, the valence band edge of STO appears located about 2.0 eV below the valence band edge of Si so that conduction band edges of both materials are almost aligned. This is similar to the previous DFT estimate by Zhang *et al.*[133] and in the range of experimental measurements.[156–158] On the other hand, for other atomic arrangements with 1/2 ML Sr atoms at the interface layer and/or further addition of O atoms, the valence band offset is reduced so that the conduction band offset increases. This is consistent with a decrease in the interface dipole pushing down the STO states. These alternative interfaces do not seem, however, compatible with what is observed experimentally. We note that the absence of a significant barrier for electrons at the direct Si/STO interface was anticipated by Robertson and Chen;[159] it can be overcome by the inclusion of a buffer layer with a sufficiently large bandgap if required for some electronic applications[153,160] or can be an asset for photocatalysis applications, as previously discussed.

VII. CONCLUSIONS

Epitaxial growth of ferroelectric oxides on silicon is experimentally very delicate since the reaction between the deposited material and Si needs to be kinetically trapped. With optimized growth parameters, the high crystalline quality of an oxide layer can be achieved with a minimum thickness of the interfacial layer, which is crucial for the electronic coupling between the constituents.

High quality, dense PZT films can be grown on Si using various nucleation layers. The resulting variation in the values of piezoelectric parameters can be explained in terms of small differences in the porosity of the films, resulting in changes in the elastic parameters of the film. The differences in piezoelectric parameter values of dense PZT thin films on Si are relatively small, and there appears little room for much increase in $d_{31,\mathrm{eff}}^{cl}$. An interesting result is that the value of $d_{33,\mathrm{eff}}^{cl}$ can be varied over a fairly large range by varying film porosity, which opens perspectives for applications that use the “piston” motion of capacitor structures, as, for example, in wavefront correction in extreme ultraviolet optics.[161,162] The discussion here is limited to PZT thin films, which appear to show somewhat larger piezoelectric properties than in dense, lead-free,[163,164] or relaxor[165] clamped, near-epitaxial films. From the perspective of applications, it is important to note that there is a lack of studies on the stability of the different films under the operational conditions of a specific device.

Ferroelectric oxides on silicon also offer a disruptive alternative to enhance functionalities in electro-optical components. The technology is now coming to a new level of maturity and will revolutionize integrated photonics, a key technology for future ICT. Having a new class of materials integrated in this platform will also trigger innovation based on novel functionalities (e.g., bistability) that has been rarely investigated for optical devices. Finally, engineering ferroelectrics will enable scientists to tune electro-optical properties, e.g., through strain engineering.

Oxide-semiconductor integration has demonstrated a promising route to photoelectrochemical water splitting. However, the realization of the ferroelectric/semiconductor material system for catalysis is challenging and relies on the direct contact between the materials, proper engineering of the band structure to facilitate efficient carrier transport, and the need of a co-catalyst integration. In this regard, first-principles calculations are considered as a promising tool to get an insight at the atomic scale of the system to help interpreting experimental data, as well as to chemically tune the corresponding interface.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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[166]The subindices indicate that the field E is in the 3-direction (z-direction), i.e., normal to the film, while the strain is in the 1- and 2-direction (x- and y-direction) in the plane of the film.
[167]However, in the above axis definition, it should be, strictly speaking, the d_{11} mode. For cubic symmetry, the piezoelectric parameters d_{33} and d_{11} are equal. However, for clamped films, this is not necessarily and even likely to be the case.
[168]Since one is not interested in thickness changes, the indentation effect is not so relevant for the determination of d_{31}. In addition, the domain structure does not play a role in the effective value of d_{31}, although hard clamping and domain wall motion are taken into account.[75]
[169]The tabulated samples from Refs. 52 and 54 are for very comparable samples with a 50 nm nucleation layer, 100 nm electrodes, and a 1 μm PZT. All devices were made by the same researcher using the same deposition and patterning technologies (PLD for oxide layers and sputtering for the Pt layers).
[170]Note that there is a significantly lower saturation polarization of the films on Pt compared to those on oxide nucleation layers (not shown in table), although all films are subject to the same in-plane tensile stress. This suggests increased polarization rotation into the plane for the first group of films. We speculate that it might be due to charged grain boundaries. However, this polarization difference is not reflected in very different values of the piezoelectric parameters for comparable films.
[171]Although the monolithic integration of silicon compatible light sources is a field of intense research—e.g., using Si–Ge–Sn alloys—well-established packaging solutions can be used to integrate III–V laser diodes.

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