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Fully-Integrated Dickson Converters for Single Photon Avalanche Diode Arrays

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ABSTRACT This paper presents a novel low EMI technique to regulate the output voltage of fully-integrated switched capacitor Dickson type step-up DC/DC converters for SPAD arrays implemented in the Silterra 0.13 μm HV-CMOS process. SPAD sensors are extremely sensitive to EMI and therefore require careful biasing. This design utilises current sources to limit the current flow into the flying capacitors altering the converter ratio and reduces the discontinuous pulse currents associated with capacitive converters. A variable voltage-controlled reference current enables output voltage regulation. The proposed four stage converter boosts 3.3 V up to an adjustable 15 V output voltage. A typical Dickson converter regulated by frequency control and the proposed current controlled converter were designed and manufactured to compare performance. Measurements confirm that the proposed design reduces the output ripple by more than 2 V when compared to the typical converter. The inclusion of the proposed voltage regulation technique reduces EMI which enables this fully-integrated Dickson charge pump to bias sensor arrays where the noise typically produced by these converters currently restricts or prohibits their use.

INDEX TERMS SPAD sensors arrays, integrated charge-pump, current control, voltage regulation, monolithic switched-capacitor dc-dc converters, switching noise, Dickson charge pump.

I. INTRODUCTION

SINGLE Photon Avalanche Diodes (SPADs) require a high reverse bias voltage to be applied to generate a sufficiently high electric field for single photon detection [1]. This bias voltage can exceed 15 V depending upon the process technology in order to generate an electric field strength of $> 3 \times 10^8\ V/m$ [2]. This is significantly higher than the typical supply voltage of deep sub-micron CMOS technologies. To minimise total system area a high efficiency fully integrated converter is proposed to generate this voltage on chip. Switched capacitor (SC) DC/DC converters provide better performance than inductor based converters when fully integrated [3]–[5]. As this application requires a high power density, efficient, fully-integrated power converter, a SC converter is very suitable.

SPAD imaging integrated circuits (ICs) require additional front-end circuitry, such as active quenching systems and counters, benefiting from the advantages of very low supply voltages used in modern CMOS technology [6]–[10]. However, SPADs operate with an applied bias voltage well above the breakdown of the P-N junction which varies with temperature and process and is therefore the bias voltage is required to be precisely adjustable [11]. The key performance metric of the proposed voltage regulation method to bias SPAD sensors is a very low output voltage ripple. SPAD sensor performance is extremely sensitive to bias voltage changes and therefore the output ripple of the converter is required to be kept to a minimum. These sensors present a difficult load to precisely regulate due to the SPAD avalanche pulses resulting in very high instantaneous currents and an average current that strongly depends upon the illumination level. This SPAD image sensor benefits from the advantages of the implementation of fully-integrated switched capacitors DC/DC converters where multiple rails are required to be independently controlled, providing highly efficient, tightly regulated, low noise supplies [3]. The inclusion of a fully-

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integrated SC converter enables the image sensor to be supplied by a single external supply rail reducing the total camera system size.

Chip area is a significant factor in the cost of the full integration of SC DC/DC converters. The Dickson charge pump topology is a fully-integrated step up switched capacitor DC/DC converter [12]. This topology suits applications where high voltage gain and lower current drive are required [13]. Evaluation of the total required capacitance and hence area used for a given voltage gain shows that the Dickson topology is equivalent on an area-cost metric to the series-parallel and Fibonacci topologies and superior to the voltage doubler [4]. Traditional Dickson charge pumps either run open-loop, where the output voltage is determined by the number of stages and the load current, or closed loop voltage regulation using frequency control, where the switching frequency limits the charge flow through the converter. Switched capacitor converters are able to be modelled through their output impedance [14]. This impedance causes the output voltage of the charge pump to decrease as load current increases.

A number of previous designs have utilised charge pumps to generate the required high SPAD bias voltage [15]–[23]. The majority have been used to bias arrays of a small number of sensors where the maximum avalanche current is very limited [15]–[18]. A larger 1024 pixel array of SPADs was biased using a Dickson doubler hybrid topology converter capable of supplying up to 550 mA. However this converter was not fully-integrated [22]. A SPAD voltage generation circuit based upon that proposed in [16] was used to supply a 67,392 sensor array [23]. This fully-integrated converter was able to produce a maximum voltage of 25 V at a load current of 1.4 mA. The converter proposed in the present work are designed to supply a 64x48 SPAD image sensor array requiring an increase in maximum current output in comparison to these previous fully-integrated implementations whilst providing reduced voltage ripple.

This paper compares the performance of the proposed fully-integrated charge pump DC/DC converter to a typical design manufactured in the Siltera 0.13 μm HV-CMOS process for the application of biasing SPAD sensor arrays. This paper proposes a voltage regulation method using current control to set the bias voltage of the SPAD sensors dynamically. The proposed converters utilises a current control technique to regulate the output voltage. This technique has advantages over the conventional frequency voltage regulation scheme resulting in improved regulation, lower output voltage ripple and reduced conducted emissions. A typical Dickson SC converter was also designed and manufactured to enable direct measurement of the performance with the proposed current controlled converter. This paper is organised as follows: Section II gives an overview of the proposed converter topology and the current controlled voltage regulation mechanism. Section III discusses the implemented device and Section IV presents results with measurements showing a greater than 4 V reduction of output voltage ripple when compared with the conventional topology. Section V discusses the design and potential alternative methods to achieve low voltage ripple. Section VI concludes the paper and highlights the improved performance of the proposed converter

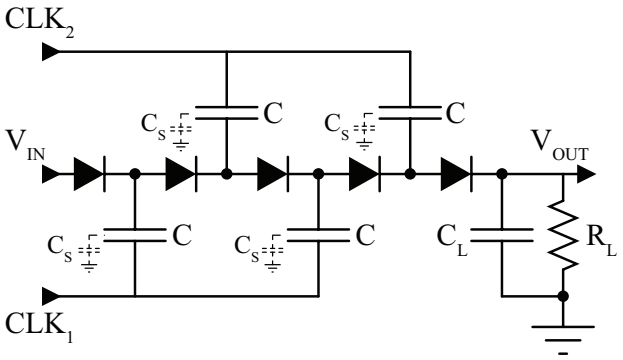

FIGURE 1: Typical four stage Dickson topology charge pump schematic [12].

II. FULLY-INTEGRATED DICKSON CHARGE PUMP

A. DICKSON CONVERTER

The Dickson topology switched capacitor converter is an established method for generating high voltages on chip [12]. The voltage multiplier uses a series of diodes to isolate the flying capacitors through which the clock cycles are coupled to the chain [24]. A schematic of a traditional four stage Dickson topology converter is shown in Fig. 1. The output voltage, V_{OUT}, for a given input voltage, V_{IN}, for a N stage charge pump is [12]:

$$V_{OUT} = V_{IN} - V_D + N\left[\left(\frac{C}{C+C_S}\right).V_\phi - V_D\right] \quad (1)$$

where V_D is the forward bias diode voltage, V_ϕ is the voltage swing, C is the flying capacitor and C_s is the stray capacitance at each node. From (1) it can be observed that V_D has a significant impact on the voltage gain possible per stage and should be kept to a minimum.

The Dickson topology produces a fixed voltage gain per stage with a theoretical N × V_ϕ voltage gain [5]. The control and clock switching circuitry is not subjected to supplies of higher than V_{IN} enabling the use of the core voltage devices throughout the design.

Voltage ripple at the clock switching frequency is present at the output due to the output capacitor, C_L, being discharged by the load, R_L, during the non-conduction period of the final diode stage in each cycle. The output ripple is given by

$$V_{PP} = \left(\frac{NC}{C+C_S}+1\right)V_\phi - (N+1)\,V_D - \frac{NI_{PP}}{f\,(C+C_S)} \quad (2)$$

where f is the switching frequency and I_{PP} is the steady-state current transfer [25].

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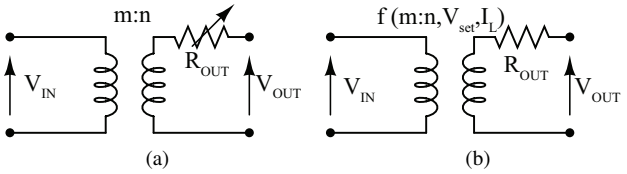

FIGURE 2: Switched capacitor equivalent models for (a) the traditional fixed ratio design, and (b) current controlled design [14].

A fundamental parameter in the voltage gain expression in one Dickson charge pump stage is the ratio between the flying capacitor, C, and its parasitic capacitance, C_S. In bulk CMOS processes, C_S is a capacitance formed between the lower flying capacitor plate and substrate generally tied to ground. To minimise this stray capacitance, the distance between the plates and substrate should be maximised while the area of the capacitances should be minimised. The proportion of this parasitic capacitance to the flying capacitance is larger in fully integrated CMOS implementations due to relatively small value in comparison with external capacitances. This impacts the voltage gain and maximum efficiency of fully integrated converters.

Since the capacitors are directly charged/discharged by other capacitors or voltage sources, large transient current spikes can occur, reducing the efficiency of the converter. These transient effects increase the device stress and cause EMI [26]. Reduction of these transients present in the typical Dickson converter have been shown to produce higher efficiency and lower emissions compared with the traditional design [26]. Other techniques to reduce the output ripple, for example the use of an output buck converter, are not feasible for full integration due to the limited quality and large area of on-chip inductors.

B. VOLTAGE REGULATION EQUIVALENT MODEL

As presented in [14], Fig. 2a shows an ideal model of a switched capacitor DC-DC converter. The converter can be modelled as an ideal DC transformer and conversion losses being replaced with a variable output impedance. This resistive output-impedance accounts for charge transfer and conduction losses present throughout the converter. Additional sources of losses in these converters are not included in this model are: short circuit conduction, parasitic capacitance and gate drive losses. The output impedance sets the maximum converter output power and also determines the open loop properties [14].

1) Frequency Control

Voltage regulation using the ideal model (Fig. 2a) is expressed as the voltage division between the output impedance, R_{OUT}, and the load impedance, R_L. Due to the switching nature, the converter is able to operate in the slow switching limit as introduced by [14]. In this mode the output impedance can be increased by slowing the switching frequency, reducing the output voltage of the converter. Due to the fixed fundamental conversion ratio, $m : n$, of the converter this reduction in switching frequency has a resultant increase in output ripple. As analysed in [13], the output voltage produced by the converter has a constant value where the large voltage ripple is produced during the conduction and blocking periods of the final stage of the converter. The output load is charged only during the conduction period and discharged through the load continuously. The voltage ripple present at the load changes with changing switching frequency. A schematic of the typical frequency controlled Dickson topology charge pump is shown in Fig. 3. In this voltage regulation method, an error amplifier controls the clock switching frequency through a voltage controlled oscillator [13].

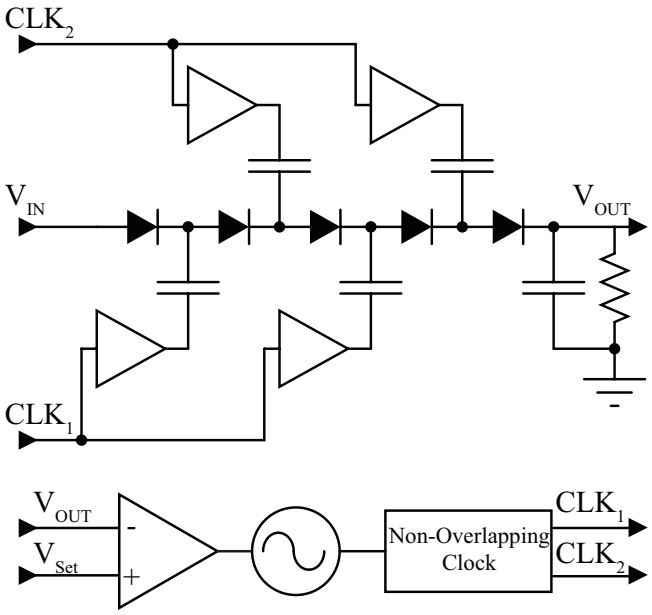

FIGURE 3: Typical four stage frequency controlled Dickson converter schematic. The oscillator, control and clock buffers are supplied by V_{in}.

2) Current Control

The proposed Dickson topology based charge pump uses a current control method to regulate the output voltage. An ideal model of this scheme is shown in Fig. 2b. The technique was first proposed with an unregulated Dickson charge pump used to drive a linear regulator pass transistor [27]. Other current-controlled methods have been successfully used to minimise conducted emissions including a design implementing a shunt regulation system which dynamically adjusts the floating ground voltage keeping the output voltage fixed [28]. This was first implemented as a technique to regulate the output voltage in a voltage doubler [29]. The effective conversion ratio of the converter is fixed by design. The implementation of the current control system enables variation

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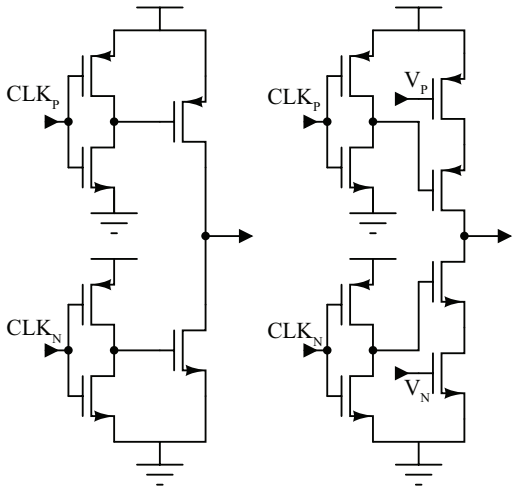

FIGURE 4: Schematic of (a) typical and (b) current starved clock buffers.

of the clock swing voltage, V_ϕ, giving a resulting variable conversion ratio for a given switching clock frequency. V_ϕ is therefore a product of the set voltage, V_{SET}, and the load current, $I_L = V_{OUT}/R_L$. Eq. (1) can be therefore rewritten as

$$V_{OUT} = V_{IN} - V_D + N\left[\left(\frac{C}{C+C_S}\right).V_\phi\left(V_{SET}, I_L\right) - V_D\right]. \tag{3}$$

This current control is achieved by replacing a traditional clock buffer, shown in Fig. 4a, with a current starved clock buffer, as shown in Fig. 4b. In this design two current control voltages, V_P and V_N, are supplied from the voltage-controlled current control circuit shown in Fig. 5. A control voltage V_{CTRL}, is used to control the current flow of both the N and P current limiting devices. These current control voltages depend upon the converter load for a given set voltage. For the current controlled voltage regulation method, the converter operates at the externally set switching frequency which is fixed during operation. The error amplifier in this topology feeds back V_{CTRL} into the voltage controlled current control block. The overall block diagram of the current regulated Dickson charge pump is shown in Fig. 6. The typical waveform for the clock swing voltage for various output voltages into a fixed load is shown in Fig. 7. For low output voltages the current control limits the clock voltage swing which reduces the voltage gain per stage. As the required output voltage increases the current control increases the maximum per stage clock voltage swing to increase the voltage gain per stage to approximately that of the conventional frequency controlled implementation.

3) Other Voltage Regulation Techniques

Other mechanisms to regulate the output voltage are altering the fundamental converter ratio, (N), changing the diode drop, (V_D), changing the flying capacitor size, (C), or adjusting the input voltage, (V_{IN}), which alters the flying capacitor voltage, (V_ϕ). Each of these mechanisms either require significant additional circuitry or are impractical to be implemented in a physical design.

Flying capacitor size modulation was used in conjunction with frequency control to supply a SPAD sensor array [16]. Digital control of both the flying capacitance and switching frequency enabled voltage regulation across load currents. Voltage ripple control was implemented as part of the output voltage regulation in [30]. The design enabled the disabling of three quarters of the converter capacity to reduce ripple

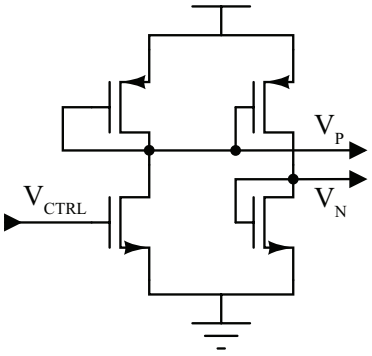

FIGURE 5: Voltage controlled current control schematic.

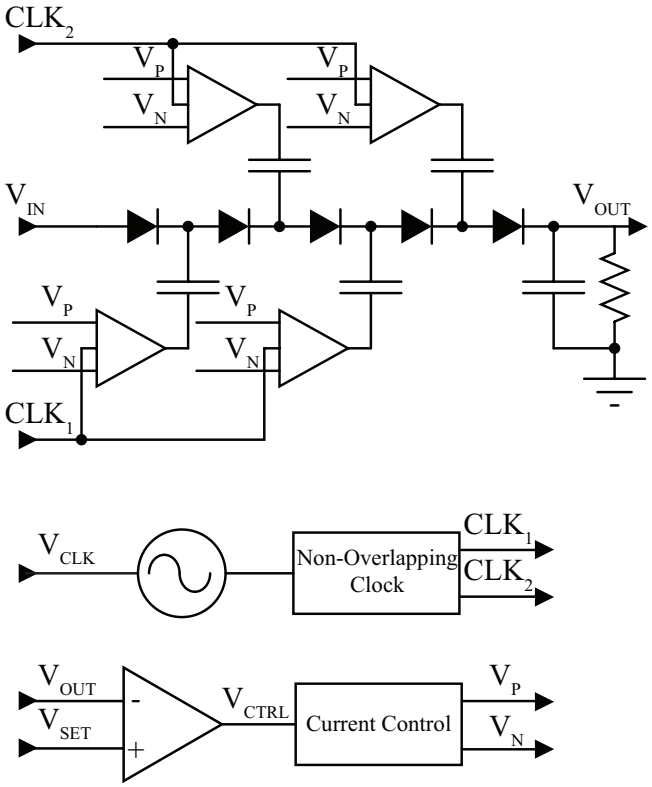

FIGURE 6: Proposed four stage Dickson based current controlled converter schematic. Oscillator, control and clock buffers are supplied by V_{in}.

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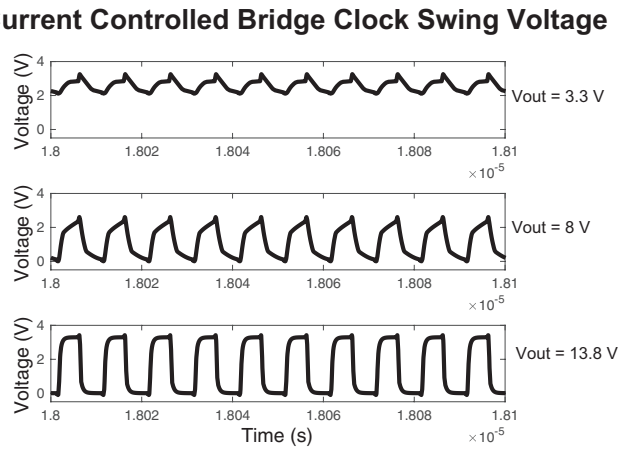

FIGURE 7: Proposed four stage Dickson based current controlled converter clock swing voltage for different output voltages.

when lightly loaded. These designs require significant additional circuitry when compared to the proposed current control implementation.

C. EFFICIENCY COMPARISON

There is a trade-off between the maximum efficiency of the converter and the produced voltage ripple. The current control method for regulating the output voltage dissipates more power in the current limiting clock buffer compared to the traditional design due to the switches being in the linear region for a longer period. Conventional switched capacitor DC/DC converters have a fixed output voltage and are unregulated [5]. Unlike methods that regulate the output voltage in inductor-based DC-DC converters, the regulation schemes employed by SC DC/DC converters designed to achieve output voltages less than the conversion ratio are lossy. Output voltage above the required value is dropped across a regulating element which reduces the efficiency [31].

III. PROPOSED CONVERTER

A four stage Dickson based DC/DC converter using the proposed current control technique was designed in a Silterra 0.13 μm HV-CMOS process. A four stage typical frequency controlled variant was also manufactured to enable direct comparison of performance. This CMOS process contains triple well, thick gate medium voltage rated MOSFETs from which this converter was designed. Both converters utilise the same switches, error amplifier and clock generation circuits which were designed using 3.3 V tolerant devices. A symmetrical operational transconductance amplifier (OTA) was used as the error amplifier which includes resistive divider to attenuate the output voltage used in the feedback path.

The symmetrical OTA was designed with a NMOS output buffer. A Miller capacitor was used to limit the unity gain bandwidth of the amplifier to ensure that the converter was stable. The OTA has an open loop gain of 74 dB, a gain bandwidth of 45 kHz and operated with a phase margin of 84°.

The ladder pass diodes were constructed from 6 V tolerant devices. The 85 pF per stage flying capacitors were implemented as 5 metal layer finger capacitors offering the highest capacitance per unit area available in this process at a sufficiently high breakdown voltage. These metal-metal capacitors have a low substrate capacitance of 3 % [27].

The switches and flying capacitors have been sized for a maximum output power of 3 W. Each stage was equally sized. The distribution of the two phase clock was through tapered clock buffers. Gate drive buffers were sized suitably for the main flying capacitor switches. Matching of the transistors in the current controlled bridge and OTA was very important. The mirrored currents in the current controlled bridge must be well matched to ensure the current starved clock buffers are equally controlled. The input to the OTA and current controlled bridge are also sensitive to noise so care was taken to isolate these nodes from the noise sources. The parasitic capacitance of the flying capacitors and connected metal was minimised through layout.

A micro-photograph of the manufactured devices as well as the layout is shown in Fig. 8. This integrated circuit contains a number of SPAD imaging arrays as well as the DC/DC converters supplying the former. The area used by each of the two DC/DC converter designs is 0.56 mm^2.

A. BLOCKING DIODE DESIGN

Increasing the number of stages in the converter should result in a greater output voltage being generated. In CMOS processes, breakdown voltage limitations of capacitors and isolation junctions restrict the maximum voltage. Fig. 9 shows a cross section of the diode used in these converters. A triple well process was used with the desired junction formed between the N+ cathode and medium voltage P-Well anode. This junction can withstand the 6.6 V maximum voltage reverse bias that can be applied by two consecutive stages. The body terminal is modulated to minimise the threshold voltage of the diode though the body modulation effect. Effectiveness of the body effect is limited in this topology as the threshold for each stage is different due to the different voltage applied to each stage [12]. The maximum breakdown voltage of the deep N-Well to P-Well is larger than the output voltage of this converter. The body terminal in the proposed design is connected to the output voltage preventing forward biasing of these parasitic junctions.

IV. MEASUREMENT RESULTS

The frequency controlled and current controlled Dickson based converters were fabricated and tested to compare their performance. A current voltage transfer plot is shown in Fig. 10. It can be observed that the maximum output voltage of the current controlled design is lower than the typical frequency controlled design. This reduction is due to the maximum clock voltage swing, V_ϕ, being lower than the frequency-controlled design due to the voltage drop across

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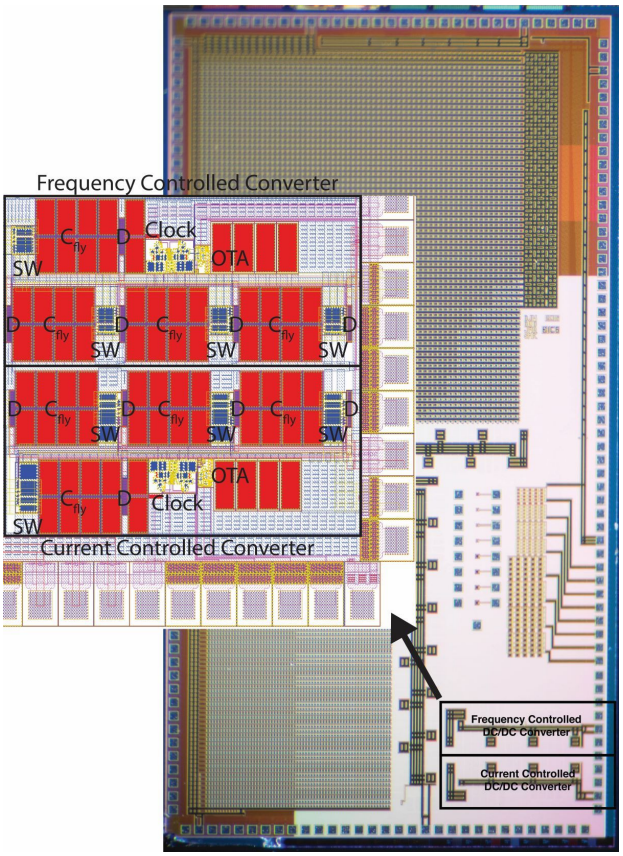

FIGURE 8: Micro-photograph with DC/DC converters labelled and the layout insert. The layout has the major constitute block labelled as following: C_{fly} are flying capacitors, D are the blocking diodes, SW are the flying capacitor switches, Clock is the clock generating circuitry and OTA is the error amplifier.

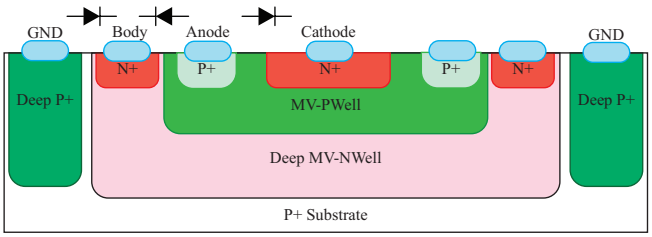

FIGURE 9: Diode cross section. Breakdown voltage for cathode to anode diode is 12.5 V, body to substrate diode is 61.5 V and the body to anode diode is 19.5 V.

the current control devices in the current starved clock buffer. This also translates to a lower maximum output current of 120 mA compared to 200 mA for the frequency controlled design.

A. OUTPUT VOLTAGE RIPPLE

The key performance metric required this proposed voltage regulation method to bias SPAD sensors is a very low output voltage ripple. The reason for this is that SPAD sensors are

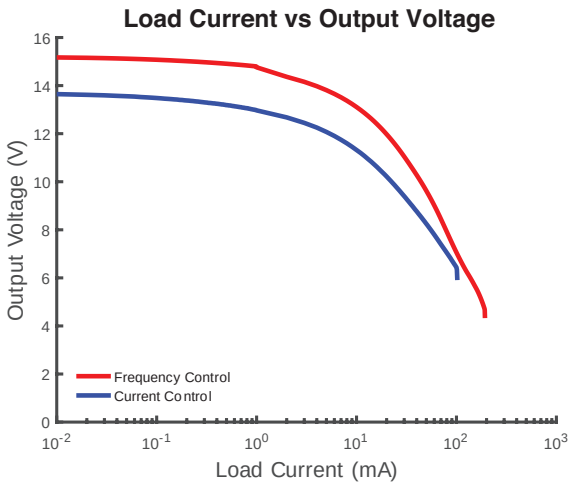

FIGURE 10: Output current with respect to output voltage plot for the proposed current controlled and typical frequency controlled converters.

extremely sensitive to bias voltage change and therefore output ripple must to be kept to a minimum. This is particularly the case for low supply currents typically at bias voltages less than the breakdown point.

Figure 11a shows the output voltage ripple for the typical frequency regulated converter for an output voltage of 12 V into a load current of between 1 μA and 1 mA. This output voltage was chosen as a typical operating point. The behaviour of the converters is similar throughout the output voltage range. The low current ripple is dominated by the ripple produce by the slow switching speed of the converter to maintain a regulated output voltage.

These results are as expected for a converter operating at the slow switching limit. As the load current is increased towards the maximum of the converter, the output ripple voltage does decrease. This does not resolve the requirement of precise regulation as the SPAD array will require a wide range of load current requirements due to changing ambient light conditions and hence event rates.

Figure 11b, shows the output voltage ripple from the proposed current regulated converter for an output voltage of 10 V and load current of between 1 μA and 1 mA. The impact of the current control technique was evaluated at three switching frequencies to demonstrate its impact upon the output voltage ripple. These measurements show that the voltage ripple is significantly lower than the frequency controlled implementation particularly at higher output load currents. Peak to peak voltage ripple was measured for a 1 mA load to be 0.25 V_{PP} and 0.20 V_{PP} for a 1 μA load.

Maximum efficiency operation does not necessarily correspond to the maximum switching frequency. Reducing the maximum switching frequency to a point between the fast switching limit and slow switching limit would reduce dynamic switching losses. This extra degree of freedom presented by the adjustable switching frequency enables optimi-

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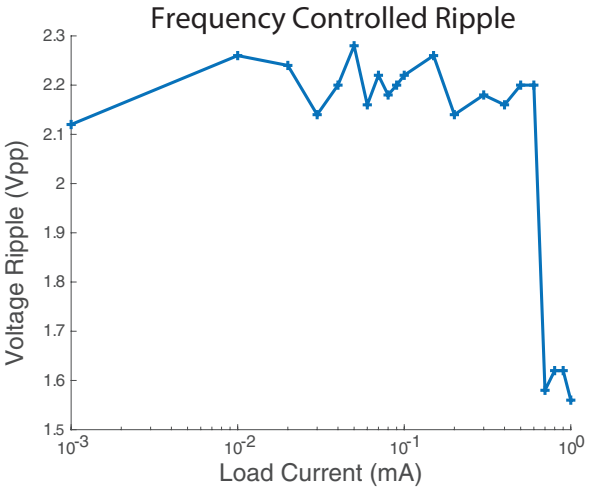
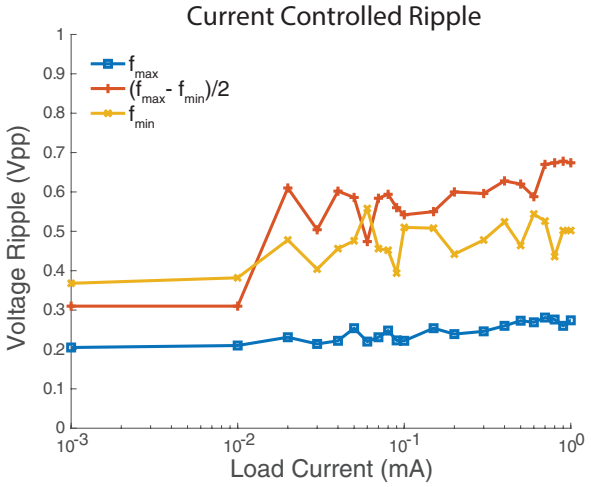


(a)



(b)

FIGURE 11: Output voltage ripple for (a) the frequency controlled Dickson converter and (b) the proposed current controlled Dickson based converter. F_{max} = 100 MHz and F_{min} = 20 MHz for this design.

sation of the converter performance for system requirements.

B. POWER EFFICIENCY

A comparison between the efficiency across operating point for the proposed current controlled Dickson based charge pump and the typical frequency controlled charge pump is shown in Fig. 12. There is a negligible maximum efficiency penalty between the current control and the typical control mechanisms. The difference in peak efficiency is close to 9 %. The decrease in efficiency can be attributed to the current starved clock buffers, increasing switching losses and reducing the maximum voltage gain of the converter. These measurements were taken across the operating range of the clock frequency for the proposed current controlled converter and supply voltage with the maximum efficiency configuration for a given load current plotted.

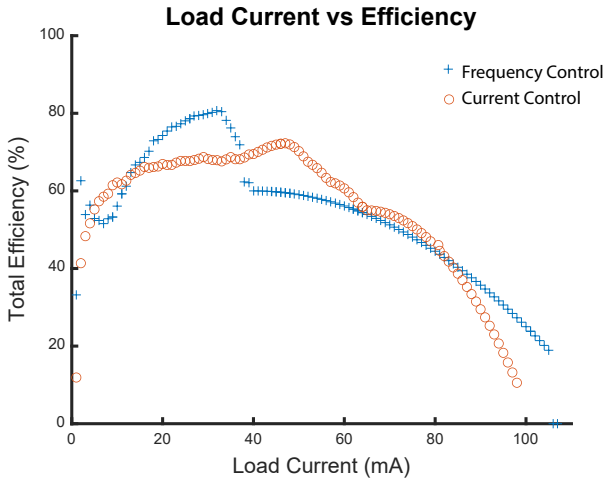


FIGURE 12: Efficiency comparison between proposed current controlled Dickson based converter and the frequency controlled Dickson charge pump.

V. DISCUSSION

The proposed current controlled Dickson based converter produces a reduced output ripple whilst switching at a fixed clock frequency. This switching frequency is externally set by a control voltage.

The mechanism of the reduction of the output voltage ripple by the proposed current controlled Dickson based converter in comparison to the frequency controlled Dickson converter is through the varying of the fundamental conversion ratio of the converter chain. The voltage gain of each stage is able to be varied through the current control to reduce the gain at each stage in order to achieve voltage regulation at a higher switching frequency than if the converter operated at a fixed conversion ratio. This higher switching frequency and variable voltage gain results in lower reliance on the output impedance of the converter dividing the output voltage with the load to achieve regulation.

When compared to the state-of-the-art the converters compare favourably, as shown in Table 1. Direct comparison of the performance of the proposed converter to these other designs is difficult due to the significantly different implementation, operating specifications and technology used. Integrated SC converters have been used to bias SPAD sensor arrays previously. Fully-integrated designs have been of limited number of pixels and therefore significantly lower maximum output current than what is required here. The Dickson doubler hybrid topology design presented in [22] was not fully-integrated, but is the most similar design in terms of number of pixels. This design has a much larger voltage ripple than the proposed design. The fully integrated Dickson converter presented in [17] produces a similar bias voltage but operates at a much higher switching frequency. The converter supplies an array of 9 pixels and used almost double the area of the proposed design.

For the optimum efficiency the switching frequency of the

TABLE 1: Performance Comparison with State of the Art

Parameters	[27]	[15]	[22]	[16]	[17]	[18]	Typical Frequency	Proposed Current
Process Technology	0.35μm BiCMOS	0.35μm CMOS	0.35μm CMOS	90nm CMOS	90nm CMOS	0.13μm CMOS	0.13μm CMOS	0.13μm CMOS
Topology	Dickson	Dickson Doubler Hybrid	Dickson Doubler Hybrid	Dickson	Doubler	Dual Phase Dickson	Dickson	Dickson Based
Level of Integration	Fully Integrated	Not Fully Integrated	Not Fully Integrated	Fully Integrated	Fully Integrated	Fully Integrated	Fully Integrated	Fully Integrated
Application	NMOS LDO	SPAD Bias	SPAD Bias	SPAD Bias	SPAD Bias	SPAD Bias	SPAD Bias	SPAD Bias
SPAD Sensor Pixels	-	1	1024	9	3	1	1960	1960
Number of Stages	2	1	4	11	5	12	4	4
Input Voltage	12 V	3.3 V	3 V	3.3 V	2.5 V	1.8 V	3.3 V	3.3 V
Maximum Output Voltage	24 V	12.4 V	40.4 V	25 V	10.9 V	22 V	15 V	13.8 V
Maximum Output Current	50 μA	25 μA	550 mA	100 μA	-	100 μA	200 mA	120 mA
Clock Frequency	6 MHz	-	-	43.7 MHz-1.2 GHz	700 kHz	100 MHz	20-100 MHz	20-100 MHz
Flying Capacitance (per stage)	-	10 nF	-	1.64 pF	1.6 pF	800 fF	85 pF	85 pF
Total Area	-	0.315 mm^2	1.4 mm^2	1.008 mm^2	0.0192 mm^2	0.149 mm^2	0.56 mm^2	0.56 mm^2
Maximum Efficiency	-	-	-	-	-	46 %	81 %	72 %
Voltage Ripple	-	750 mV_{PP} (70 V 4.6 mA)	5.5 V	110 mV_{PP}	100 mV_{PP}	1.4 V_{PP}	2.2 V_{PP} (10 V 1 mA)	250 mV_{PP} (10 V 1 mA)
Voltage Ripple Maximum Output Voltage	-	2.14 %	13.6 %	0.9 %	1.8 %	13 %	29 %	3.6 %

converter should vary depending upon its operating conditions. A number of previously proposed converters operate using a dual-mode control loop enabling the use of both switching frequency control and another mechanism [30]. A future design could include a similar control scheme to optimise efficiency across operating points.

Multi-phase interleaved converters have been implemented successfully previously and have produced a reduced output voltage ripple [3] [32].

The ripple reduction provided by the current controlled Dickson based converter is achieved at low load currents typically encountered when the SPAD sensor array is exposed to low illumination levels or when the array is biased below the breakdown voltage. At this low avalanche rate the variation of the applied bias voltage due to the voltage ripple would correspond to a wide fluctuation in detection performance.

The proposed current controlled Dickson based converter has some implementation disadvantages compared to existing methods. The converter requires a larger area than the typical frequency controlled design due to the additional switching devices used. The efficiency of the converter is reduced due to the lossy regulation method. The output ripple produced by the converter is higher than produced by the alternative topology of switching converter followed by linear regulator. The proposed design has a significant advantage over alternative topologies as it does not requiring the use of integrated inductors. Careful consideration of the optimal implementation is required to maximise converter design.

VI. CONCLUSION

This paper presents a novel technique to regulate the output voltage using current control for a fully-integrated step-up DC/DC converter for SPAD arrays. The proposed four stage converter boosts 3.3 V up to an adjustable 15 V output voltage to bias the SPAD sensors. SPAD sensors are very sensitive to small changes in applied bias voltage and therefore require a low voltage ripple supply. The proposed design utilises current sources to limit the current flow into the flying capacitors altering the converter ratio and reducing the discontinuous pulse currents associated with capacitive converters. The proposed Dickson based current controlled converter reduces the output ripple at least 2 V when compared to the conventional design. A negligible peak efficiency penalty is associated with the proposed regulation technique.

REFERENCES

[1] C. Niclass, et. al., *A Single Photon Avalanche Diode Implemented in 130-nm CMOS Technology*, IEEE J. Sel. Topics. Quantum Electron., vol. 13, no. 4, July/Aug. 2007, pp. 863-869.

[2] F. Zappa, et. al., *Principles and Features of Single-Photon Avalanche Diode Arrays*, Sens. Actuators A, Phys, vol. 140, issue. 1, October 2007, pp. 103-112.

[3] S. Sanders, et. al., *The Road to Fully Integrated DC-DC Conversion via the Switched-Capacitor Approach*, IEEE Trans. Power Electron., vol. 28, no. 9, Dec. 2012, pp. 4146-4155.

[4] T. Van Breussegem, et. al., *Area-Driven Optimisation of Switched-Capacitor DC/DC Converters*, Electronics Letters, Vol. 44, No.25, Dec. 2008, pp. 1488-1490.

[5] M. Forouzesh, et. al., *Step-Up DC-DC Converters: A Comprehensive Review of Voltage Boosting Techniques, Topologies and Applications*, IEEE Trans. Power Electron., vol. 32, no. 12, Dec. 2017, pp. 9143-9178.

[6] F. Zappa, et. al., *Monolithic Active-Quenching and Active-Reset Circuit for Single-Photon Avalanche Detectors*, IEEE J. Solid-State Circuits, vol. 38, no. 7, July 2003, pp. 1298-1301.

[7] A. Ximenes, et al., *A Modular, Direct Time-of-Flight Depth Sensor in 45/65-nm 3-D-Stacked CMOS Technology*, IEEE J. Solid-State Circuits, vol. 54, no. 11, Nov. 2019, pp. 3203-3214.

[8] F. Della Rocca, et al., *A 128×128 SPAD Motion-Triggered Time-of-Flight Image Sensor With In-Pixel Histogram and Column-Parallel Vision Processor*, IEEE J. Solid-State Circuits, vol. 55, no. 7, July. 2020, pp. 1762-1775.

[9] S. Hutchings, et al., *A Reconfigurable 3-D-Stacked SPAD Imager With In-Pixel Histogramming for Flash LIDAR or High-Speed Time-of-Flight Imaging*, IEEE J. Solid-State Circuits, vol. 54, no. 11, Nov. 2019, pp. 2947-2956.

[10] D. Morrision, et al., *A 64×64 SPAD Flash LIDAR Sensor Using a Triple Integration Timing Technique with 1.95 mm Depth Resolution*, IEEE Sensors Journal, Oct. 2020.

[11] P. Chang et. al., *Constant Excess Bias Control for Single-Photon Avalanche Diode Using Real-Time Breakdown Monitoring* IEEE Electron Devices Letters, vol. 36, no. 8, June. 2015, pp. 859-861.

[12] J. Dickson, *On-chip High-Voltage Generation in NMOS Integrated Circuits Using an Improved Voltage Multiplier Technique*, IEEE J. Solid-State Circuits, vol. 11, no. 3, Jun. 1976, pp. 374-378.

[13] J.Y. Lee, et. al. *A Regulated Charge Pump with Small Ripple Voltage and Fast Start-Up*, IEEE J. Solid-State Circuits, vol. 41, no. 2, Feb. 2006, pp. 425-432.

[14] S. Seeman and S. Sanders, *Analysis and Optimization of Switched-Capacitor DC-DC Converters*, IEEE Trans. Power Electron., vol. 23, no. 2, March. 2008, pp. 841-851.

[15] M. Al-Rawhani, et. al., *Photocurrent Dependent Response of SPAD Biased by a Charge Pump*, 2011 IEEE International Symposium on Circuits and Systems (ISCAS), Rio de Janeiro, Brazil, May 2011.

[16] S. Mandai, and E. Charbon, *A 3.3-to-25 V All-Digital Charge Pump Based System with Temperature and Load Compensation for Avalanche Photodiode Cameras with Fixed Sensitivity*, Journal of Instrumentation, vol. 8, March. 2013.

[17] B. Shen, S. Bose and M. Johnston, *On-Chip High-Voltage SPAD Bias Generation Using a Dual-Mode, Closed-Loop Charge Pump*, 2017 IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, MD, USA, May 2017.

[18] R. Henderson, et. al., *A 3×3, 5 μm pitch, 3-Transistor Single Photon Avalanche Diode Array with Integrated 11 V Bias Generation in 90 nm CMOS Technology*, 2010 International Electron Devices Meeting, San Francisco, CA, USA, Dec. 2010.

[19] B. Shen, S. Bose and M. Johnston, *Fully-Integrated Charge Pump Design Optimization for Above-Breakdown Biasing of Single-Photon Avalanche Diodes in 0.13 μ m CMOS*, IEEE Trans. Circuits and Systems I, vol 66, no 3, March 2019.

[20] B. Shen, S. Bose and M. Johnston, *A 1.2 V-20 V Closed-Loop Charge Pump for High Dynamic Range Photodetector Array Biasing*, IEEE Trans. Circuits and Systems II, vol 66, no 3, March 2019.

[21] H. Ouh, B. Shen, and M. Johnston, *Combined In-Pixel Linear and Single-Photon Avalanche Diode Operation With Integrated Biasing for Wide-Dynamic-Range Optical Sensing*, IEEE J. Solid-State Circuits, vol 55, no 2, Feb 2020.

[22] M. Al-Rawhani, J. Beeley and D. Cummings, *Power Management System for a Capsule Endoscope using Autofluorescence Imaging*, 2014 IEEE International Symposium on Circuits and Systems (ISCAS), Melbourne, Australia, June 2014.

[23] A. Carmiatto, et. al., *A 67,392-SPAD PVTB-Compensated Multi-Channel Digital SiPM with 432 Column-Parallel 48 ps 17 b TDCs for Endoscopic Time-of-Flight PET*, 2015 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, Feb. 2015.

[24] J. Witters, G. Groeseneken, H. Maes, *Analysis and Modelling of On-Chip High-Voltage Generator Circuits for use in EEPROM Circuits*, IEEE. J. Solid-State Circuits, Vol. 24, No. 5, May 1989, pp. 1372-1380.

[25] T. Tanzawa, *An Optimal Design for Integrated Switched-Capacitor Dickson Charge Pump Multipliers with Area Power Balance*, IEEE Trans. On Power Electronics, vol. 29, no. 2, Feb. 2014, pp. 534-538.

[26] Y. Lei, R. May, and R. Pilawa-Podgurski, *Split-Phase Control: Achieving Complete Soft-Charging Operation of a Dickson Switched-Capacitor Converter*, IEEE Trans. On Power Electronics, vol. 31, no. 1, Jan. 2016, pp. 770-782.

[27] J. Wittmann, J. Neidhardt, and B. Wicht, *EMC Optimized Design of Linear Regulators Including a Charge Pump*, IEEE Trans. Power Electron., vol. 28, no. 10, Oct. 2013, pp. 4594-4602.

[28] F. Biziitu, *Dickson Charge Pump Regulation Mechanism Optimised for EMC Performance*, 2015 International Semiconductor Conference (CAS), Sinaia, Romania, Dec. 2015, pp. 193-196.

[29] S. Kennedy, M. Yuce, J.-M. Redouté, *A Low EMI Fully-Integrated Switched-Capacitor DC/DC Converter* IEEE Trans. Electro. Compat., vol 60, no. 1, Jan. 2018, pp. 225-233.

[30] T. Van Breussegem, and M. Steyaert, *A Fully Integrated Gearbox Capacitive DC/DC-Converter in 90 nm CMOS: Optimisation, Control and Measurements*, 2010 IEEE 12th Workshop on Control and Modelling for Power Electronics (COMPEL), Boulder, CO, USA, June 2010.

[31] G. Villar-Pique, H. Bergveld and E. Alarcon, *Survey and Benchmark of Fully Integrated Switching Power Converters: Switched-Capacitor Versus Inductive Approach*, IEEE Trans. Power Electron., vol. 28, no. 9, Sept. 2013, pp. 4156-4167.

[32] L. Chen and D. Ma, *Design of Monolithic All-NMOS Three-Level Three-phase Switched-Capacitor Power Converter for Industrial Environmental Sensor Conditioning*, IEEE Transactions on Industrial Electronics, vol. 67, no. 11, Nov. 2020, pp. 9873-9881.

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