Experimental and simulation study of the Schottky barrier lowering by substrate doping variation for PtSi Source/Drain SBFETs

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***Abstract*— In this paper, we study experimentally and numerically the Schottky barrier height (SBH) lowering of Pt silicide/*n*-Si diodes and its implications to Schottky-barrier (SB) source/drain *p*-FETs. We demonstrate that hole SBH can be lowered through an image-force mechanism by increasing the *n*-Si substrate doping, which leads to a substantial gain of the drive current in the long-channel bulk *p*-SBFETs. Numerical simulations show that the channel doping concentration is also critical for short-channel *n*- & *p*- SOI SBFETs performance.**

I. INTRODUCTION

Silicide source/drain (S/D) Schottky barrier field-effect transistors (SBFETs) are promising candidates for sub- 32nm CMOS technology [1-4], as the silicide S/D can provide abrupt junctions together with lower serial resistance as compared to conventional doped S/D junctions. One of the key challenges in SBFETs is to obtain a low Schottky barrier height (SBH) at the silicide-channel junction [2]-[3]. PtSi/$YbSi_{1+x}$ were considered to be among the best silicide materials for *p*-/ *n*- SBFETs application, due to their relative low hole/ electron SBH [4].

Recently, different approaches have been proposed to reduce the electron SBH, e.g. by inserting a thin insulator layer [3] or by creating a highly doped region located at the silicide/Si interface with a dopant segregation technique [5]-[6]. To our knowledge, no such reports were available for hole SBH modulation. In this paper, we experimentally demonstrate that hole SBH of PtSi/*n*-Si diodes could be lowered through an image-force mechanism [7] by increasing the *n*-Si substrate doping, which leads to a substantial gain of the drive current in the long-channel bulk *p*-SBFETs. Numerical simulations show that the substrate (channel) doping is also critical for short-channel bulk & SOI SBFETs performance improvement. SBH modulation method proposed in this work only relies on the conventional CMOS process techniques such as well ion implantation (I/I), and thus is very attractive for future SBFETs development.

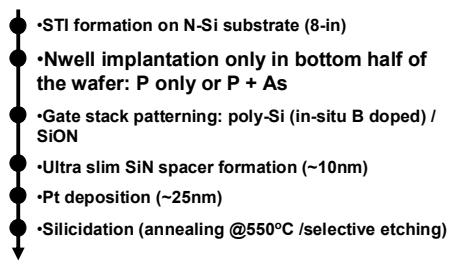

Figure 1. *Process flow for the fabrication of Schottky barrier FET. Gate length and gate with are 1μm.*

II. DEVICE FABRICATION

The SBFETs device (W/L=1μm/ 1μm) fabrication process is depicted in Fig. 1. Note that only bottom part of the wafers received the well I/I: either P (3e12 cm^{-2}, 120KeV) or P (3e12 cm^{-2}, 120KeV) + As (1e12 cm^{-2}, 90KeV). Here we define bottom part as south well, and top part as north well in the following text. The simulated dopant profile of the south well with the 2 different splits is reproduced in Fig. 2 (a). CV measurements of MOS capacitors (data not shown) indicates a substrate doping level of 1e16 cm^{-3} in the north well and of 8e16 or 2e17 cm^{-3} in the south well respectively with P or P+As I/I. The EOT of SiON extracted from CV for the SBFETs is ~ 2nm. XSEM of a SBFET with PtSi S/D (~50nm in depth, consistent with 1Å Pt + 1.32Å Si -> 2.0Å PtSi) is presented in Fig. 2 (b). A slim SiN spacer (~11nm) is used in our work to enhance the device drive current [8]. XSEM shows that the S/D silicide reaches the gate edge due to a lateral diffusion of the PtSi under the SiN spacer.

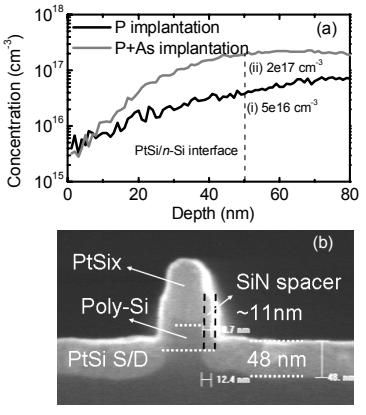

Figure 2. *(a) Dopant concentration in the south well in the case of 3e12 cm^{-2} – 120 KeV P implantation and 3e12 cm^{-2} – 120 KeV P + 1e12 cm^{-2} – 90 KeV As implantation. The PtSi/n-Si interface is located at 48 nm in depth. (b) XSEM of the SBFET.*

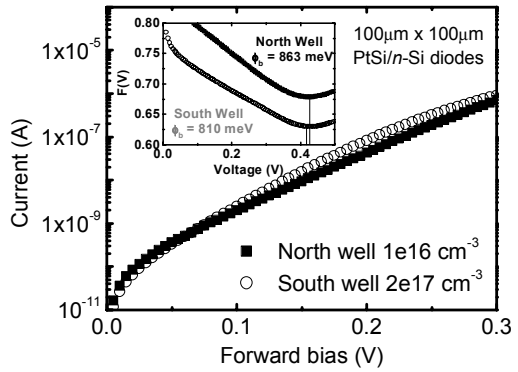

Figure 3. *IV characteristics of PtSi/n-Si diodes. The substrate doping is 1e16 cm^{-3} (square) and 2e17 cm^{-3} (circle). Inset shows the corresponding Norde function F(V). Extracted electron barriers (ϕ_b) are 863 meV (north well) and 810 meV (south well).*

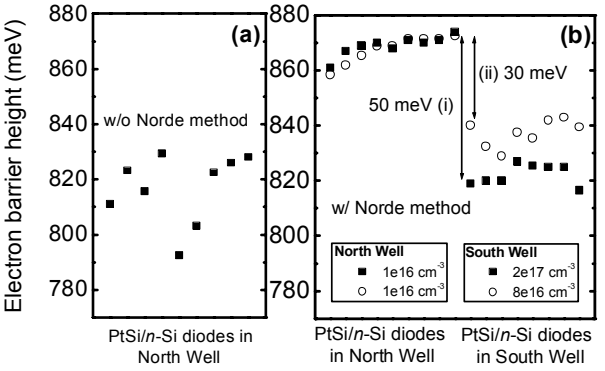

Figure 4. *Electron barrier heights extracted without (a) and with (b) Norde method of PtSi/n-Si diodes located on a straight line in the wafer. The n-type bulk Si substrate has a dopant concentration of 1e16 cm-3 (north well), 8e16 cm-3 (circle in south well) and 2e17 cm-3 (square in south well).*

III. EXTRACTION OF SBH

We use the diode forward current-voltage (I-V) for the SBH extraction [7]. Fig. 3 shows typical I-V curves measured from two diodes (100μm x 100μm) in wells with different dopant concentration. Considering the possible high series resistance, we adapted a method initially given by Norde[9]. The electron SBH (ϕ_e) was thus extracted from the minimum value of the Norde function F(V) (inset of Fig.3)

$$F(V) = \frac{V}{2} - \frac{kT}{q}\ln\left(\frac{I}{AA^{**}T^2}\right) \Rightarrow \phi_e = F(V_{\min}) + \frac{V_{\min}}{2} - \frac{kT}{q} \qquad (1)$$

A set of extracted electron SBH of PtSi/n-Si diodes is plotted in Fig. 4. SB diodes were measured in a statistical manner, i.e. they lie on a north-to-south straight line in the wafer. Comparison of the SBH extracted w/ or w/o considering Norde model [Fig. 4 (a)-(b)] justifies the Norde model used in this work for SBH extraction. In Fig. 4 (b), it is seen that the electron SBH distribution of the north well diodes is tight and has an average value close to 870 meV. In the south well, the values of the SBH are a function of the doping concentration: the average value is around 840 meV for the 8e16 cm^{-3} doped substrate and 820 meV when the doping concentration is 2e17cm^{-3}. Note that the extracted SBHs show more fluctuation in the south well. The PtSi thickness variations in the non-uniformly doped substrate [see Fig. 2 (a)] are suspected to be the reason for these SBH fluctuations. It is expected that they could be minimized by improving PtSi thickness variations.

The electron SBH is reduced by ~30 meV and ~50 meV respectively when the doping level rises from 1e16 cm^{-3} to 8e16 cm^{-3} and 2e17 cm^{-3}. This lowering may be caused by the electrostatic image-force attracting the carriers to the metal and therefore decreasing the electric field repealing the carrier from the interface [7]. As sketched in Fig. 5, this would result in a reduction of the effective electron and hole SBH (ϕ_{e0} and ϕ_{h0}). According to the image-force lowering model ($\Delta\phi = 2\sqrt{qE_{\max}/16\pi\varepsilon_s}$) [7], we have calculated from MEDICI simulation [10] the SBH lowering corresponding to the maximum electric field value at the interface (E_{max}), and the data are summarized in Table 1. It is seen that the simulations are in excellent agreement with our measurement data. We should also note that the electric field increases with the forward voltage, and thus the effective SBH lowering calculated for relatively low voltage in Table 1 would be enhanced.

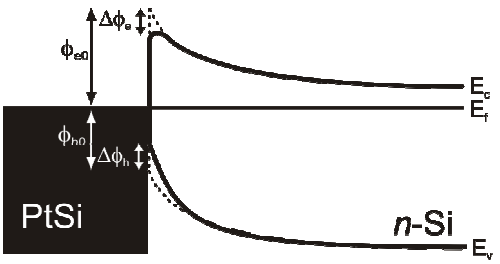

Figure 5. *Image-force SBH lowering $\Delta\phi_e$ and $\Delta\phi_h$ for the electron barrier height ϕ_{e0} and hole barrier height ϕ_{h0} [7]*

Doping (cm^{-3})	E_{max} at interface (V/cm)	*e*-SBH lowering by image-force	Calculated *e*-SBH difference	Measured *e*-SBH difference
1e16	*2e4*	*15.7 meV*	-	-
8e16	*1e5*	*39.3 meV*	*~25meV*	*30 meV*
2e17	*3e5*	*60.9 meV*	*~45meV*	*50 meV*

Table 1. *Simulated maximum electric field at the PtSi/n-Si junction, calculated electron SBH lowering by [7] and the calculated & measured [from Fig. 4 (b)] e-SBH difference from the 1e16 cm^{-3} doping level, for dopant concentrations of 1e16 cm^{-3}, 8e16 cm^{-3} and 2e17 cm^{-3}.*

IV. IMPACT OF THE BARRIER HEIGHT LOWERING ON SBFETS

The hole SBH lowering due to the image-force mechanism (see Fig. 5) would be expected to directly impact the performance of *p*-SBFET. The I_s-V_g and I_d-V_g of the *p*-SBFETs in the north well (1e16 cm^{-3}, circle symbols) and the south well (2e17 cm^{-3}, square symbols) are represented in Fig. 6 (a)-(b) respectively. Due to the drain junction leakage induced by the electron tunnelling, the $I_{d,off}$ is much larger than $I_{s,off}$. This leakage could be drastically reduced by using a SOI substrate [11]. For convenience of comparison, we will focus on the I_s-V_g analysis [Fig. 6 (a)]. The subthreshold slope *SS* of I_s-V_g of the SBFETs in the south well is ~ 70 mV/dec, with a I_{on}/I_{off} ratio ~ 10^7, demonstrating excellent electrical properties of PtSi S/D SBFETs fabricated in this work. Note that the DIBL value is reduced substantially with a high substrate doping (from 40 mV/V for 1e16 cm^{-3} to 5mV/V for 2e17 cm^{-3}). The reason behind is believed to be the much reduced lateral depletion region in the channel with high substrate doping.

In Fig. 7, after considering the SBH lowering effect, MEDICI simulation well matches the measured I_s-V_g of the SBFETs with a substrate doping of 1e16 cm^{-3}(b) and 2e17 cm^{-3}(a). The relative difference of SBH used for I_s-V_g simulation is again in good agreement with the 50 meV observed in the SBH extracted from the diode characteristic [Fig. 4 (b) & Table 1]. Thus, we believe the image-force barrier lowering effect [7] is responsible for the electron / hole SBH reduction observed in diode *I-V* / transistor I_s-V_g measurement respectively. However, we should mention that the model [7] predicts a slightly larger electron SBH lowering than the corresponding hole SBH lowering.

It is interesting to note the 2 different *SS* values measured in the I_s-V_g of the transistor in the north well, while there is only 1 *SS* for the one in south well. From simulation results shown in Fig. 8, it is observed that there is a change of the SS due to the high SBH, as SBH lowering modifies the curvature of the I_s-V_g curve at the transition from the subthreshold thermoionic emission to the field emission regime. Thus, it is believed that the increased effective SBH accounts for the 2 different *SS* observed in Fig. 7(b), confirming the previous report [11].

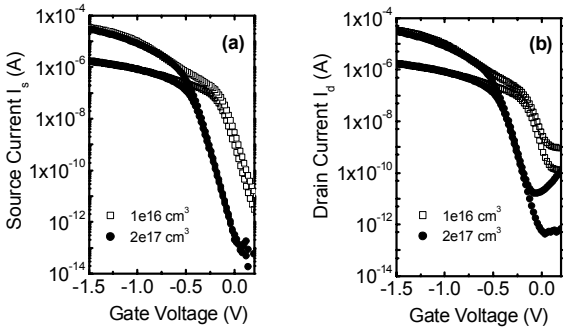

Figure 6. *Measured transfer characteristics of a 1μm-channel length SBFET at V_d=-0.05V and -1 V, on a substrate doping of 1e16 (square) and 2e17 cm^{-3}(circle). The source current is represented in the left panel (a) and the drain current in the right panel (b).*

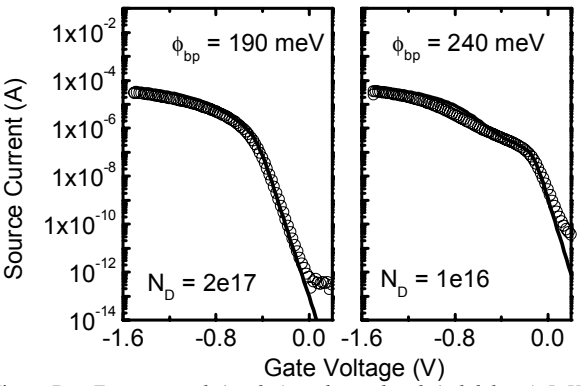

Figure 7. *Experimental (circles) and simulated (solid lines) I_s-V_g of p-SBFET with channel doping of 2e17 cm^{-3} (left panel) and 1e16 cm^{-3} (right panel). The hole barrier heights are respectively 190 meV for doping concentration of 2e17 cm^{-3} and 240 meV for 1e16 cm^{-3}. V_d = -1.1 V*

In Fig. 9, the measured output curve (I_s-V_d) for SBFETs (@ V_g-V_t= -1V) with 3 different substrate doping demonstrates the substantial gain of the drive current due to the high doping stemming from the SBH lowering effect. Note that a reduction of the hole mobility due to high substrate impurities tends to lower the drive current, but the overall effect of increasing substrate doping is to enhance the drive current through the image-force barrier lowering effect.

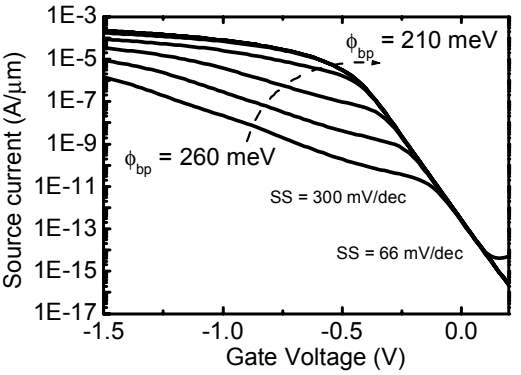

Figure 8. *Simulated transfer characteristics of a 1μm-channel length SSDT for hole barrier heights varying from 210 meV to 260 meV. Doping concentration is 1e16 cm^{-3}. Drain voltage is -1.1 V.*

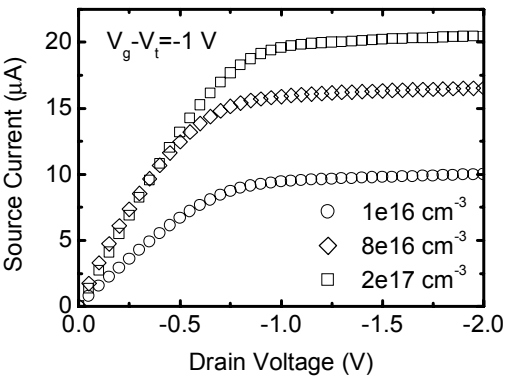

Figure 9. *Measured I_s-V_d of a 1μm-channel length SBFET on a substrate doping of 1e16 cm^{-3}(circle), 8e16 cm^{-3} (rhombus) and 2e17 cm^{-3}(square). V_g-V_t = -1V. V_t is defined as the voltage corresponding to a current of 10^{-8}A*

V. EXTENSION TO SHORT-CHANNEL SBFETS

The substrate doping concentration is also critical for the short channel SBFET performance. The simulated I_s-V_g (after offsetting the V_t difference, Fig. 10) of two SBFETs (with L_g =100 nm, and substrate doping of 1e16 and 1e18 cm^{-3} respectively) indicates higher drive current in the highly-doped SBFET, after considering the barrier lowering effect in MEDICI simulation. The similar simulation of two 100 nm channel length SBFETs on p- & n- SOI substrate brings identical conclusions [Fig. 11 (a)-(b)]. The observed relative larger I_s difference in bulk SBFET compared to the SOI one might be due to a device geography difference. Nevertheless, higher substrate doping is beneficial for device performance, on both bulk and SOI substrates.

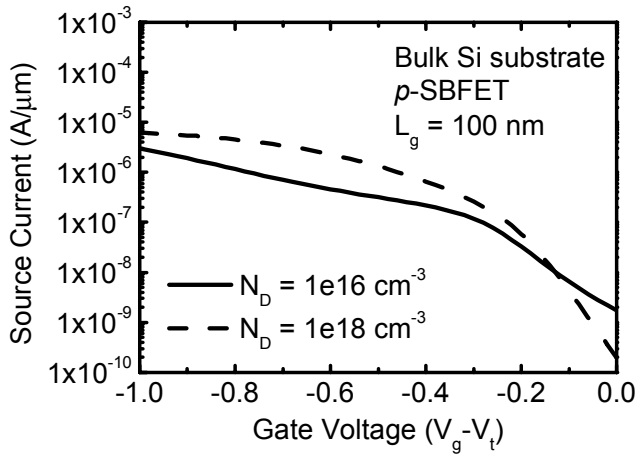

Figure 10. *Simulated transfer characteristics of a 100 nm-channel length PtSi S/D SBFET at V_{ds} = -0.1 V on a bulk substrate with a doping of 1e16 cm^{-3}(solid line) and 1e18 cm^{-3}(dashed line).*

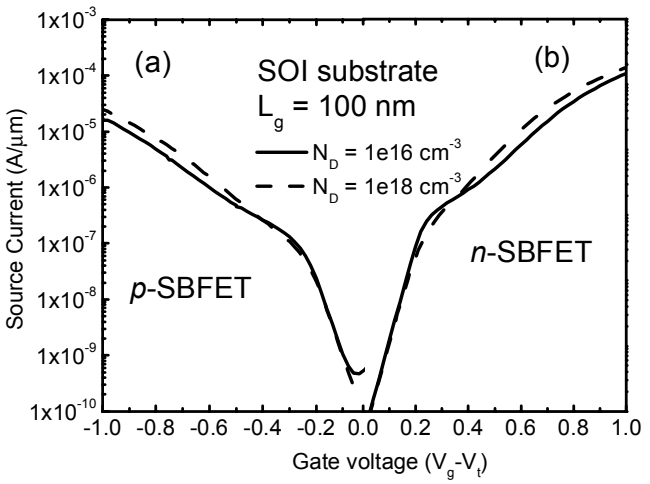

Figure 11. *Simulated transfer characteristics of a 100 nm-channel length PtSi (a) and $YbSi_{1+x}$ (b) SBFET at V_d = -1.1 V on a SOI substrate with a Si body doping of 1e16 cm^{-3}(solid line) and 1e18 cm^{-3}(dashed line). Si body thickness is 10 nm and silicide thickness is 4 nm.*

VI. CONCLUSION

In conclusion, we demonstrate that hole SBH can be lowered through an image-force mechanism by increasing the *n*-Si substrate doping, which leads to a substantial gain of the drive current in the long-channel bulk PtSi S/D *p*-SBFETs. Numerical simulations show that the channel doping concentration is also beneficial for short-channel bulk & SOI *n*- /*p*- SBFETs. It would be critical to adjust the well I/I for SOI SBFETs as well in order to improve its performance.

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