

# Experimental Validation of a Model Predictive Control Strategy on a Three-terminal VSC-HVDC Mock-up

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## Abstract

The subject of this paper is the experimental validation of a recently proposed advanced control scheme for Voltage Source Converters (VSC) based on Model Predictive Control (MPC). The main purpose of the investigated advanced controller is the frequency support from an AC grid to another after significant disturbance through HVDC Grid. The paper reports on the implementation methodology on a small-scale 3-terminal DC mock-up grid consisting of several physical low-scale VSCs, actual DC cables. These components are coupled with real-time simulation tools simulating the adjacent AC grids. The different steps for the validation process of the MPC strategy are illustrated, starting from offline simulation based on a model of the DC grid, up to the actual implementation of the controller in the mock-up of the DC grid.

## 1 Introduction

High Voltage DC (HVDC) transmission is becoming more and more attractive in the recent years, fuelled by the shift to renewable sources and the need for bulk power transfer over long distance. Most of the HVDC connections in operation today consist of point-to-point links. However, Multi-Terminal DC (MTDC) grids are also envisaged in the future after some challenges have been addressed [1]. Some MTDC grid projects such the European Supergrid [2] and the North Sea Super Grid [3] have already been proposed in Europe.

Unlike AC interconnections, HVDC interconnected areas operate asynchronously, i.e. the speed governors of one area do not respond to frequency deviations of the other areas. Therefore, no frequency support is provided between two AC asynchronous systems linked by HVDC system. This requires the development and integration of dedicated controllers for VSCs, which adjust the power transfer through the MTDC grid in response to frequency deviations.

Frequency support to an AC area through MTDC grid has been the subject of several works in the literature. In the majority of

them, a supplementary droop control is added to the control structure of VSC, enabling it to react to frequency deviations [4-7]. For MTDC grids, this results in the so-called dual droop control [8, 9]. However, as shown in [10], the drawback of the simple frequency droop is the strong interaction with its DC voltage droop counterpart, which has been shown to decrease the performances of both control strategies and in the worst case may lead to a DC voltage instability. To achieve the desired participation to frequency support, defined by the Transmission System Operator (TSO), the work in [11] proposes a simple method to retune the frequency droop parameter.

Instead of the dual droop control, the work in [12-14] proposed to use MPC to achieve the desired participation. This allows taking into account the expected effect of DC voltage deviations to the VSC power, as well as respecting DC voltage constraints. The main characteristic of MPC is that it solves a quadratic optimization problem with linear constraints at each sampling time step in order to calculate the control actions [15].

All of the aforementioned schemes have been tested with extensive offline dynamic simulations using simplified models of the VSC and the MTDC grid. However, some kind of experimental validation is required before applying such methods on real systems. Obviously, implementing and testing on real high-scale VSCs is not feasible. To this purpose, the authors of [16] proposed the use of Hardware In the Loop (HIL) and Power Hardware In the Loop (PHIL) simulation with a low-scale mock-up MTDC grid as an intermediate step. Initial results were obtained during the TWENTIES project [17], whereas the work in [18] provided experimental validation of the behaviour of the dual droop control of [11].

This study focuses on the implementation and experimental validation of the MPC-based method proposed in [12]. Compared to conventional linear control schemes (e.g. PI controllers, droop, etc.) this is much more challenging since it requires the formulation and solution of an optimization problem inside the control structure of the VSC. Thus, the main idea of this research work is to illustrate the different steps for the validation process of the MPC strategy, from the offline simulation based on a high-scale power MTDC system to a low-scale power MTDC Mockup. Therefore, a rigorous step-by-step validation method is performed starting from an

offline transient stability simulation software then describing the different stages under SimPowerSystem/Matlab, real time simulation environment, Hardware In the Loop (HIL) simulation and finally Power-Hardware-In-the-Loop (PHIL). The rest of the paper is organized as follows: Section 2 briefly describes the MPC-based strategy for AC frequency support originally proposed in [12]. Section 3 details the various steps followed for the implementation on the low-scale three-terminal mock-up. The results of the validation are analysed in Section 4. Concluding remarks are provided in Section 5.

## 2 MPC-based control strategy for AC frequency support

### 2.1 Description of the studied system

The three-terminal VSC-MTDC system under concern is depicted by the following Fig.1.

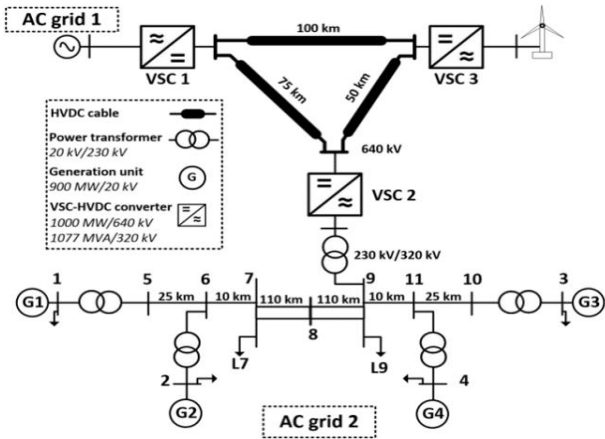


Figure 1: The studied three terminal MTDC System.

It consists of two AC areas (AC grid 1 and 2) and a large offshore wind. The wind farm is assumed to be located 100 km from AC grid 1 and 50 km from AC grid 2. The HVDC cable connecting AC grids 1 and 2 is 75 km. The three VSCs forming the MTDC grid have a nominal DC voltage of 640 kV and a nominal apparent power of 1077 MVA, i.e. a nominal active power of 1000 MW. The VSC 1 and VSC 2 operate in DC voltage droop mode. The offshore wind farm and VSC 3 inject constant power into the MTDC grid, thus not participating to DC voltage control. The AC grid 1 is modelled as an infinite bus. However, the AC grid 2 is based on the hereafter-called Kundur power system, detailed in [19]. It represents two AC areas connected by two long AC lines, whose lengths are shown in Fig. 1. There are four generators, each having a rating of 900 MVA and 20 kV [19, 20]. Then, following the tripping of a generator in this system, the frequency deviates from its nominal value, while the remaining adjust their mechanical power output to restore the equilibrium. The objective of the proposed control strategy is to support frequency when this kind of faults occurs. It is detailed in the next section.

### 2.2 Studied MPC control strategy

The method for frequency support proposed in [12] is considered as an “emergency” control scheme. For small frequency deviations, the controller is inactive and the VSC power command  $P^{cmd}$  is adjusted according to DC voltage deviations following a P-V droop characteristic as follows:

$$p^{cmd} = p^{set} - K_v(V - V^{set}) \quad (1)$$

where  $K_v$  the DC voltage droop gain,  $V$  the DC voltage of the VSC,  $V^{set}$  its corresponding setpoint.

As shown in Fig. 2,  $P^{cmd}$ , along with the reactive power command  $Q^{cmd}$ , is passed to the current controllers which adjust the signals sent to the modulation strategy of the converter. The VSC 2 is synchronized to the AC grid with a Phase Lock Loop (PLL). When a large enough frequency deviation is sensed through the PLL on the AC side of the VSC, the controller is activated and adjusts the power transfer through the MTDC grid to take advantage of the primary reserves of the other AC areas. The objective of the control is to provide in steady state a predefined participation to frequency support, as defined by a frequency droop gain  $K_f$ .

To achieve this, the power setpoint  $P^{set}$  of the VSC 2 is adjusted as shown in Fig. 2. First, measurements at time  $k$  of the DC voltage, power and frequency  $V^m(k)$ ,  $P^m(k)$  and  $f^m(k)$  are collected. Then a constrained-optimization problem is solved. The output is the setpoint change  $\Delta P^{set}(k)$ . The cumulative control changes are then added to the  $P^{set}$  of the VSC as shown in Fig. 2.

### 2.3 Constrained optimization problem

A constrained-optimization problem is the core of the studied MPC-based control. This allows computing a sequence of control changes that minimizes an objective function while satisfying various input and output constraints [15]. This optimization is based on simplified models for the MTDC grid, able to predict the future system evolution. The complete formulation is also included here for convenience. For more information on how the prediction models are computed, as well as definitions of the involved variables, readers are kindly referred to the original reference [12].

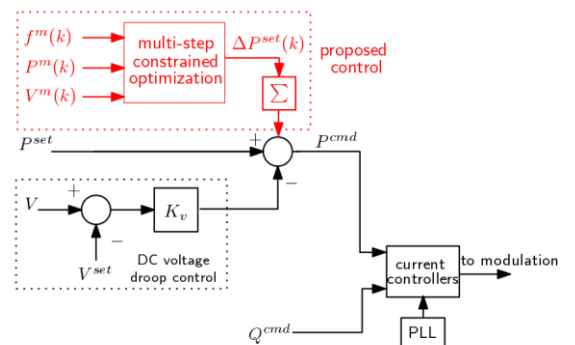


Figure 2: Control structure of VSC including MPC-based frequency support scheme.

The objective function consists of minimizing the deviations of the predicted VSC power from a pre-specified reference trajectory over the control horizon.<sup>1</sup>

$$\min_{P, \epsilon, V, \Delta P^{set}} w \sum_{j=1}^{N_c} [P^{set}(k+j) - P(k+j)]^2 + v \sum_{j=1}^{N_c} [\epsilon(k+j)]^2 \quad (2)$$

where  $w$  and  $v$  are weighting factors.

The minimization of (2) is subject to the following constraints for  $j = 1, \dots, N_c$ :

$$V^{min} - \epsilon(k+j) \leq V(k+j) \leq V^{max} + \epsilon(k+j) \quad (3)$$

$$P^{min} \leq P(k+j) \leq P^{max} \quad (4)$$

$$\epsilon(k+j) \geq 0 \quad (5)$$

$$V(k+j) = V(k+j-1) + s_v \Delta P^{set}(k+j-1) \quad (6)$$

$$P(k+j) = P(k+j-1) + \Delta P^{set}(k+j-1) - K_v(V(k+j) - V(k+j-1)) \quad (7)$$

Constraint (3) ensures that the DC voltage will not violate the security minimum and maximum limits  $V^{min}, V^{max}$ , respectively, while supporting frequency. Constraint (4) specifies that the VSC minimum and maximum power ( $P^{min}$  and  $P^{max}$ , respectively) are satisfied. Equality constraints (6)-(7) yield the predicted power and DC voltage in response to the control actions.  $\epsilon$  is a slack variable to relax output constraint (3) in case of infeasibility. Choosing a high value for the weighting factor  $v$  in (2) keeps the value of  $\epsilon$  as small as possible.

Note that the studied MPC-based control strategy is triggered when frequency exits a deadband (a value of  $\pm 100$  mHz has been taken) and remains active until frequency is restored inside a narrower deadband (e.g.  $\pm 10$  mHz).

### 3 Step-by-step implementation of MPC on low scale three-terminal VSC-HVDC Mockup

The general idea of this section is to explain the proposed methodology that has been developed starting from a High voltage offline simulation and ending in the real-time implementation on a low voltage DC mock up. So, two main steps have been identified such as the integration of the algorithm in C language in a real-time high voltage simulation, and the downscaling of the application to a low voltage MTDC grid.

#### 3.1 Validation of the MPC controller for High Voltage MTDC Grid

The behaviour of the controller has been tested with off-line dynamic simulations in Ramses, a FORTRAN-based dynamic simulation tool developed at University of Liege, which is mandatory for the designed real-time solver [21]. Before moving to the mock-up low-scale DC grid, some steps are required to validate the controller in the tools used by L2EP laboratory, as shown in Fig. 3.

1. The first step consists of the implementation of the whole system and the MPC-based control scheme in the Matlab/SimPowerSystem environment.
2. The second step involves the reformulation of the quadratic optimization control by using only inequality constraints. Then, the updated formulation of MPC-based scheme is implemented and tested under Matlab environment.
3. The last step concerns the implementation of the MPC controller in C language, necessary for implementation in the Digital Signal Processor (DSP) of the VSC. To accelerate the solution of the convex optimization problem, the solver accepts the optimization of the objective function under only inequality constraints.

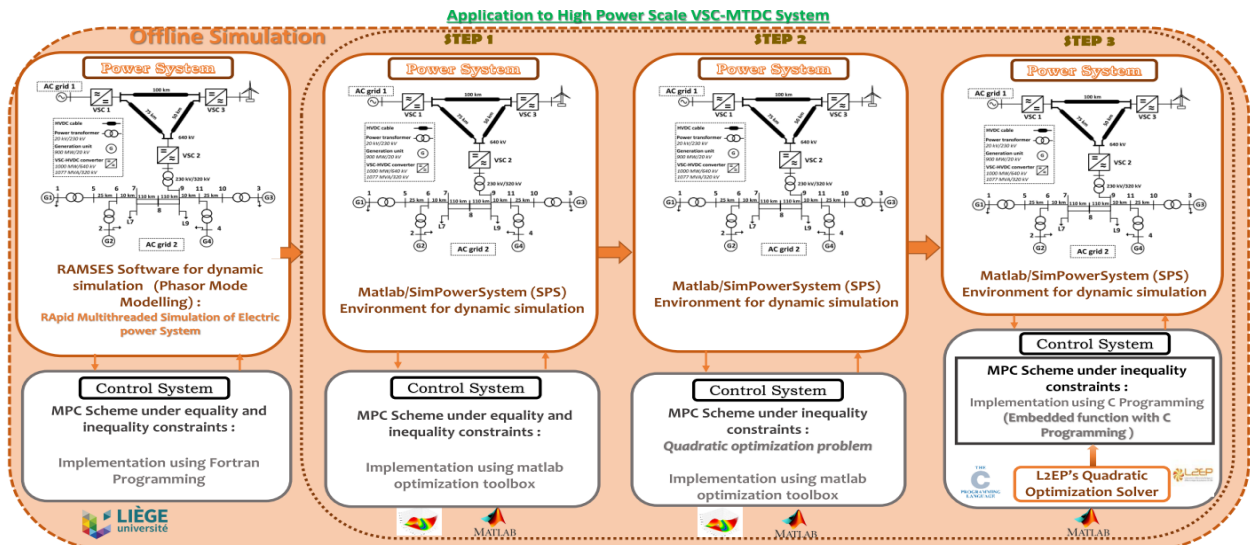


Figure 3: Different steps of MPC validation for high power scale studied system.

<sup>1</sup> here set equal to the prediction horizon

### 3.2 Validation of the MPC controller on low-scale MTDC mock-up

The next step is the validation of the controller on the low-scale mock-up configuration shown in Fig.4. The mock-up includes two main parts: (i) the physical part (in the middle of the figure below) and (ii) the virtual part implemented in a real-time simulator (highlighted in blue). The interface between the physical devices and the analogue outputs of the real-time simulator is achieved by high-bandwidth AC or DC power amplifiers. The VSC converters are 2-level converters with an LCL filter for mitigating the current harmonics on the AC side, and with a DC capacitor on the DC side. Each one is rated at 3.15 kVA / 200 V - 3 kW / 400 V. Three real DC cables are used to build the DC grid where the lengths are mentioned on the Fig.4. The reader is kindly referred to [16] for more details concerning this system.

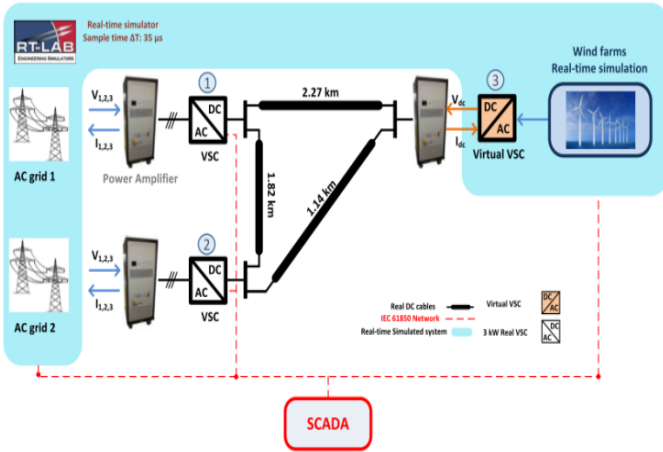


Figure 4: Mock-up general overview.

Four main steps are carried out in order to implement and validate the control on the mock-up:

**Step 1:** The first step validates the off line simulation of the MPC applied on the down scaled model of the system, As illustrated in Fig.5, the interface between the simulated low-scale DC grid and the high-power Kundur AC grid is performed through a homothetic gain  $G$ , equal to the ratio of the base power  $P_b^{high}$  of the high-scale system (i.e. the simulated system) over the base power  $P_b^{low}$  of the low-scale low scale physical system, i.e.:

$$G = \frac{P_b^{high}}{P_b^{low}} \quad (8)$$

#### Step 2: Full Real Time Simulation

The second step involves the full real-time simulation performed with a sampling time of 35  $\mu$ s using OPAL-RT and RTLab tools [22].

#### Step 3: HIL Simulation

The third step is HIL simulation. The MPC algorithm, as well as the low-level and high-level conventional VSC controllers, is implemented inside the DSP development kit. In this work, the DSP TMS320F28377D (Dual Core Delfino Micro Controller) is used. One core is used to solve the quadratic optimization problem of the MPC, whereas the second for the rest of the VSC controls. It has to be highlighted that the correct operation of the DSP requires good synchronization between both cores. The power part of the system is still simulated in real-time using OPAL-RT. It is important to mention that the CPU of the DSP runs on a 32-bit floating-point precision. The same precision is used for the solution of the MPC. This yields a computational time of 33 ms to solve the quadratic optimization scheme, well below the sampling time of the MPC (set to 250 ms).

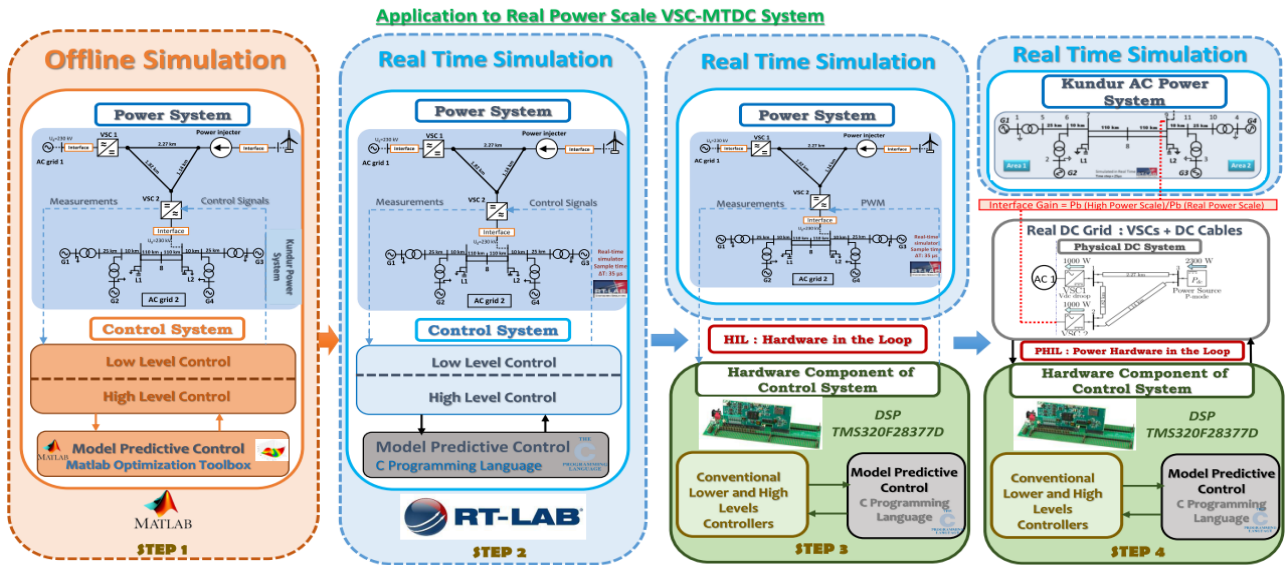


Figure 5: Steps description of MPC application to real power scale of 3 Terminal DC grid.



**Step 4: PHIL Simulation.** The last step concerns the validation of the controller using PHIL. This consists of using hardware components interacting with the external simulated systems. This last and most important step represents the practical test allowing the experimental validation of the studied advanced control strategy. More technical details concerning the PHIL step are available in [22].

#### 4 Experimental results based on mock-up MTDC grid using PHIL

This section presents the results of the last step i.e. the PHIL simulation depicted by the Fig. 6. The initial operating points for AC grid 2 and the MTDC grid are given in Table 1 and Table 2, respectively. The parameters of the MPC-based controller of VSC2 are given in Table 3. The controller is activated if the frequency measured by VSC2 exceeds a deadband of  $\pm 100$  mHz.

The experimental results following the tripping of generator G4 are shown in Figs. 7, 8 and 9, which show the frequency of AC grid 2, the DC powers of VSC1 and VSC2, and the MTDC grid DC voltages, respectively. Note that the frequency behaviour corresponds to the speed response of synchronous machine G1. Following the disturbance, the frequency starts decreasing and drops below the frequency deadband (i.e. 49.9 Hz). This activates the frequency support scheme of VSC2, which starts injecting more power in the AC grid. As shown in Fig.7, this support yields good performances in transient and steady state. The power requested by VSC2 is provided through the DC voltage droop mechanism by VSC1, which increases the power it injects into the DC grid, as shown in Fig. 8. It should be highlighted that the frequency support of VSC2 is somewhat “stalled” around 130 s. This is explained due to the DC voltage reaching its threshold  $V^{min}$ , hence preventing

Pmin (p.u)	Pmax (p.u)	Vmin (p.u)	Vmax (p.u)	Sv (p.u)	Kv (p.u)	Kf (p.u)
-1	1	0,90	1,1	0,4365	0,82	0,05

Table 3: Control parameters of MPC.

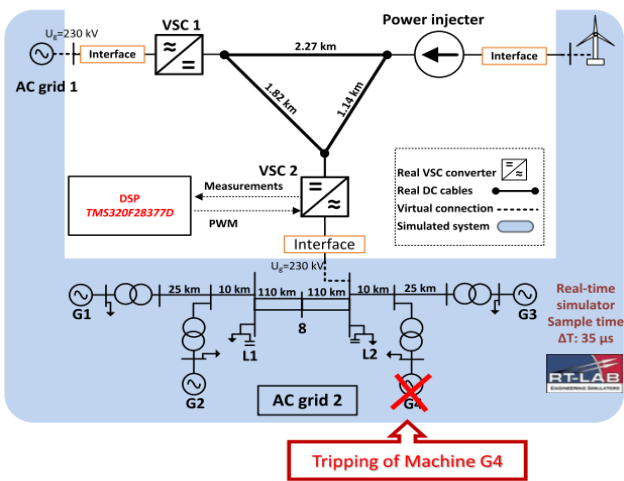


Figure 6: PHIL simulation test with G4 tripping.

VSC2 from providing more power. However, following the AC frequency recovery, the power of VSC2 also recovers and settles at the value defined by the selected frequency droop.

Converter	VSC 1	VSC 2	VSC 3
DC Power (W)	1000	1000	-2100
DC Voltage (V)	400		

Table 1: Operating point of DC grid.

	Area 1		Area 2	
Machines	G1	G2	G3	G4
Pn(MW)	900	900	900	900
P (MW)	615	615	615	315
Statism (pu/pu)	----	0,04	0,04	----
Loads (MW)	1463		986	

Table 2: Operating point of AC grid 2.

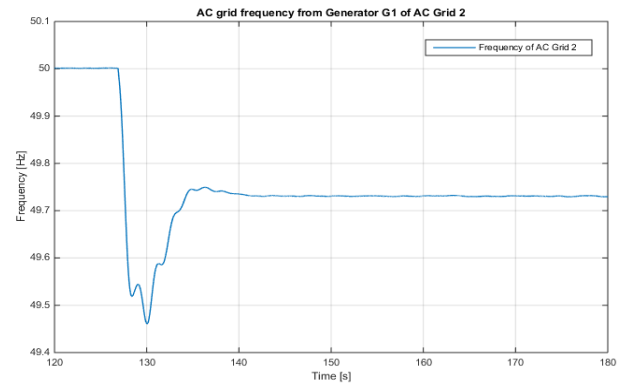


Figure 7: Frequency behaviour of AC grid 2.

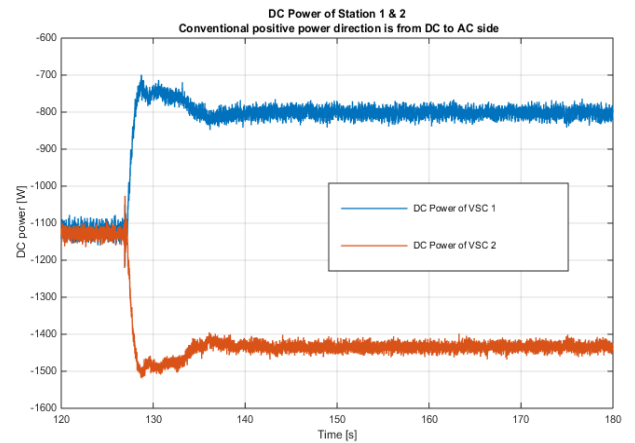


Figure 8: DC Power after losing G4 based on MPC.

## 5 Conclusion

This paper has presented a step-by-step implementation process of an advanced control strategy inspired of MPC for primary frequency support. A rigorous systematic validation method is performed starting from offline dynamic stability simulations, up to the experimental validation on a physical low-scale mock-up MTDC grid.

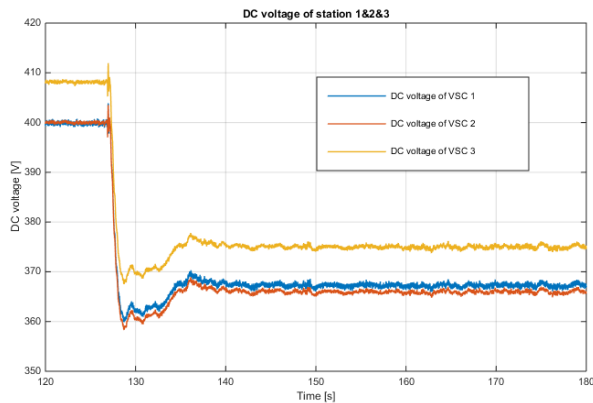


Figure 9: DC voltages after losing G4 based on MPC.

HIL and PHIL simulation methods are employed to reach this purpose. This study has served two purposes. First, it validates the results of the method presented in [12], and demonstrates the agreement between simulation and experimental results. Second, it has demonstrated the feasibility of implementing such advanced control strategies (like MPC), that require the solution of optimization problems. This has been achieved, by using conventional hardware development boards, like the DSP of the VSC, and proves that the use of powerful calculators is not necessary.

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