Stability of a Voltage Source Converter subject to Decrease of Short-Circuit Capacity: a Case Study

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***Abstract*—The subject of this paper is the investigation of the stability of a Voltage Source Converter (VSC) undergoing a sudden decrease of the Short Circuit Capacity of the AC system to which it is connected. A case study is reported on a simple system including an HVDC terminal and a Thévenin equivalent. First, a small-signal stability analysis is performed showing that the PLL-based vector control may become unstable at powers lower than the theoretical static stability limit. Dynamic simulations demonstrate that the stability limit may further decrease depending on the disturbance. The need for a fast instability detection method is highlighted.**

***Index Terms*—High Voltage Direct Current (HVDC), stability limit, Voltage Source Converter, weak AC grid.**

I. Introduction

During the recent years, power systems have been undergoing a gradual decommissioning of conventional power plants in favor of converter-interfaced renewable generation units. In combination with the opposition against installation of new AC lines, this is expected to lead to weaker AC systems, i.e. systems with lower Short-Circuit Capacity (SCC) values.

In addition, more High Voltage Direct Current (HVDC) connections are planned, to encourage bulk power transfer over long distances and the integration of distant renewable sources. The majority of these HVDC connections are based on Line Commutated Converters (LCC). LCC-based connections require to be connected to a strong system with a large enough SCC. However, connections based on Voltage Source Converters (VSC) have been gaining momentum, due to better flexibility and control capabilities. VSC-based connections do not necessarily have such an SCC requirement as discussed in [1]. However, as noted in various publications (e.g. [2] and [3]) the so-called vector control scheme of the VSC may become unstable when connected to a weak or a very weak AC grid.

The stability of a VSC connected to a weak AC grid has been the subject of several works in the literature. For instance, the work in [3] focuses on the destabilizing effect of the Phase Locked Loop (PLL) of the VSC. It is shown that the maximum theoretical limit of power transfer can be approached only with considerable slowing down of the PLL response.

The same problems with PLL-based vector control were identified in [2]. In this work, the authors propose the Power Synchronization Method (PSM) to control the VSC. By emulating the way the synchronous machines are synchronized with the network, it was shown that stable operation of the VSC even in very weak grid conditions can be achieved. Nevertheless, a backup PLL is still required to avoid loss of synchronism and limit the VSC overcurrent during AC faults. The PSM was also used in [4] with additional terms to provide damping and self synchronization.

An adaptive vector control is proposed in [1] to ensure stable VSC behavior in weak AC grid conditions. Instead of the PLL, the authors focused on the outer loops of the VSC, which control the VSC power and AC voltage to their respective reference values. By introducing cross-coupling terms between these controllers, with gains adapting depending on the operating condition of the VSC, stable operation even in very weak conditions was achieved.

A robust vector control is described in [5]. An AC voltage controller is synthesized including the PLL and AC voltage dynamics enabling power transfer for weak AC grid.

The maximum stable power transfer was increased in [6] by virtually connecting the VSC to a stronger point of the AC grid. This was achieved by introducing a term in the PLL compensating a part of the network impedance.

Nevertheless, in the aforementioned works, the investigation is limited to a VSC initially operating on a weak AC grid. The system response to a sudden large drop of the SCC, i.e. when an initially strong grid becomes suddenly weak, has not yet been investigated. This is the subject of this paper.

To this purpose, a case study is presented on a simplified system. A small-signal analysis is used to identify the impact of the various control parameters on stability. Then, dynamic simulations in phasor mode are performed to assess the system stability following a large decrease of SCC, taking into account the compliance of the VSC with grid code requirements.

The rest of the paper is organized as follows. Section II describes the VSC modeling. Results of the small-signal analysis are presented in Section III. Section IV investigates the VSC response to large disturbances using time-domain simulations. Concluding remarks are offered in Section V.

II. Test system

A. Overall system structure

The system that will be investigated is shown in Fig. 1. It consists of a point-to-point HVDC link and a simplified representation of the AC system by a Thévenin equivalent

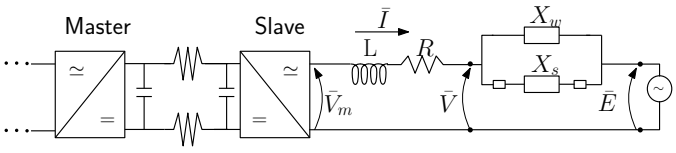


Figure 1. Test system of case study

involving an ideal voltage source (with magnitude E) and a small reactance X_s, in parallel with a larger reactance X_w.

The Slave VSC is connected to the AC system through its phase reactor with inductance L and resistance R. The VSC controls the current $\bar{I}$ flowing through the phase reactor by adjusting the voltage $\bar{V}_m$. In turn, the current is adjusted so that the VSC controls its active power P, as well as the AC voltage V at the connection point of the HVDC link. The Master VSC is controlling the DC voltage at its DC bus by adjusting its power, thereby ensuring the power balance of the HVDC link. In this paper, the focus is on the AC side of the Slave VSC, thus, the DC dynamics do not play a significant role. This simplification should be revisited in case the study would involve a disturbance in the AC grid of the Master VSC. This is not further discussed in this paper.

The static limit of the active power that can be absorbed by the AC system, is given by the well-known formula (e.g. [7]):

$$P_{max}^{st} = \frac{V\ E}{X_{eq}} \tag{1}$$

corresponding to a $90°$ phase angle difference and an equivalent reactance X_{eq} between the voltage-controlled nodes.

Clearly, if some lines are tripped in the AC system, the equivalent impedance X_{eq} seen by the VSC increases and the maximum power is reduced. If the active power P that the VSC seeks to inject is larger than the new reduced limit P_{max}^{st}, operation is impossible and instability will result.

B. VSC model

This section describes the generic model of the VSC and its controllers. The model is of the Type 6 in [8]. It has been set up based on various references (in particular [9], [10]).

1) PLL: All equations of the VSC are expressed in the dq frame. This is provided by the PLL, which is used to synchronize the VSC to the grid and provide the dq frame required for the controllers.

The PLL aims to align the d axis with the terminal voltage phasor $\bar{V}$ as shown in Fig. 2. The x and y axes are the orthogonal, rotating axes used to project all phasors. The xy frame is rotating with speed ω_{ref}, whereas the dq frame of the PLL with speed ω. In steady state, the voltage $\bar{V}$ is aligned with the d axis, and, thus, the components v_d and v_q of the terminal voltage are equal to V and zero, respectively. In addition, the angle θ is equal to δ, the component i_d of the current flowing through the phase reactor is the active current, and the component i_q is the reactive current with opposite sign. Following a transient, the PLL adjusts the speed ω accordingly, until the d axis again coincides with the voltage phasor.

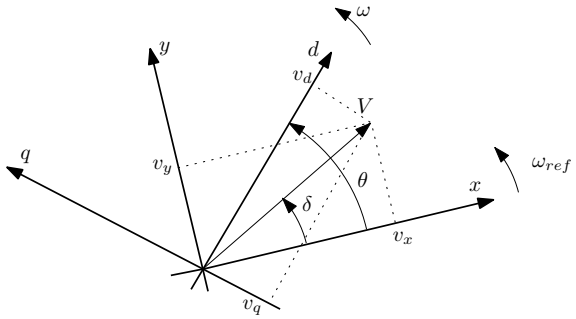


Figure 2. xy and dq reference frames

A typical scheme relying on a PI controller is used to achieve this synchronization. The controller drives to zero the v_q component of the terminal voltage V. The equations of the PI controller are as follows:

$$\omega = K_{p\omega} v_q + M_\omega \tag{2}$$

$$\frac{dM_\omega}{dt} = K_{i\omega} v_q \tag{3}$$

where $K_{p\omega}$, $K_{i\omega}$ are the PI gains, and M_ω the integrator internal state. The angle θ of the PLL evolves according to:

$$\frac{d\theta}{dt} = \omega - \omega_{ref}. \tag{4}$$

2) Phase reactor: The phase reactor equations expressed in the *dq* frame are as follows:

$$\frac{di_d}{dt} = \frac{\omega_N}{L}\left(-Ri_d + \frac{\omega L}{\omega_N} i_q + v_{md} - v_d\right) \tag{5}$$

$$\frac{di_q}{dt} = \frac{\omega_N}{L}\left(-Ri_q - \frac{\omega L}{\omega_N} i_q + v_{mq} - v_q\right) \tag{6}$$

where v_{md} and v_{mq} are the d and q components of voltage $\bar{V}_m$, respectively, ω_N and ω are the nominal angular frequency and the angular frequency measured by the PLL. All parameters and variables are in per unit, except ω_N and ω, which are in rad/s.

3) Current controllers: Each of the i_d and i_q currents is controlled to its reference i_d^{ref} and i_q^{ref}, respectively, by a dedicated PI controller adjusting the voltage components v_{md} and v_{mq} of $\bar{V}_m$. Feedforward and decoupling terms are added to ensure independent control of the currents [10]. This yields the following set of equations:

$$v_{md} = v_d - \frac{\omega L}{\omega_N}\, i_q + K_p\left(i_d^{ref} - i_d\right) + M_d \tag{7}$$

$$\frac{dM_d}{dt} = K_i\left(i_d^{ref} - i_d\right) \tag{8}$$

$$v_{mq} = v_q + \frac{\omega L}{\omega_N}\, i_d + K_p\left(i_q^{ref} - i_q\right) + M_q \tag{9}$$

$$\frac{dM_q}{dt} = K_i\left(i_q^{ref} - i_q\right) \tag{10}$$

where K_p, K_i are the proportional and integral gains of the PI controllers, and M_d, M_q the internal states of the integrators.

4) Outer controllers: The current references are provided by the outer loops, which aim to control the active power output P and the terminal voltage V of the VSC to their reference values P^{ref} and V^{ref}, respectively. Integral controllers are used to this purpose corresponding to:

$$\frac{di_d^{ref}}{dt} = K_{pi}\left(P^{ref} - P\right) = K_{pi}\left(P^{ref} - v_d i_d - v_q i_q\right) \quad (11)$$

$$\frac{di_q^{ref}}{dt} = K_{vi}\left(V - V^{ref}\right) = K_{vi}\left(\sqrt{v_d^2 + v_q^2} - V^{ref}\right) \quad (12)$$

where K_{pi}, K_{vi} are the gains of the controllers. A proportional term can be also added, but it was neglected for simplicity.

The complete structure of the VSC model and its controls is shown in Fig. 3. v_x and v_y are the rectangular components of the voltage phasor $\bar{V}$, and i_x and i_y those of the current $\bar{I}$ injected into the grid, all in the xy reference frame. The block $\boldsymbol{R}_{dq\to xy}$ denotes the change of reference frame from dq to xy and $\boldsymbol{R}_{xy\to dq}$ the inverse operation. The transformation of voltage coordinates from the xy to the dq frame is given by the following equations:

$$v_d = v_x\, cos\theta + v_y\, sin\theta \quad (13)$$

$$v_q = -v_x\, sin\theta + v_y\, cos\theta. \quad (14)$$

5) AC grid equations: The phasor approximation is used for the AC grid, as in standard AC system stability studies. Therefore, the equations giving the voltage at the terminal of the VSC in the xy frame are the following:

$$v_x = E - X_{eq} i_y \quad (15)$$

$$v_y = X_{eq} i_x. \quad (16)$$

III. Small-signal stability analysis of VSC connected to weak AC system

A. System reduction and linearization

The small-signal analysis is performed by linearizing the system of differential-algebraic equations (5)-(16).

After algebraic manipulations and variable eliminations, the following differential state vector $\boldsymbol{x}_d$ and algebraic state vector $\boldsymbol{x}_a$ can be chosen:

$$\boldsymbol{x}_d = \left[i_d\ i_q\ M_d\ M_q\ \theta\ M_\omega\ i_d^{ref}\ i_q^{ref}\right]^T \quad (17)$$

$$\boldsymbol{x}_a = \left[i_x\ i_y\ v_x\ v_y\right]^T \quad (18)$$

which satisfy the equations:

$$\dot{\boldsymbol{x}_d} = \boldsymbol{f}(\boldsymbol{x}_d, \boldsymbol{x}_a) \quad (19)$$

$$\boldsymbol{0} = \boldsymbol{g}(\boldsymbol{x}_d, \boldsymbol{x}_a). \quad (20)$$

By linearizing the above nonlinear equations, the system is brought in the form of

$$\begin{bmatrix}\Delta\dot{\boldsymbol{x}}_d \\ 0\end{bmatrix} = \left[\begin{array}{c|c}\boldsymbol{A} & \boldsymbol{B} \\ \hline \boldsymbol{C} & \boldsymbol{D}\end{array}\right]\begin{bmatrix}\Delta\boldsymbol{x}_d \\ \Delta\boldsymbol{x}_a\end{bmatrix} \quad (21)$$

where

$$\boldsymbol{A} = \frac{\partial \boldsymbol{f}}{\partial \boldsymbol{x}_d}, \quad \boldsymbol{B} = \frac{\partial \boldsymbol{f}}{\partial \boldsymbol{x}_a}, \quad \boldsymbol{C} = \frac{\partial \boldsymbol{g}}{\partial \boldsymbol{x}_d}, \quad \boldsymbol{D} = \frac{\partial \boldsymbol{g}}{\partial \boldsymbol{x}_a}. \quad (22)$$

The small-signal stability analysis is performed with the eigenvalues of the reduced Jacobian, which is the Schur complement of block $\boldsymbol{D}$:

$$\boldsymbol{J} = \boldsymbol{A} - \boldsymbol{B}\boldsymbol{D}^{-1}\boldsymbol{C}. \quad (23)$$

B. Parameters and operating point

The nominal active power of the VSC is selected as the base power. The nominal frequency of the system is 100π rad/s. The small-signal analysis is performed in the weak grid configuration by choosing $X_{eq} = X_w = 2$ pu. For simplicity, we take $E = 1$ pu, and we assume that the VSC also keeps its terminal voltage equal to 1 pu. Hence, the static stability limit is $P_{max}^{st} = 0.5$ pu. Since the network resistance has been neglected, the same limit applies for reverse power flow. In this work, the VSC active power is considered positive for inverter operation.

The inner loop controller gains have been tuned to have a response time of 10 ms. In order to have a good time decoupling between the inner and the outer loops, the response time of the latter is chosen ten times slower [10]. The PLL has been tuned to have a response time of 50 ms. The complete set of parameters for these settings is given in Fig. 3.

C. Effect of operating point

A total of eight eigenvalues are involved. For instance, for $P^{ref} = 0.4$ pu the eigenvalues are the following:

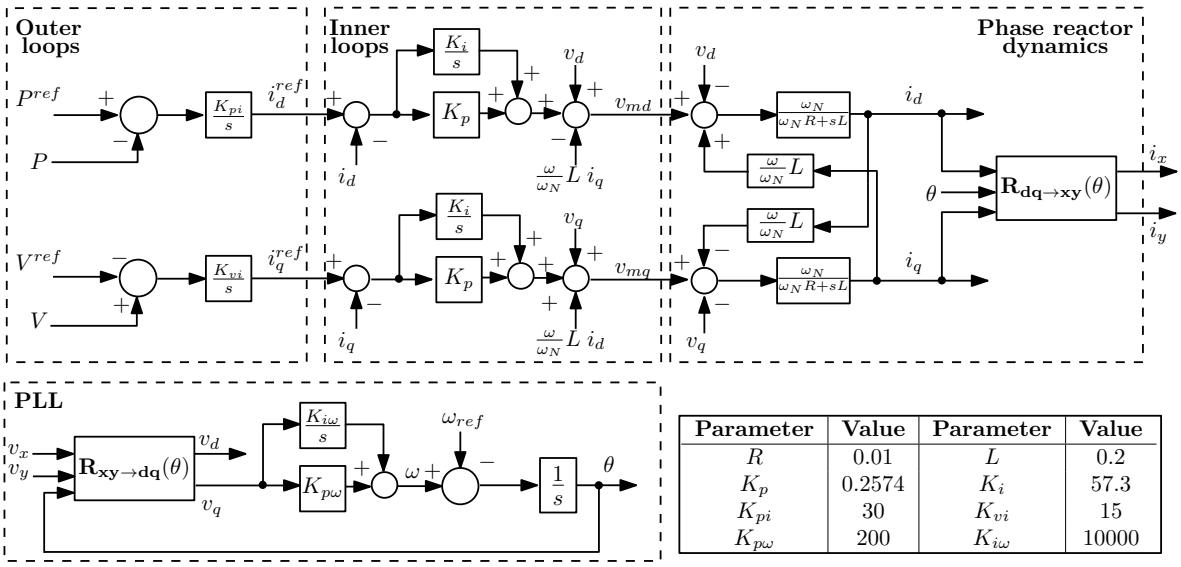
$$s_{1,2} = -196.2 \pm j242.7, \quad s_{3,4} = -203.3 \pm j215.2$$
$$s_{5,6} = -68.2 \pm j18.4, \quad s_{7,8} = -12.4 \pm j29.6$$

Due to the non-linearities in (11), (12), (13), (14), the Jacobian $\boldsymbol{J}$ and its eigenvalues change with the operating point. The effect of changing progressively P^{ref} on the dominant eigenvalues (i.e. $s_{7,8}$) is shown in Fig. 4. The eigenvalues are located in the left hand plane indicating a stable system for low P^{ref}. However, as the power increases the eigenvalue moves to the right. The system becomes unstable for P^{ref} greater than 0.44 pu.

Note that this limit is smaller than P_{max}^{st}. In fact, the system undergoes a Hopf bifurcation (growing oscillations) for $P^{ref} = 0.45$ pu. For $P^{ref} = 0.5$ pu, it loses its equilibrium, i.e. it undergoes a saddle-node bifurcation, easily identified by the zero eigenvalue.

D. Effect of outer loops tuning

The effect of adjusting the active power and voltage control loops is now discussed. Unless otherwise specified, the response time of the inner loops is 10 ms, of the PLL 50 ms, and of the outer loops 100 ms. The analysis is performed at the first unstable operating point identified in the previous subsection, i.e. for $P^{ref} = 0.45$ pu.



Parameter	Value	Parameter	Value
R	0.01	L	0.2
K_p	0.2574	K_i	57.3
K_{pi}	30	K_{vi}	15
$K_{p\omega}$	200	$K_{i\omega}$	10000

Figure 3. Model of VSC and its controllers

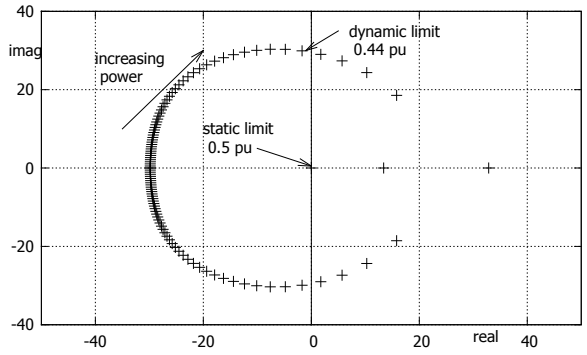


Figure 4. Dominant eigenvalues when varying the power setpoint P^{ref}

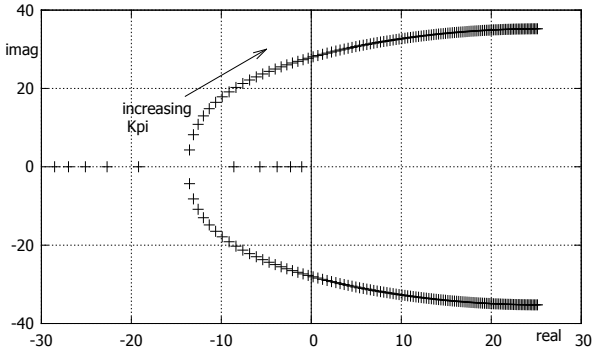


Figure 5. Dominant eigenvalues when varying K_{pi} ($P^{ref} = 0.45$ pu)

1) Effect of active power loop: The locus of the dominant eigenvalues when varying the active power loop gain K_{pi} is depicted in Fig. 5. It can be seen that accelerating the active power control deteriorates stability by moving the eigenvalues towards the right-hand plane.

2) Effect of voltage loop: In contrast, when the gain K_{vi} is increased, the stability of the system is improved as demonstrated by the locus of the dominant eigenvalues shown in Fig. 6. For low values of K_{vi} the system is unstable.

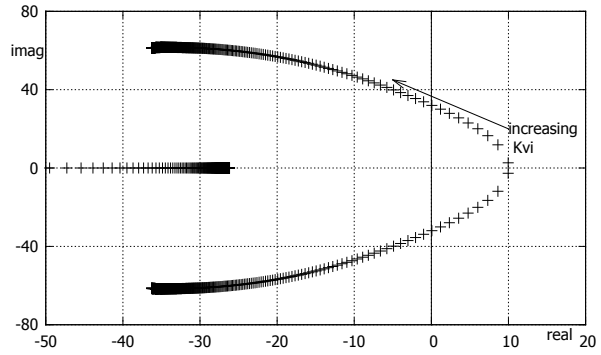


Figure 6. Dominant eigenvalues when varying K_{vi} ($P^{ref} = 0.45$ pu)

The results of Figs. 5 and 6 suggest that voltage control should be faster than active power control to increase the range of stable operating points, i.e. to make the dynamic limit approach the static one (but, of course, never exceed it).

E. Effect of PLL tuning

The effect of adjusting the PLL parameters is shown in Fig. 7. The gains $K_{p\omega}$ and $K_{i\omega}$ are tuned based on [11] in order to satisfy a desired response time τ_ω as follows:

$$K_{p\omega} = \frac{10}{\tau_\omega} \quad \text{and} \quad K_{i\omega} = \frac{25}{\tau_\omega^2} \tag{24}$$

The locus of the dominant eigenvalues when varying τ_ω from 5 ms up to 500 ms is shown in Fig. 7. It is shown that the system is stable for very slow and very fast PLL response times, whereas it becomes unstable for intermediate values.

IV. Large-disturbance analysis

In this section, the response of the system following the sudden tripping of the short reactance is investigated. Before

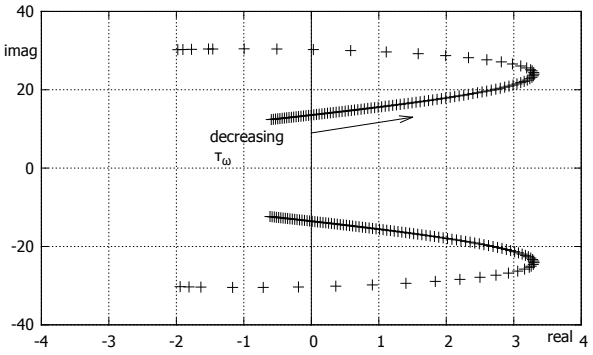


Figure 7. Dominant eigenvalues when varying τ_ω ($P^{ref} = 0.45$ pu)

the disturbance (i.e. short reactance still in operation), the AC system is adequately strong to absorb the full power of the VSC. Therefore, the power transferred through the VSC before the disturbance can be even above the SCC of the post-disturbance weak grid. If the power transfer is above the stability limit indicated by the analysis in Section III, instability is certain unless emergency actions are taken. Nevertheless, it will be shown that stability even for lower powers is not guaranteed, but depends on the disturbance conditions.

The system is subject to a large disturbance requiring to consider its non-linear behavior. Therefore, upper and lower limits on i_d^{ref}, i_q^{ref}, v_{md}, v_{mq} and ω have been included in the following analysis (not shown in Fig. 3). Furthermore, the analysis should also consider changes of control logic. Namely, since the tripping of a line is usually preceded by a fault, it is important to include the low voltage behavior of the VSC, detailed in the next sub-section.

A. Low voltage behavior of VSC

In order to avoid sudden disconnection of multiple converters, many grid codes require Fault-Ride-Through (FRT) capability by the VSCs [12], [13]. In addition, during the duration of the fault, the VSC is required to boost its reactive current injection in order to support the voltage, while limiting the active current is needed to avoid exceeding the nominal current. Then, after fault clearing, the VSC should ramp up its active power back to its pre-disturbance value. For example, the German grid code specifies that the active power should be restored with a gradient of at least 20% of its nominal value per second [14]. Other grid codes, e.g. in UK [15], are even more constraining by demanding faster active power recovery.

This behavior is modeled as shown in Fig. 8 relative to the outer loops of the VSC.

In normal operation both the active power and the voltage loops correspond to (11) and (12), respectively, and priority is given to the active current, which can increase up to the maximum VSC active current αI^{max}, α being the fraction of the maximum current I^{max} allocated to active current. Namely, the upper limits shown in Fig. 8 are given by:

$$I_d^{max} = \alpha I^{max} \quad \text{and} \quad I_q^{max} = \sqrt{(I^{max})^2 - \left(i_d^{ref}\right)^2}. \quad (25)$$

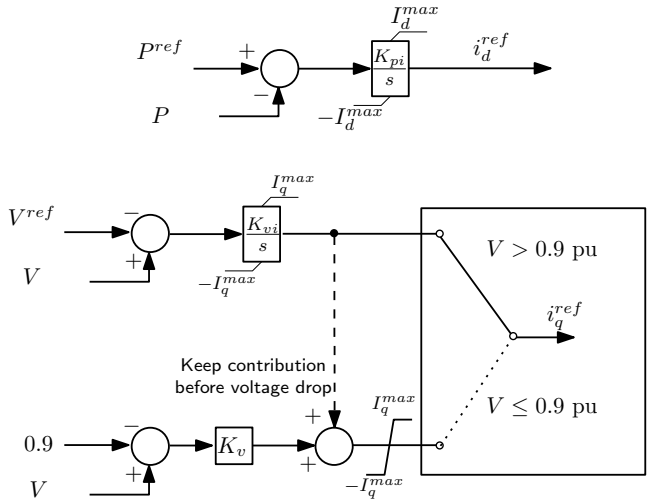


Figure 8. Outer loops of VSC including low voltage support

In case the voltage drops below 0.9 pu the priority goes to reactive current, i.e.

$$I_d^{max} = \alpha\sqrt{(I^{max})^2 - \left(i_q^{ref}\right)^2} \quad \text{and} \quad I_q^{max} = I^{max} \quad (26)$$

and the voltage control loop is replaced by a proportional controller with gain K_v. It is noted that the i_q contribution of the voltage control before the fault is kept and added as a constant term to the contribution of that proportional controller. In addition, the voltage control integrator is frozen to prevent windup during the fault.

After fault clearing and the subsequent recovery of the voltage above 0.9 pu, the integral voltage control is restored in operation and priority is once again given, albeit gradually, to the active current. This is achieved by ramping up the active current limit I_d^{max}.

B. Simulation results

1) Case 1 - Tripping of short reactance with fault: The disturbance considered is a solid three-phase fault in the middle of the short reactance ($X_s = 0.1$ pu), cleared after five cycles (0.1 s) by disconnecting the reactance X_s. K_v is set equal to 2.5 pu and the active power recovery rate is $20\ \%/s$. The response times of the inner loops, the PLL and the outer loops are 10, 50 and 100 ms, respectively. I^{max} has been set equal to 1 pu and $\alpha = 1$. All dynamic simulations were performed with RAMSES, a time simulation software developed at the Univ. of Liège [16], using the techniques described in [17].

Figures 9, 10 and 11 show the evolution of respectively the VSC terminal bus voltage V, the active P and the reactive power Q. Three initial operating points are considered: (i) $P^{ref} = 0.44$ pu (marginally small-signal stable point), $P^{ref} = 0.45$ pu (marginally small-signal unstable point) and $P^{ref} = 0.8$ pu (unstable point).

Following the fault, the VSC voltage drops below the threshold of 0.9 pu, as shown in Fig. 9, and the VSC enters

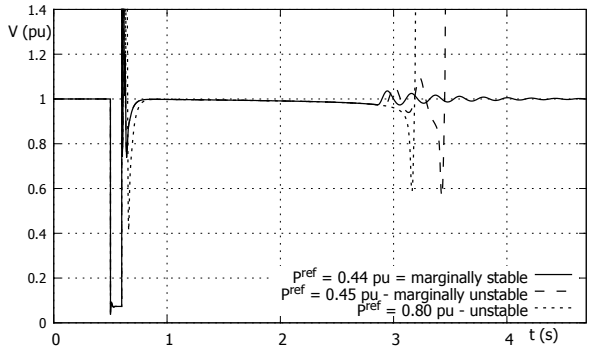


Figure 9. Case 1 - Voltage at VSC terminal

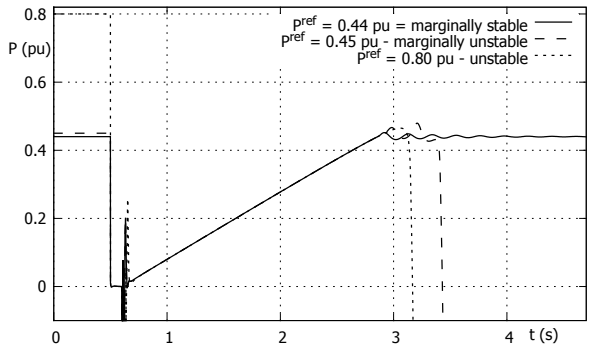


Figure 10. Case 1 - VSC active power

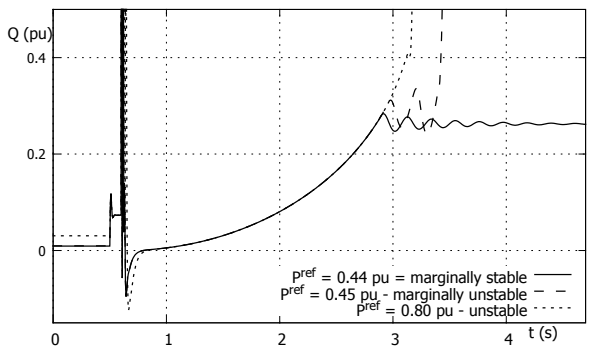


Figure 11. Case 1 - VSC reactive power

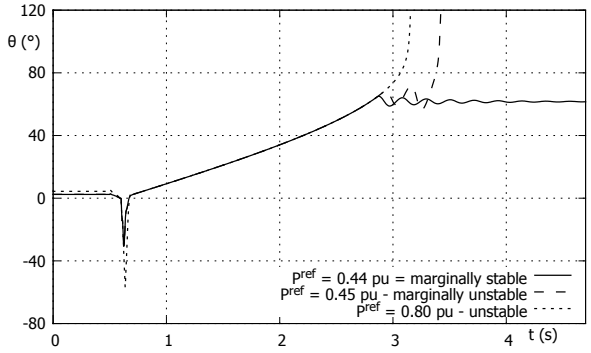


Figure 12. Case 1 - PLL angle

the reactive support mode by giving priority to the reactive current. Since, the full capability of the VSC is devoted to reactive power the active power drops to 0 pu during the fault.

After the clearing of the fault and the tripping of the reactance, there is a large fast transient caused by the voltage and phase angle variations. An overvoltage spike is observed immediately after fault clearing due to the large reactive current contribution during the fault. This is corrected by VSC controls, which swiftly restore the voltage near its nominal value. The spike is due to the reactive current, which reached a high value during the fault and takes a short time to decrease, combined with the large Thévenin reactance. One cannot preclude that an overvoltage protection trips the VSC. If not, the VSC enters the active power restoration mode and ramps up its active power. As expected, in the unstable case ($P^{ref} = 0.8$ pu), the reference power is infeasible and the attempt to recover it leads to collapse. As far as the $P^{ref} = 0.45$ case is concerned, the system becomes small-signal unstable, as also predicted from Fig. 4. For $P^{ref} = 0.44$ pu, the power experiences some oscillations, but eventually reaches a stable steady state.

The angle θ of the PLL is shown in Fig. 12, for all cases. For the stable case, the angle increases almost linearly, as the power is ramped up and settles at $61°$. On the contrary, it raises monotonically in the two unstable cases indicating that the VSC cannot be resynchronized with the AC grid.

It is interesting to note that the results of Fig. 10 are in agreement with the small-signal stability analysis of Fig. 4. This is mainly due to the active power reduction during the fault and the gradual power restoration after. Hence, the system is smoothly brought to its final equilibrium point, and the stability limit is not influenced by non-linearities.

2) Case 2 - Tripping of short reactance without fault: Whether the fault-ride-through behavior of the VSC is activated depends on the type of the disturbance, the system under concern, etc., and is not a priori known.

In this case, the SCC is decreased without a fault. The evolutions of the VSC voltage and active power are shown in Figs. 13 and 14, respectively, for various initial operating points. The short reactance is tripped at $t = 0.6$ s.

Figure 14 reveals that the case of $P^{ref} = 0.44$ pu, identified as marginally stable by both the small-signal analysis and Case 1, is no longer stable. In contrast, almost immediate collapse is observed after the disturbance. Indeed, after an initial increase caused by the sudden angle change and the time it takes for the VSC to track the new angle, the voltage drops below 0.9 pu, but not much. Thus, the magnitude of the reactive current i_q injected is smaller and leaves room for the whole active current i_d. The latter is not reduced and the VSC attempts to force the pre-disturbance active power immediately.

In order to identify a secure operating point, the pre-disturbance power P^{ref} was decreased in steps of 0.01 pu. The first stable operating point was found for $P^{ref} = 0.37$ pu. However, as seen in Fig. 13, the voltage has dropped and settled below the threshold of 0.9 pu, indicating that the VSC has been locked in the reactive support mode. Nevertheless,

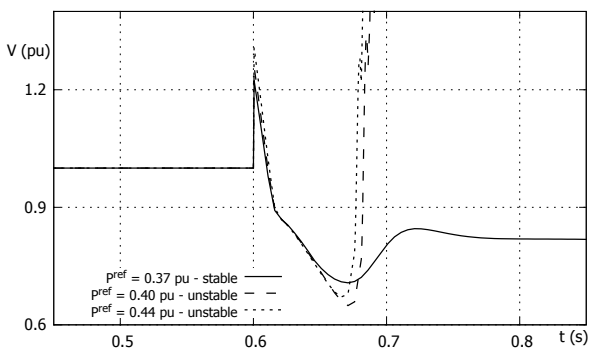


Figure 13. Case 2 - Voltage at VSC terminal

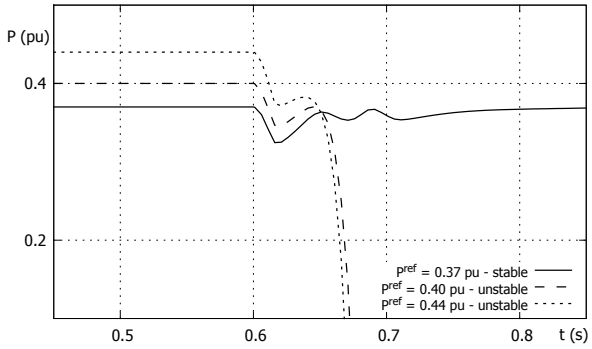


Figure 14. Case 2 - VSC power

since the active power is successfully restored, the operating point is considered stable.

V. Conclusion

This paper has investigated the stability of a VSC when connected to a suddenly weakened AC grid. First, a small-signal analysis was conducted revealing that the stability of the system is mainly affected by the tuning of the outer loop parameters and the response time of the PLL.

Then time-domain simulations were performed to further investigate the VSC response to large disturbances. It has been shown that depending on the sequence of events leading to the SCC decrease, the stability limit detected by small-signal analysis may be optimistic, and further reduction of the pre-disturbance VSC power would be required to ride through the disturbance. In addition, it has been shown that the system may undergo severe transients when subject to a sudden decrease of the SCC. Therefore, various controls of the VSC, in particular the switching to reactive support when a low voltage is detected followed by the gradual restoration of the active power, have to be taken into account when conducting stability studies.

In view of the large transients, the adequacy of the generic model used should be further investigated, as well as the appropriateness of the phasor approximation in the AC system. For instance, preliminary checks including the fast network transients have shown that eigenvalues with high frequency can become unstable, if the integral gain K_{vi} is increased so much that the outer voltage and the inner current control loops are no longer decoupled.

Envisaged future research concerns methods to detect the imminent instability, as well as countermeasures, such as fast power reduction or simply tripping of the HVDC link. Preventive power adjustment of the HVDC link is not desired because of the rarity of such events. Due to the speed with which the phenomena evolve, relying on a communication signal might not be desirable. This constitutes a challenge since the emergency control should depend entirely on local signals readily available to the VSC. Finally, the study will be expanded to VSC control structures relying on different than the PLL schemes for synchronization, such as the PSM.

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