IEEE PES General Meeting 2017
DSA Working Group panel
" Integration of distribution systems, data assimilation, and advanced modelling into on-line DSA "

Instability of Voltage Source Converters in weak AC grid conditions : a case study

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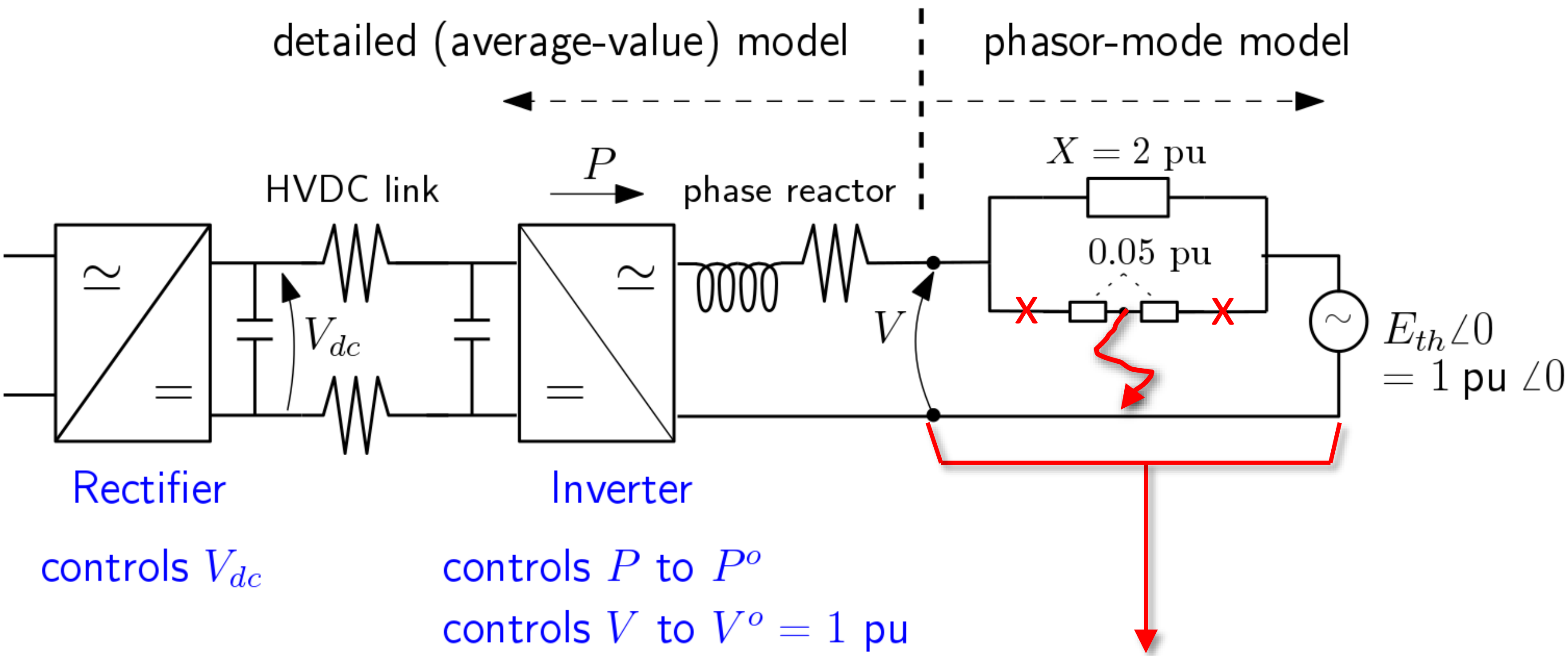
Introduction (1)

- Worldwide growth of number of HVDC links using Voltage Source Converters (VSC)
- VSCs can operate with weaker AC grids than Line Commutated Converters
  - i.e. with smaller values of $\dfrac{\text{AC system short−circuit capacity}}{\text{VSC nominal power}}$
- However, VSCs can be subject to small-signal instability when connected to a weak AC grid
  - J. Z. Zhou, H. Ding, S. Fan, Y. Zhang and A. M. Gole "Impact of short-circuit ratio and phase locked loop parameters on the small signal behavior of a VSC HVDC converter," IEEE Trans. Power Delivery, vol. 29, 2014
  - A. Canelhas, S. Karamitsos and M. Bazargan, "Review of static voltage stability screening methods for application in AC power grids with large-scale wind penetration and VSC HVDC interconnectors," Proc. 11th IET Int. Conf. on AC/DC Power Transm., 2015

Introduction (2)

- Improved controls of VSC have been proposed to extend the range of stable operation
  - J. A. Suul, S. D’Arco, P. Rodríguez and M. Molinas, “Impedance-compensated grid synchronisation for extending the stability range of weak grids with voltage source converters,” *IET Gener. Transm. & Distrib.*, vol. 10, pp. 1315–1326, 2016
  - A. Egea-Alvarez, S. Fekriasl, F. Hassan and O. Gomis-Bellmunt, “Advanced Vector Control for Voltage Source Converters Connected to Weak Grids,” *IEEE Trans. Power Systems*, vol. 30, pp. 3072–3081, 2015
  - L. Zhang, L. Harnefors and H. Nee, “Power-Synchronization Control of Grid-Connected Voltage-source Converters,” *IEEE Trans. Power Systems,* vol. 25, 2010
- This presentation: a case study of destabilization of a VSC after a severe drop of short-circuit capacity
  - relying on a simple system with generic VSC model
  - combining small-signal and large-disturbance analyses

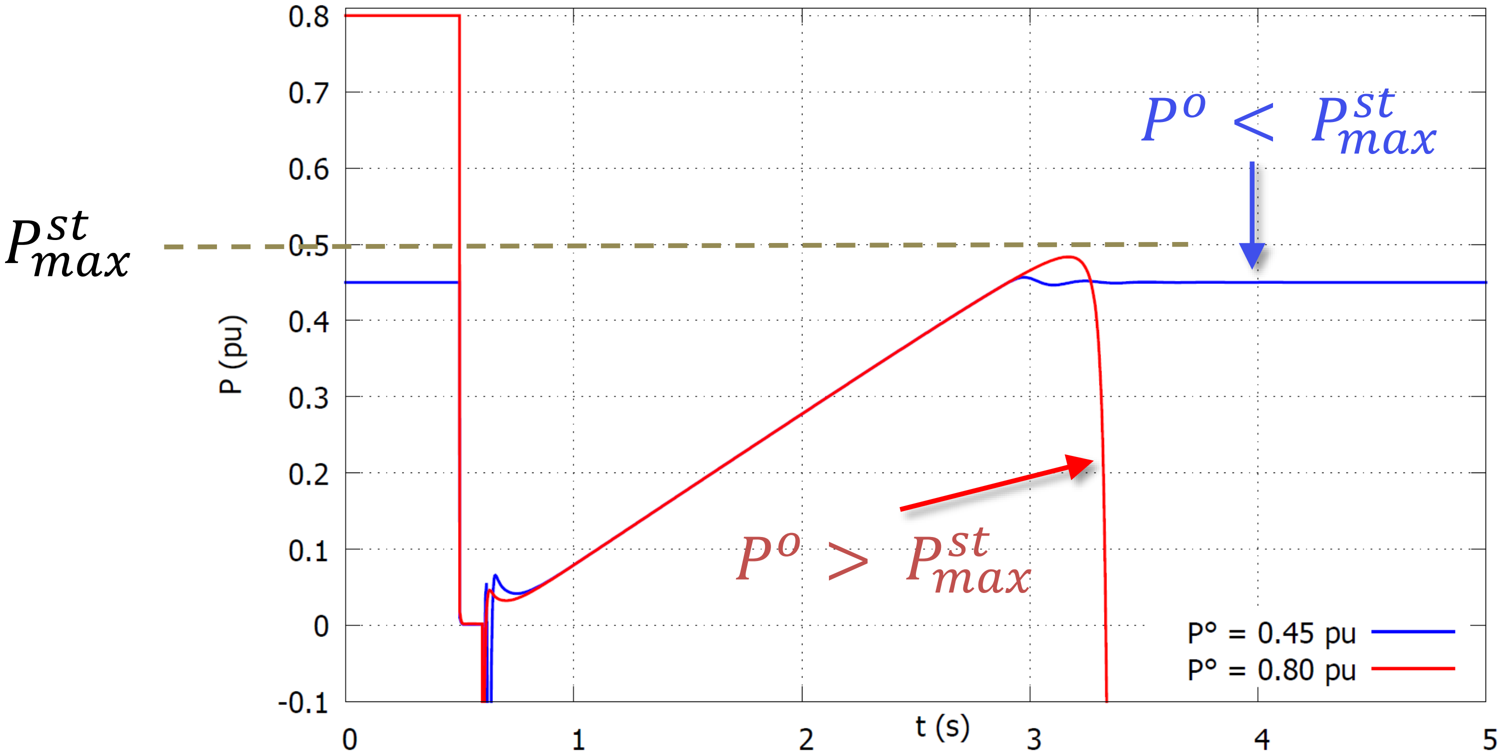
System and disturbance



after fault clearing by line opening :

$$P_{max}^{st} = \frac{V\,.\,E_{th}}{X} = \frac{1\,.\,1}{2} = 0.5 \text{ pu } (= S_{sc})$$

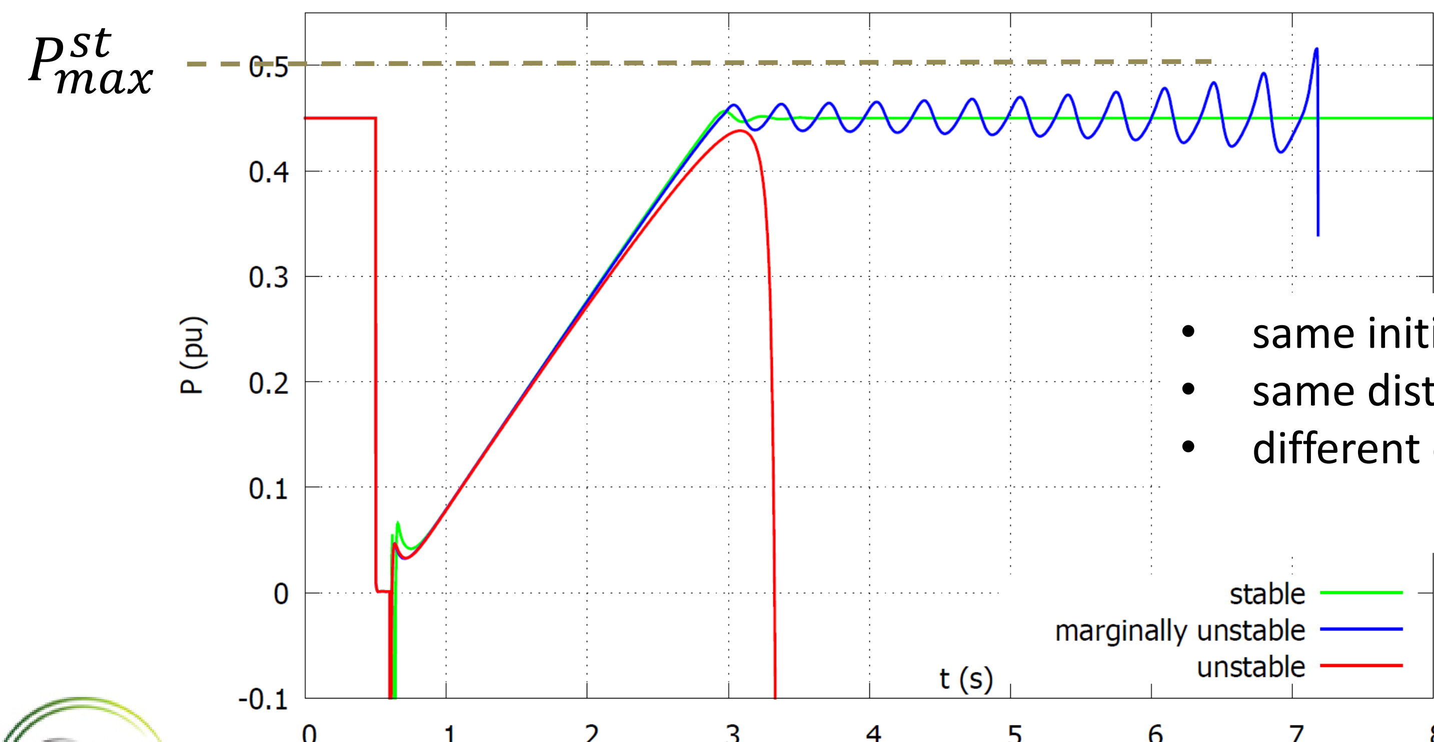
Response to fault and line tripping



- Instability driven by power electronics
- does not fall in one of the "classical" categories (angle, frequency, voltage) "ruled" by synchronous machines and loads

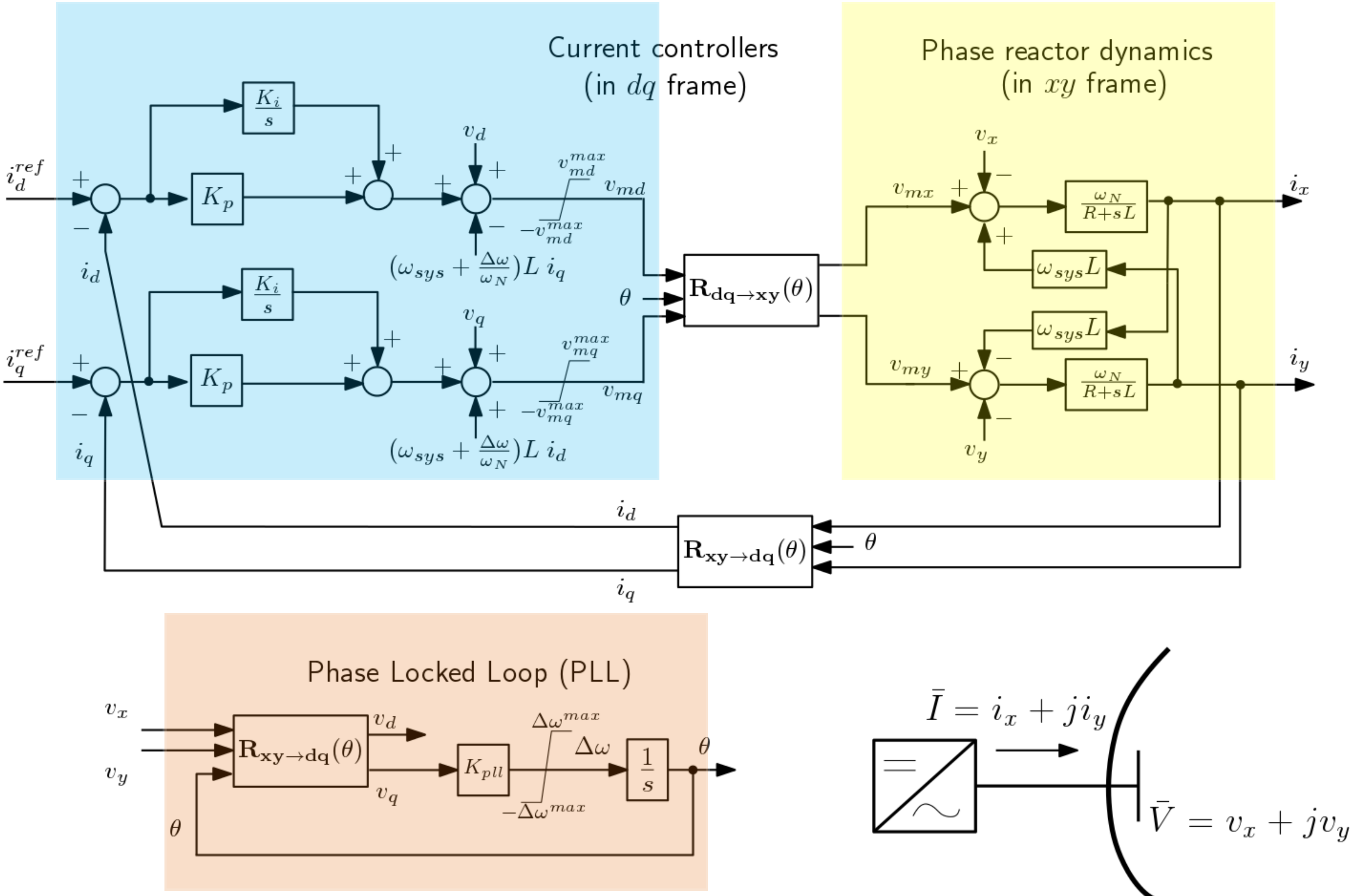
Response to fault and line tripping

- In terms of pre-fault power, P_{max}^{st} is the "static" stability limit
  - no post-disturbance equilibrium ; static power flow equations infeasible
- but the "dynamic" stability limit can be smaller :



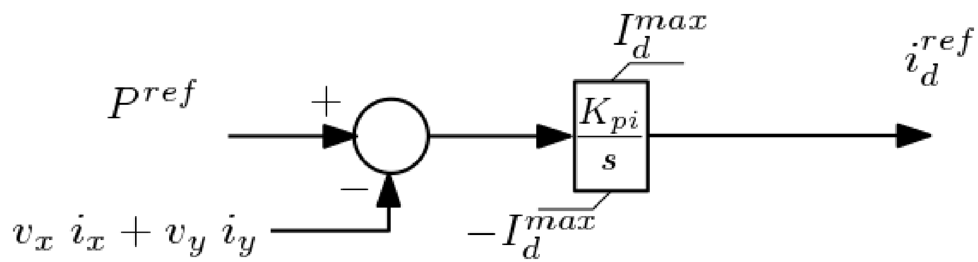
- same initial operating point
- same disturbance
- different controller settings

VSC model (1)

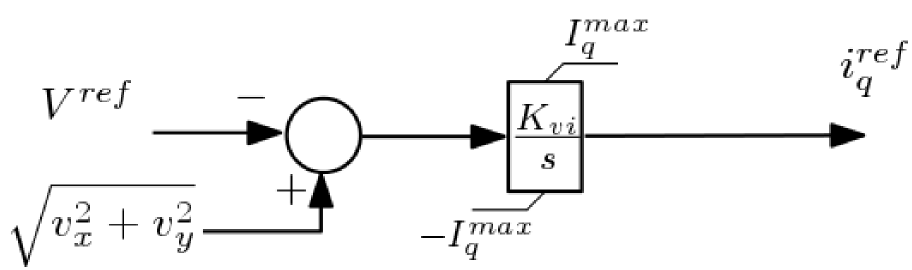

Current controllers
(in dq frame)
Phase reactor dynamics
(in xy frame)
i_d^{ref}
i_q^{ref}
$\frac{K_i}{s}$
K_p
v_d
v_q
v_{md}^{max}
$-v_{md}^{max}$
v_{mq}^{max}
$-v_{mq}^{max}$
v_{md}
v_{mq}
$(\omega_{sys} + \frac{\Delta\omega}{\omega_N})L\, i_q$
$(\omega_{sys} + \frac{\Delta\omega}{\omega_N})L\, i_d$
θ
$\mathbf{R_{dq\rightarrow xy}}(\theta)$
$\mathbf{R_{xy\rightarrow dq}}(\theta)$
i_d
i_q
v_x
v_y
v_{mx}
v_{my}
$\frac{\omega_N}{R+sL}$
$\omega_{sys}L$
i_x
i_y
Phase Locked Loop (PLL)
K_{pll}
$\Delta\omega^{max}$
$-\Delta\omega^{max}$
$\Delta\omega$
$\frac{1}{s}$
$\bar{I} = i_x + j i_y$
$\bar{V} = v_x + j v_y$

VSC model (2)

Active power control outer loop

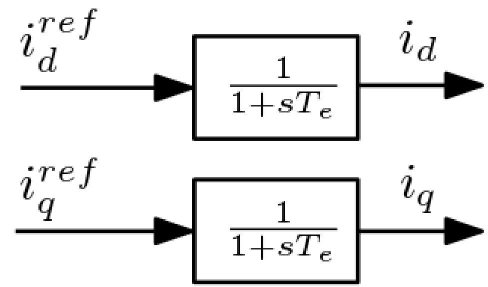


Terminal voltage control outer loop



Small-signal analysis : simplified model

$$
\begin{aligned}
\frac{d}{dt} i_d &= \frac{1}{T_e}(i_d^{ref} - i_d) \\
\frac{d}{dt} i_q &= \frac{1}{T_e}(i_q^{ref} - i_q) \\
\frac{d}{dt} \theta &= K_{pll}(-v_x \sin\theta + v_y \cos\theta) \\
\frac{d}{dt} i_d^{ref} &= K_{pi}(P^o - v_x i_x - v_y i_y) \\
\frac{d}{dt} i_q^{ref} &= -K_{vi}(V^o - \sqrt{v_x^2 + v_y^2}) \\
0 &= -i_x + i_d \cos\theta - i_q \sin\theta \\
0 &= -i_y + i_q \cos\theta + i_d \sin\theta \\
0 &= -v_x + E_{th} - X_{th} i_y \\
0 &= -v_y + X_{th} i_x
\end{aligned}
$$



PLL

active power control

terminal voltage control

dq $\rightarrow$ xy reference

network (Thévenin equiv.)

Small-signal analysis : simplified model linearized

$$
\begin{bmatrix} \Delta\dot{i}_d \\ \Delta\dot{i}_q \\ \Delta\dot{\theta} \\ \Delta\dot{i}_d^{ref} \\ \Delta\dot{i}_q^{ref} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}
=
\left[\begin{array}{ccccc|cccc}
\frac{-1}{T_e} & 0 & 0 & \frac{1}{T_e} & 0 & 0 & 0 & 0 & 0 \\
0 & \frac{-1}{T_e} & 0 & 0 & \frac{1}{T_e} & 0 & 0 & 0 & 0 \\
0 & 0 & A_{\theta\theta} & 0 & 0 & 0 & 0 & A_{\theta x} & A_{\theta y} \\
0 & 0 & 0 & 0 & 0 & -K_{pi}v_x^o & -K_{pi}v_y^o & -K_{pi}i_x^o & -K_{pi}i_y^o \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & K_{vi}\frac{v_x^o}{V^o} & K_{vi}\frac{v_y^o}{V^o} \\
\hline
\cos\theta^o & -sin\theta^o & A_{x\theta} & 0 & 0 & -1 & 0 & 0 & 0 \\
\sin\theta^o & \cos\theta^o & A_{y\theta} & 0 & 0 & 0 & -1 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & -X_{th} & -1 & 0 \\
0 & 0 & 0 & 0 & 0 & X_{th} & 0 & 0 & -1
\end{array}\right]
\begin{bmatrix} \Delta i_d \\ \Delta i_q \\ \Delta\theta \\ \Delta i_d^{ref} \\ \Delta i_q^{ref} \\ \Delta i_x \\ \Delta i_y \\ \Delta v_x \\ \Delta v_y \end{bmatrix}
$$

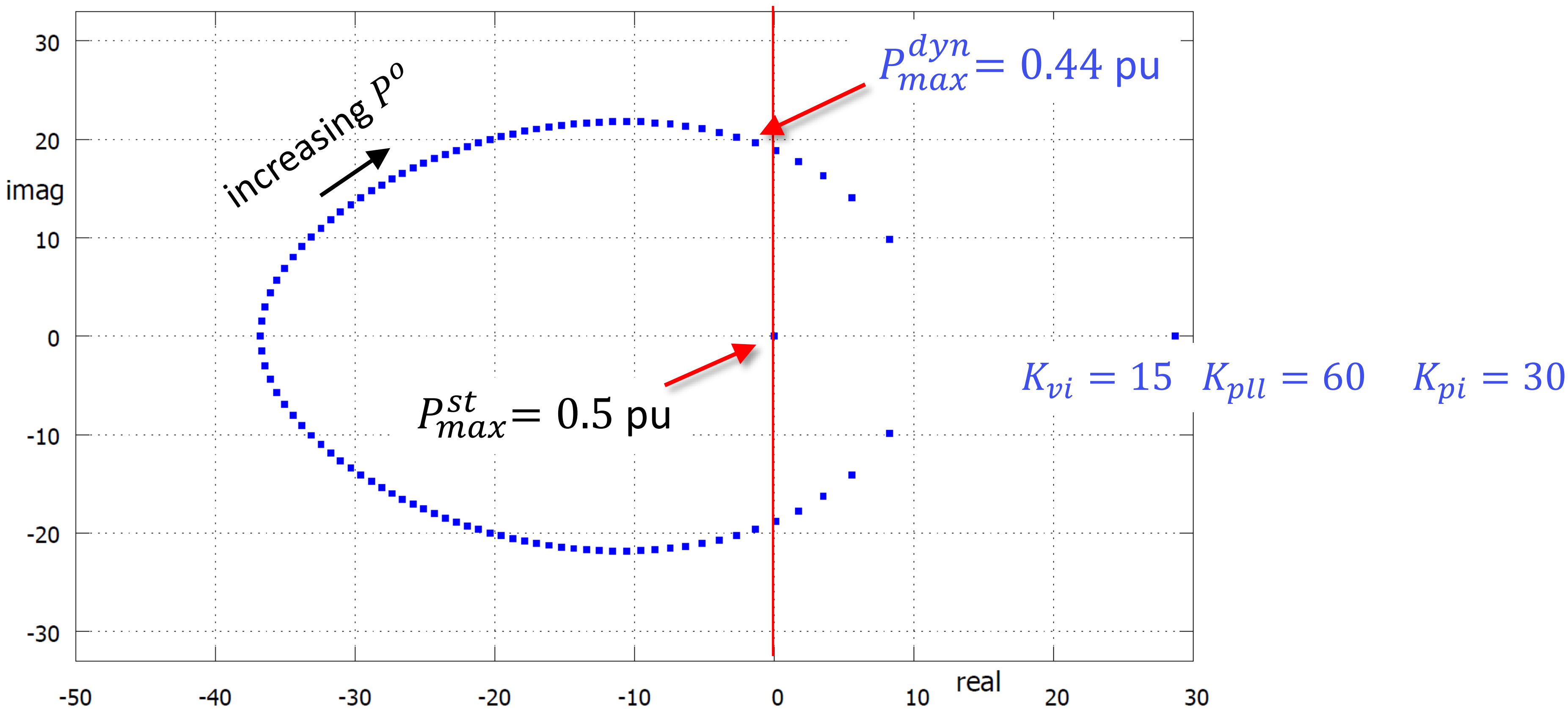
$$J_{dyn} = A - B\, D^{-1}\, C$$

$$A_{\theta\theta} = K_{pll}(-v_x^o \cos\theta^o - v_y^o \sin\theta^o) \qquad A_{\theta x} = -K_{pll}\sin\theta^o \qquad A_{\theta y} = K_{pll}\cos\theta^o$$

$$A_{x\theta} = -i_d^o \sin\theta^o - i_q^o \cos\theta^o \qquad A_{y\theta} = -i_q^o \sin\theta^o + i_d^o \cos\theta^o$$

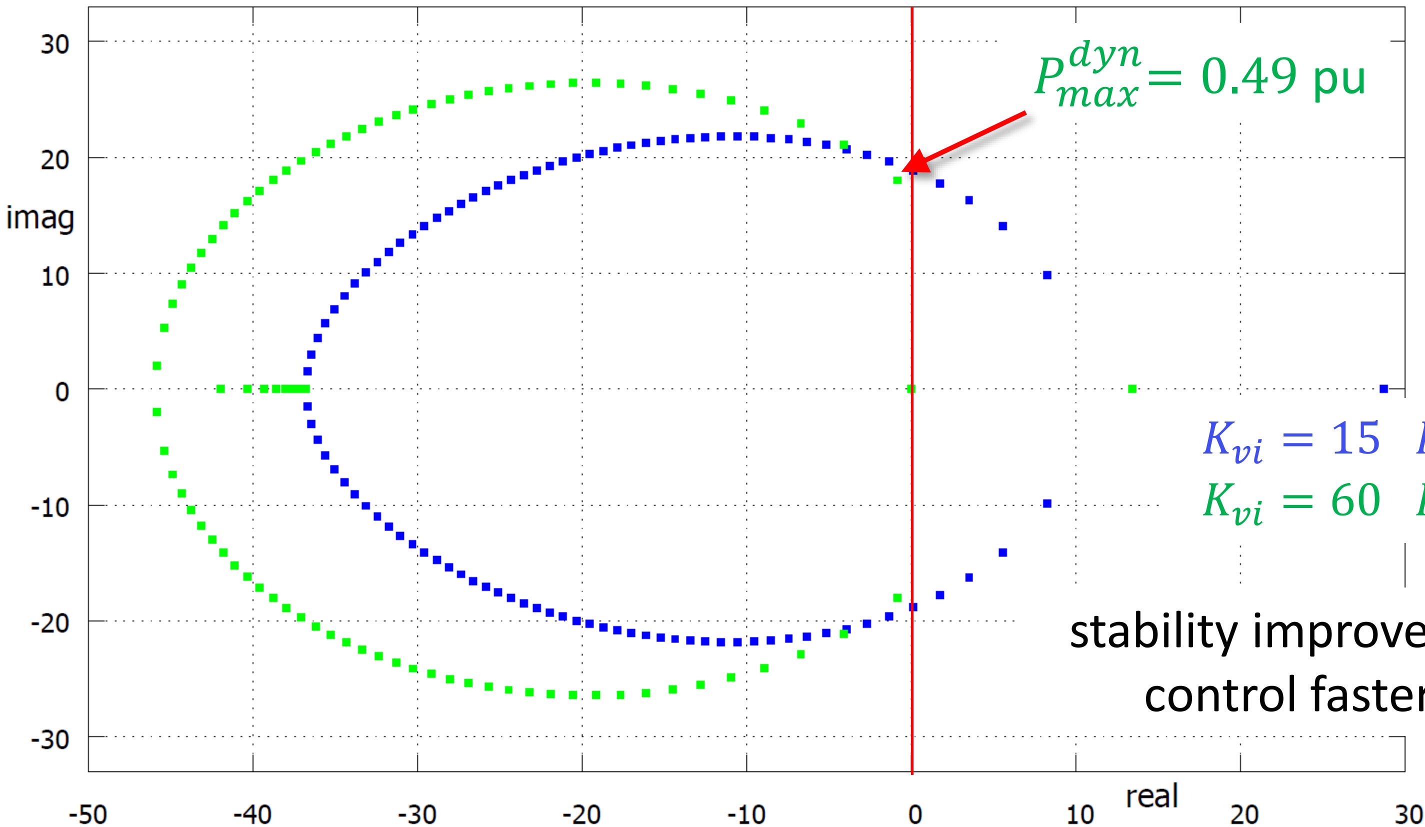
Small-signal analysis : results (1)

Locus of dominant eigenvalues when varying initial power P°; X_{th}= 2 pu



Small-signal analysis : results (2)

Locus of dominant eigenvalues when varying initial power P°; X_{th}= 2 pu



$P_{max}^{dyn} = 0.49$ pu

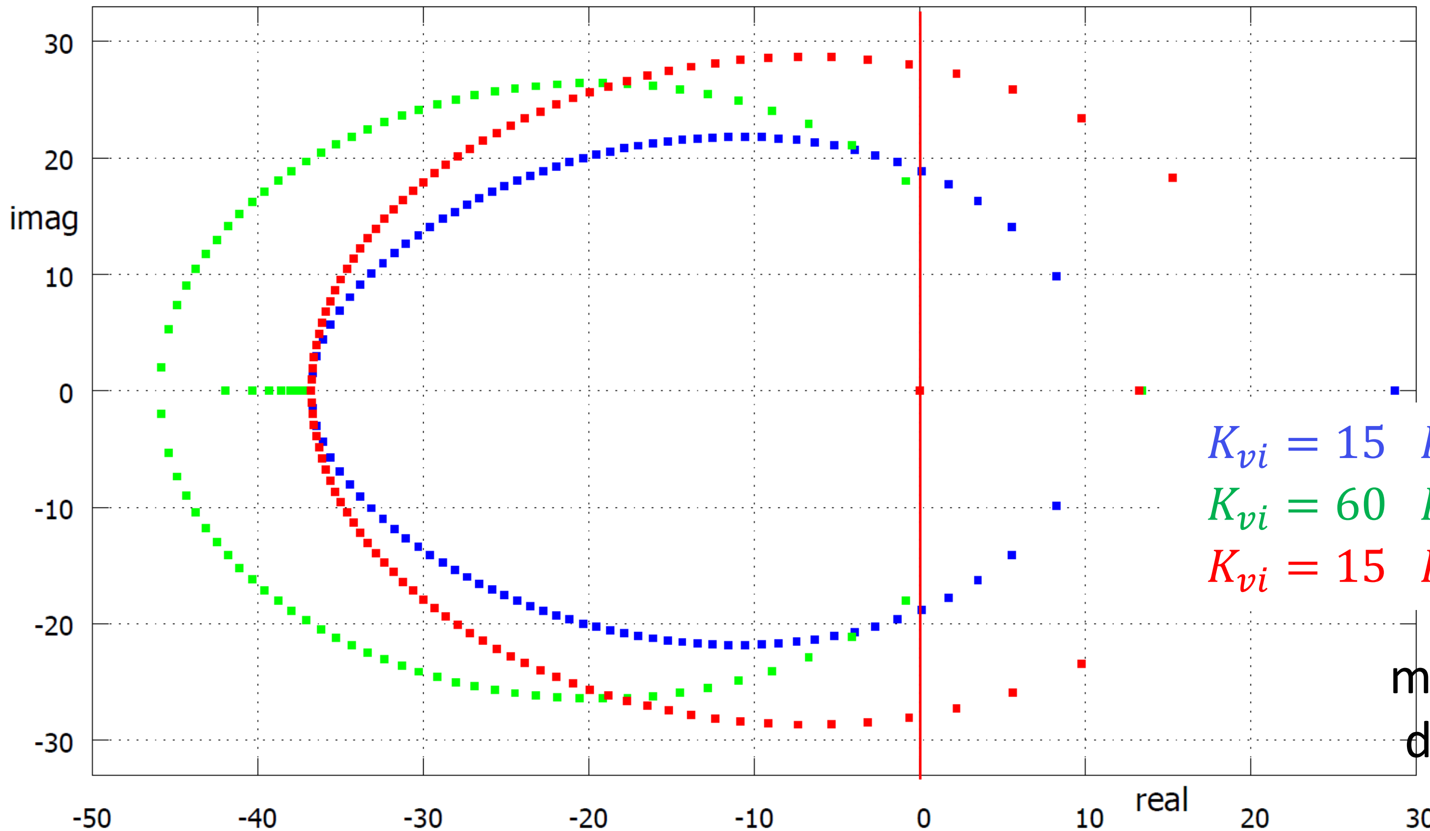
$K_{vi} = 15 \quad K_{pll} = 60 \quad K_{pi} = 30$

$K_{vi} = 60 \quad K_{pll} = 60 \quad K_{pi} = 30$

stability improved by making voltage control faster than power control

Small-signal analysis : results (3)

Locus of dominant eigenvalues when varying initial power P°; X_{th}= 2 pu



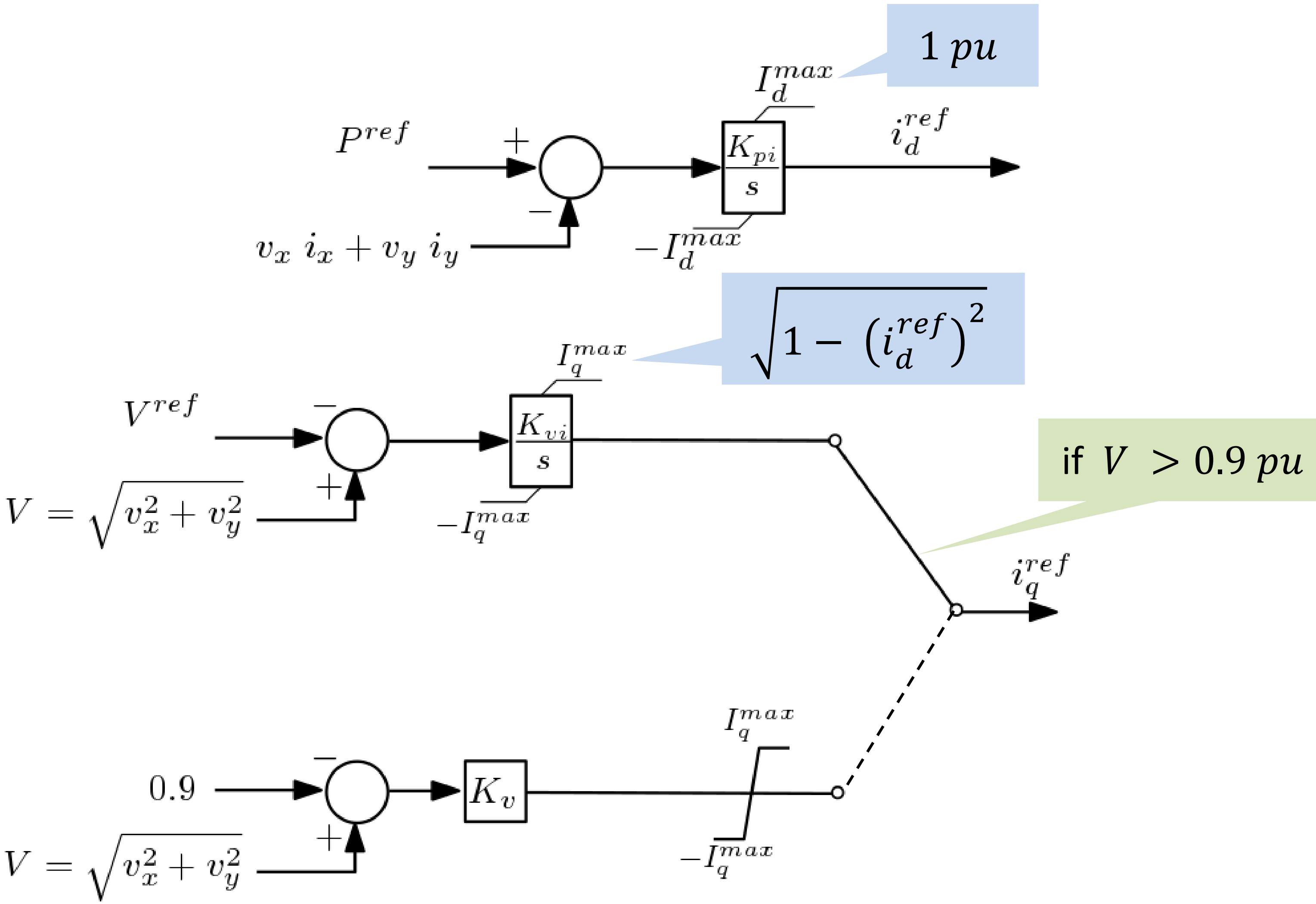
$K_{vi} = 15 \quad K_{pll} = 60 \quad K_{pi} = 30$

$K_{vi} = 60 \quad K_{pll} = 60 \quad K_{pi} = 30$

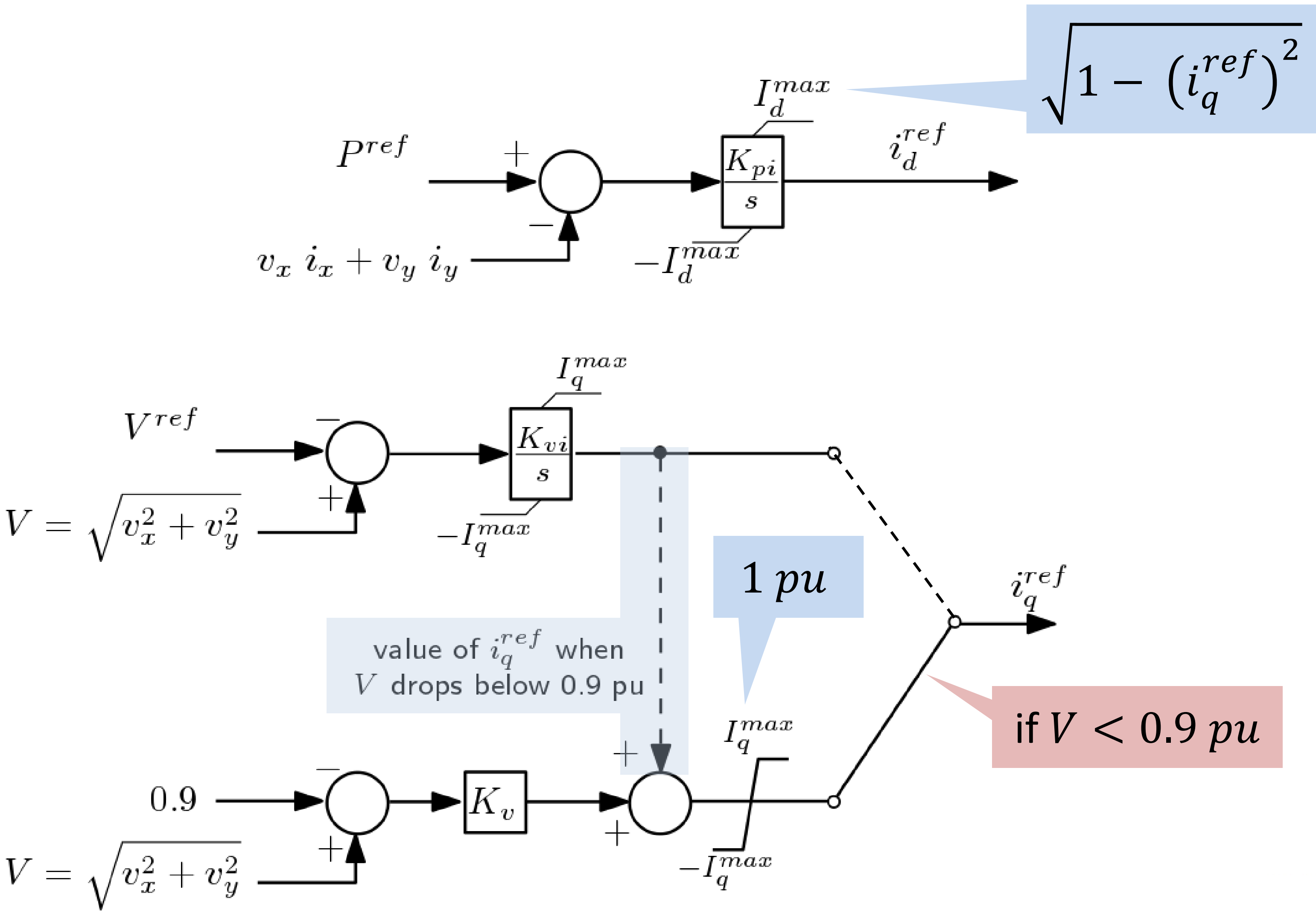
$K_{vi} = 15 \quad K_{pll} = 600 \quad K_{pi} = 30$

making the PLL faster deteriorates stability

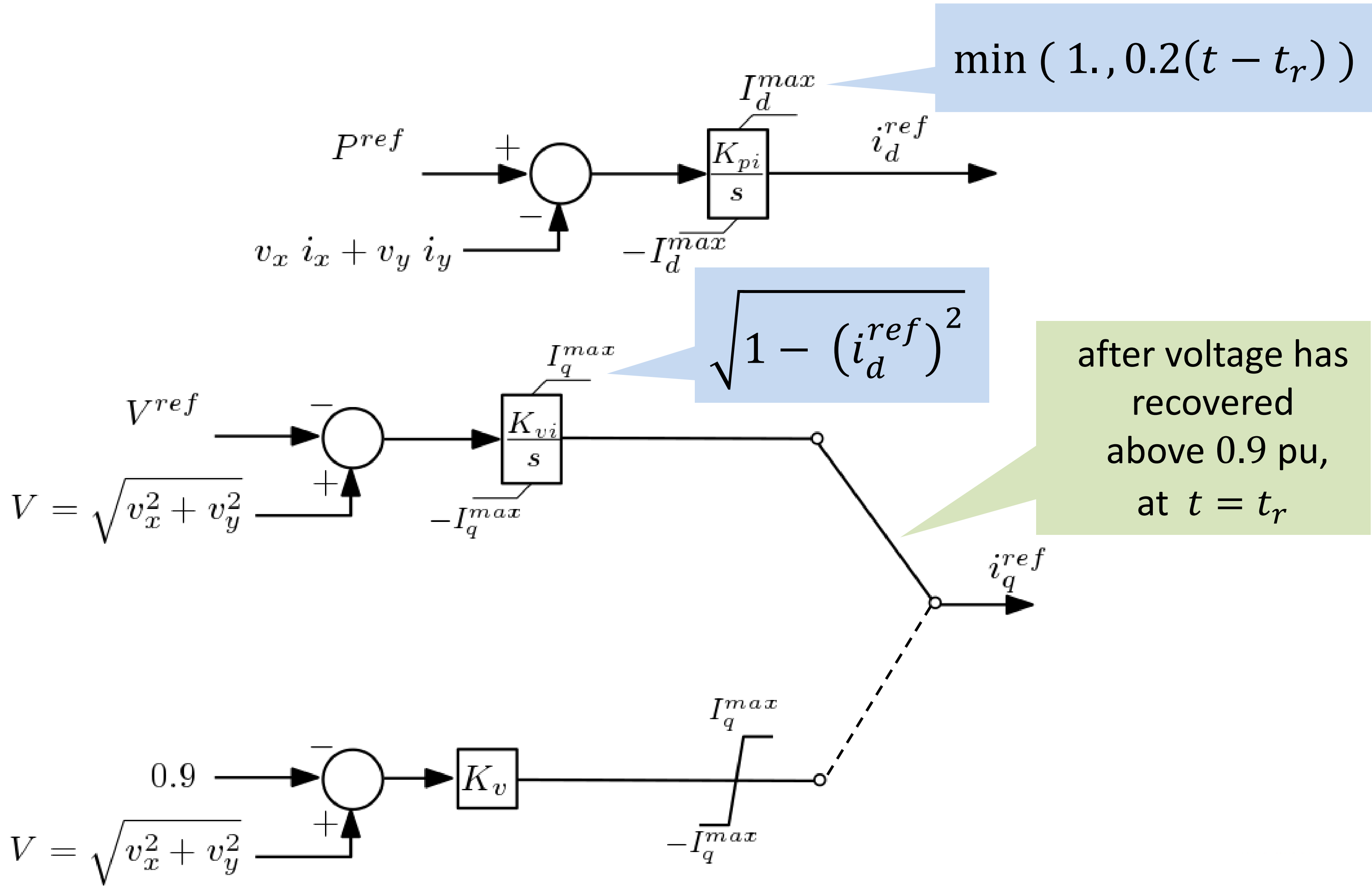
VSC model for large voltage disturbances (1)



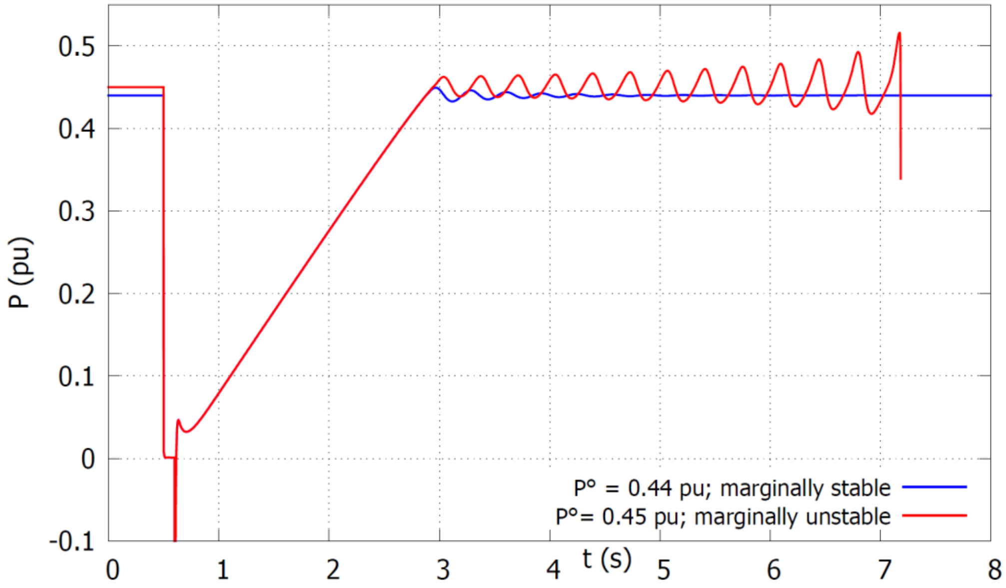
VSC model for large voltage disturbances (2)

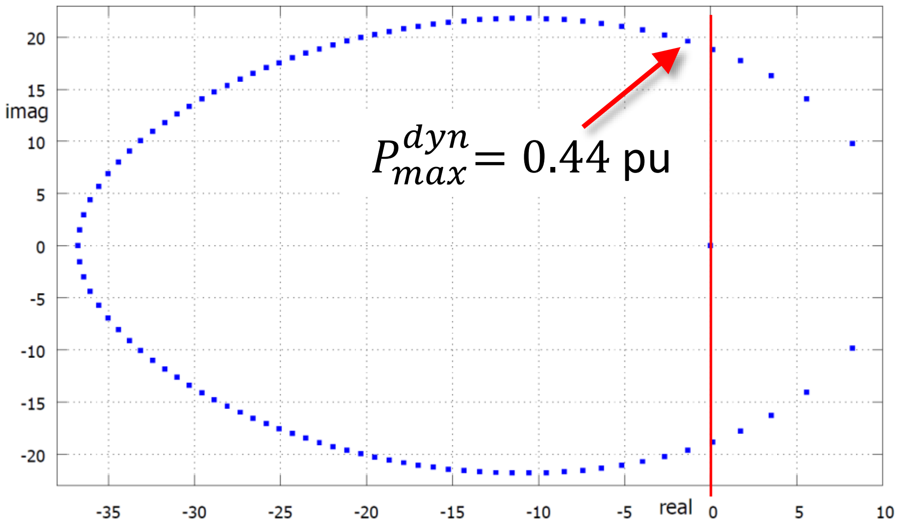


VSC model for large voltage disturbances (3)



Large disturbances validating small-signal analysis



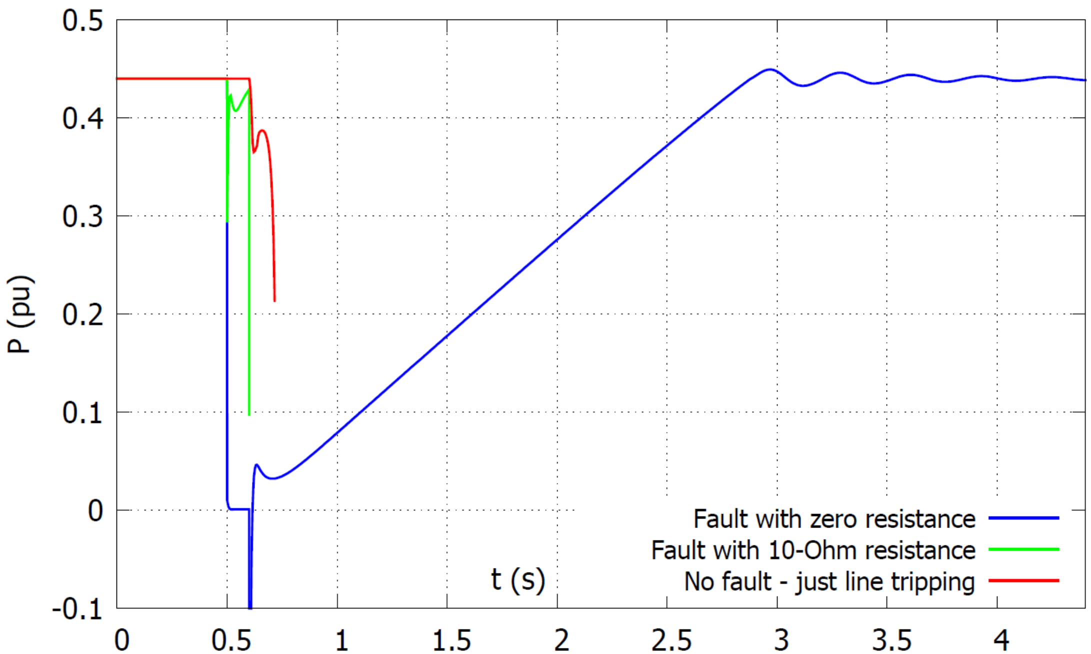


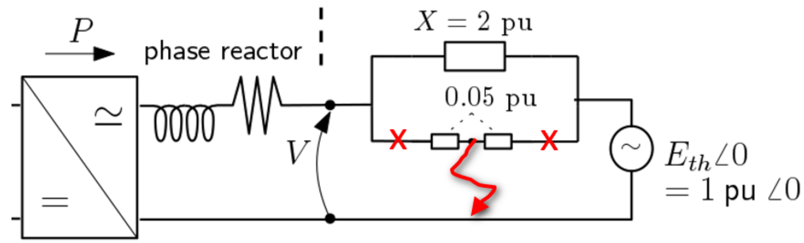
$K_{vi} = 15$ $K_{pll} = 60$ $K_{pi} = 30$

Very good agreement between small-signal analysis and large-disturbance time simulation

- active power recovers with a ramp
- system "smoothly" brought to its final equilibrium point
- $\Rightarrow$ stability limit not influenced by nonlinearities

Large disturbances: a paradox





$K_{vi} = 15$
$K_{pll} = 60$
$K_{pi} = 30$

Milder disturbance with a 10 Ω fault resistance

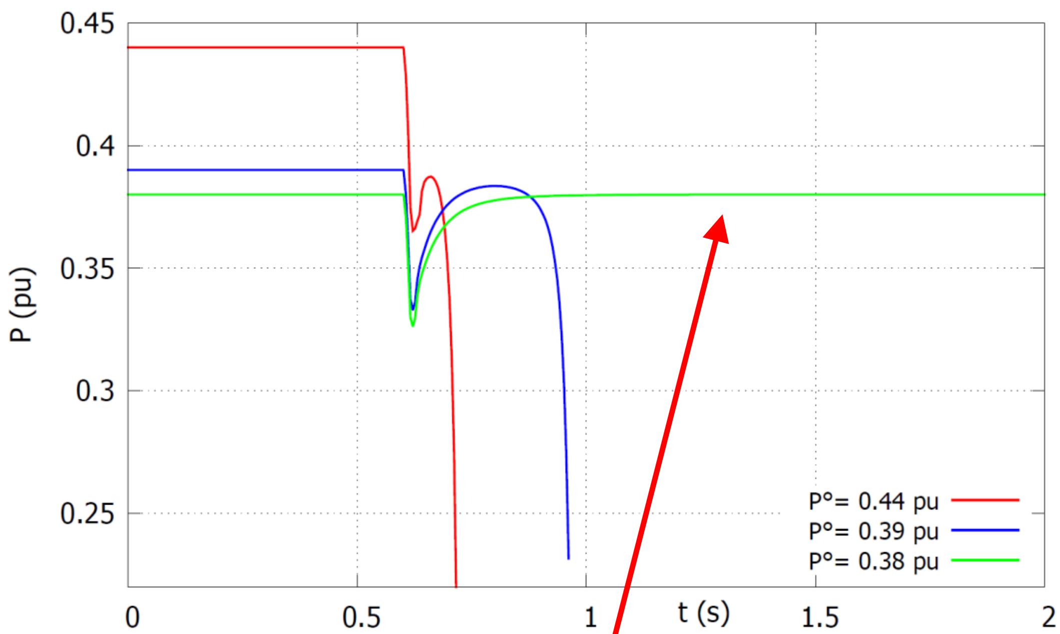
V drops below 0.9 pu, but not as much

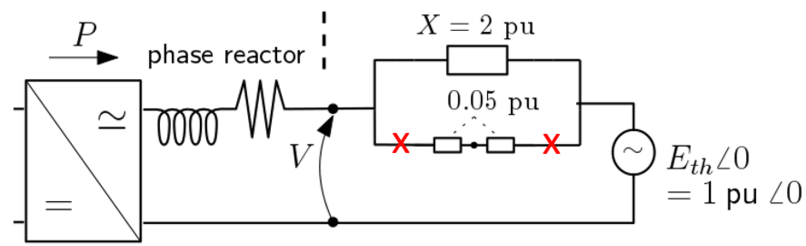
$\Rightarrow$ the injected reactive current is smaller

$\Rightarrow$ there is room for the whole active current (not reduced)

$\Rightarrow$ the pre-disturbance active power is forced immediately

Large disturbances: effective stability limit





line tripping <u>without</u> fault

$K_{vi} = 15$
$K_{pll} = 60$
$K_{pi} = 30$

lower effective stability limit (0.38 < 0.44) pu

Summary

- Power electronics-driven instability after a fault resulting in severe decrease of short-circuit capacity of AC system
- in terms of pre-disturbance power, “static” stability limit P_{max}^{st}
  - $P > P_{max}^{st}$ infeasible; can be detected by static calculation
- “dynamic” stability limit can be more severe : $P_{max}^{dyn} < P_{max}^{st}$
  - determined by small-signal / eigenvalue analysis
  - making V control faster than P control increases P_{max}^{dyn}
  - making the PLL faster decreases stability
- same limit found by large-disturbance time simulations
  - due to the ramp recovery of active power after fault clearing
- **but** fast instability if active current not reduced during fault
  - milder disturbance ⇒ lower reactive current support ⇒ active current not limited (limit case: drop of short-circuit capacity without fault !)

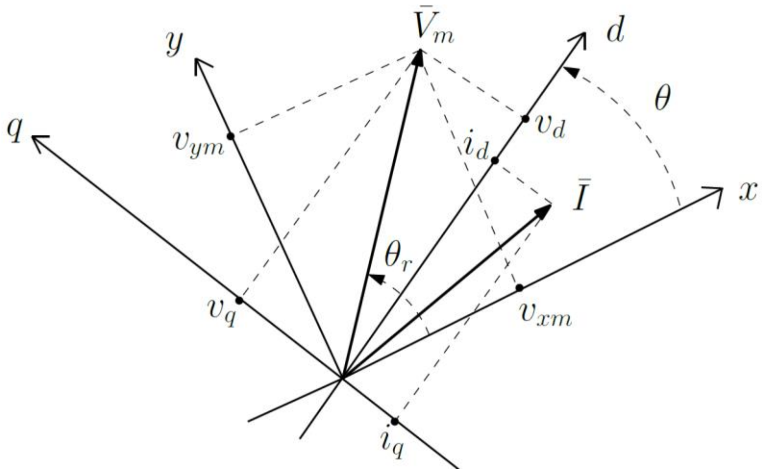
More issues to investigate…

- Adequacy of modelling
  - generic VSC model used in this case study
  - additional controls installed by manufacturers ?
  - combination of phasor-mode and detailed models appropriate ?
- Other forms of instabilities ?
  - harmonics, etc.
- Possibility of detecting the instability from local measurements ?
  - relying on internal signals readily available inside the converter
- Possibility of keeping the HVDC link in operation with a reduced power transfer ?

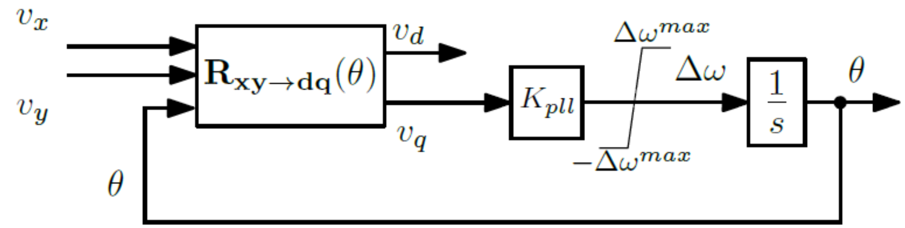
Thank you for your attention !

Discussions on modelling with Prof. Xavier Kestelyn, ENSAM, Lille (France) are gratefully acknowledged

Appendix. PLL and reference frame



Phase Locked Loop (PLL)



(x, y) : reference axes on which time-varying phasors are projected in network equations.

PLL aims at aligning d axis with V_m. In steady state:

$$v_q = 0 \qquad \theta = \theta_r \qquad i_d = i_P \qquad P = v_d\, i_d \qquad i_q = -i_Q \qquad Q = -v_d\, i_q$$

$$\begin{bmatrix} i_x \\ i_y \end{bmatrix} = \underbrace{\begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix}}_{\boldsymbol{R}_{dq\rightarrow xy}(\theta)} \begin{bmatrix} i_d \\ i_d \end{bmatrix} \qquad \begin{bmatrix} i_d \\ i_q \end{bmatrix} = \underbrace{\begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix}}_{\boldsymbol{R}_{xy\rightarrow dq}(\theta)} \begin{bmatrix} i_x \\ i_y \end{bmatrix}$$

Appendix. Data

VSC

- $S_N = 1000$ MVA
- $V_N^{ac} = 400$ kV
- $V_N^{dc} = \pm 320$ kV
- $R = 0.01$ pu
- $L = 0.2$ pu

Controls

- Inner Loops :

  $K_P = 0.127$ pu/pu

  $K_I = 2$ pu/(pu.s)

  → response time ~ 5 ms
- PLL :

  $K_{pll} = 60$ rad/(pu.s)
- Outer loops :

  $K_{PI} = 30$ pu/s

  $K_{VI} = 0.01$ pu/s

  $K_V = 2.5$ pu/pu