

Design for a multi-channel recording and stimulation device

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Abstract

Deep brain stimulation and brain implants carry great promises: possibilities to stimulate areas of the brain to prevent or treat failures of the nervous system. Today, most devices used in this domain are not capable of restricting their action to specified anatomical targets due to the large size of the electrodes. In 2007, the BES-group (imec) developed an array of small electrodes interacting at a single neuron level, both for recording and stimulation.

The present master's project focuses on the realization of a multi-channel recording system for neural applications. The read-out conditions and digitizes eight channels and provides the digitized output to an existing TI MSP430 based microprocessor system for wired or wireless data handling. The resulting platform will be used as a prototype for extensive experimental testing by biomedical scientists from the BES-group.

The first step in the study is the analysis, from a theoretical aspect, of the conditioning and digitalization of the signals: low-noise amplification, filtering, offset compensation and digitization. A SNR study is performed, leading to the selection of electronic components suitable for our project. Afterwards, the PCB layout is conceived in a miniaturized SMD design style. The code implemented in the microprocessor MSP430 is detailed both for the recording of a single channel and eight channels concurrently. Adaptation of the amplification factor can be carried out either by digital processing or by user interaction. Design of the wireless link between a PC and the board is then considered. The link is built from the eZ430-RF2500 Development Tool (Texas Instruments), a complete USB-based wireless development tool providing all the hardware and software to create a wireless network.

Eventually, the performance and limitations of our design are evaluated. Our design handles properly the entire frequency range of action potentials for both wired and wireless configurations. The major limitation is a lack of accuracy for signals below $500\mu V_{pp}$. Solutions for future designs are proposed including suppression of the offset compensation circuit and acceleration of the UART communication. Ideas for the addition of stimulation functions are proposed in hopes of a closed-loop approach, which could allow for adjustment and fine tuning of stimulation. A mixed PCB/IC design may now be considered.

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Chapter 1

Introduction

A brief introduction to biological signal processing history is proposed to start this report. Afterwards, neural implants are described in detail with an explanation of the three parts composing implants: the electrode array, the electronic implant, and the external block. The study and the research environment are discussed at the end of the chapter.

1.1 Biological signal processing

Throughout history, humankind has always been fascinated by the mystery of life and has tried to provide various explanations for birth, death, or disease. In Antiquity, human body functions were attributed to witchcraft, will of gods or demons. Perceptions of our organs' function were various: the view of the heart as being the source of consciousness was the current belief until Hippocrates, who believed that the brain was not only the center of sensation but also the center of intelligence [6]. Aristotle, however, imagined the heart as the center of intelligence, and the brain as responsible for cooling the blood [8].

During the past millennium, the rise of scientific medicine has altered or replaced many old beliefs. Progress made by modern surgery during the sixteenth, seventeenth and eighteenth centuries broadened our understanding of many mechanisms involved in the human body. In the late twentieth century, dramatic advances in the field of computer technology brought the limits of medical science even further. At approximately the same time, scientists discovered that human physiology is composed of many electrical phenomena [11]. In the early eighteenth century, biologists and physicists managed to find a connection between electricity and nervous functions [28]. L. Galvani was the first to demonstrate, in the second half of the eighteenth century, the presence of electricity in animal tissues [26]. At that time, the lack of sensitive instruments with sufficient accuracy prevented the study of electrical transients accompanying muscle excitation. In 1865, J. Bernstein and

E. du Bois-Reymond surpassed those technical limitations and recorded for the first time in history the entire course of an action potential [28].

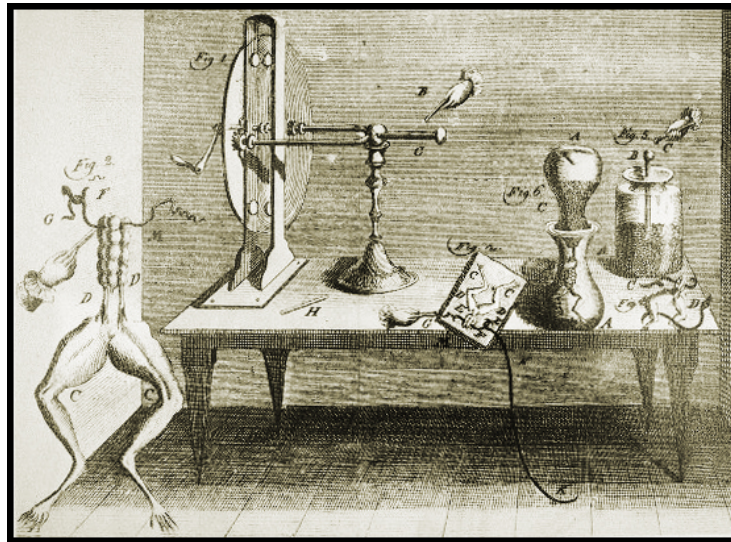


Figure 1.1: Illustration of L. Galvani's experiment on frog muscles [26]. This experiment was the first to demonstrate the presence of electricity in animal tissues.

Most bioelectric signals, however, are small and require great amplification. It is only with the appearance of the amplifier, in 1947, that it finally became possible to record very tiny currents and potentials from the human body [37]. Since then, huge progress has been made in medical signal processing. Various engineering disciplines such as informatics, modeling, and signal processing have made it possible to extract relevant information from bioelectric signals. Nevertheless, neuroscience as a discipline is still in its infancy, and much remains unknown about the brain's mechanisms and functions. A better understanding of the brain would allow for the design of a broad range of applications of use to researchers, clinicians and neuroscientists, or even to the creation of everyday objects such as neural implants or brain-computer interfaces [2].

1.2 Neural implants

Brain functions can be severely altered by accidents leading to traumatic brain injuries or by diseases such as strokes, cancers or Alzheimer's. Currently, there are no medical instruments capable of restoring cognitive function, but recent progress in neurophysiology coupled with development of engineering techniques, especially in neurotechnology, has

introduced the era of a new class of devices: the *neural implant*.

Two kinds of implant can be distinguished [29]:

- *Motor devices*, which inject signals into the nervous system;
- *Sensory devices*, which extract nervous signals and send them to a device, such as a robotic arm, or directly to a computer.

With these new devices, a broad range of medical applications becomes available. Among others, the *cochlear implant* restores hearing to thousands of people¹, and *deep brain stimulators* electrically stimulate areas of the brain to prevent or treat, for example, the symptoms of Parkinson's disease [20], dystonia, essential tremor or epilepsy [22].

Usually, a neural implant is made of three different parts [13](figure 1.2):

- An array of reception and stimulation electrodes;
- An electronic implant to provide energy to the electrodes;
- An external transmitter/controller block.

1.2.1 The electrode array

The electrode array acts as a transducer. Its role is to convert one type of energy into another. There exist two kinds of connection to neural tissues: recording and stimulation. As such, the electrodes act in a different manner and we need a description of the two in order to understand the entire mechanism.

The electrical charge balance of a neural cell is influenced by the electrode array in the vicinity of the cell [7]. Neural stimulation corresponds to a depolarization of the cell's membrane (see section 2.3) achieved by an ionic flow between electrodes, at least one of which is in the vicinity of the target tissue. The electrical stimulation is, in most neural applications, applied as a series of biphasic current pulses. Each pulse has an overall zero net charge flow thanks to an equilibrium between the amplitude and the duration for the positive and negative phase (see figure 1.3). The negative phase corresponds to a cathodal current and the electrons' flow is from the electrode to the tissue. On the contrary, the positive phase is produced by the anodal current going in the opposite direction.

¹Presently speaking, 188 000 patients possess this cochlear implant [38].

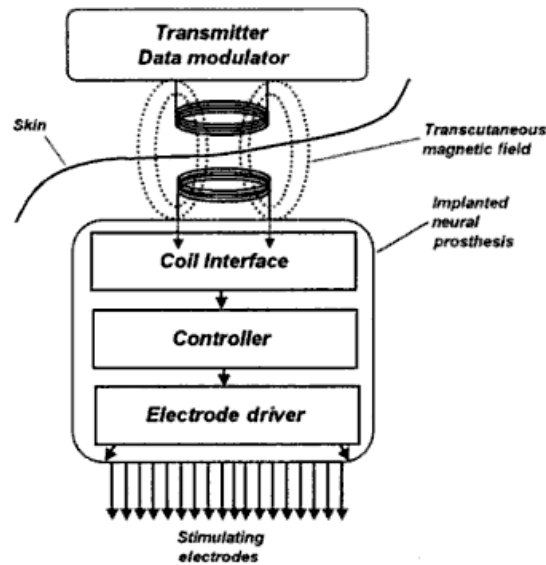


Figure 1.2: Representation of a neural implant's block diagram [13]. The three different parts are shown on this figure: the array of electrodes, the electronic implant and the external transmitter/controller block.

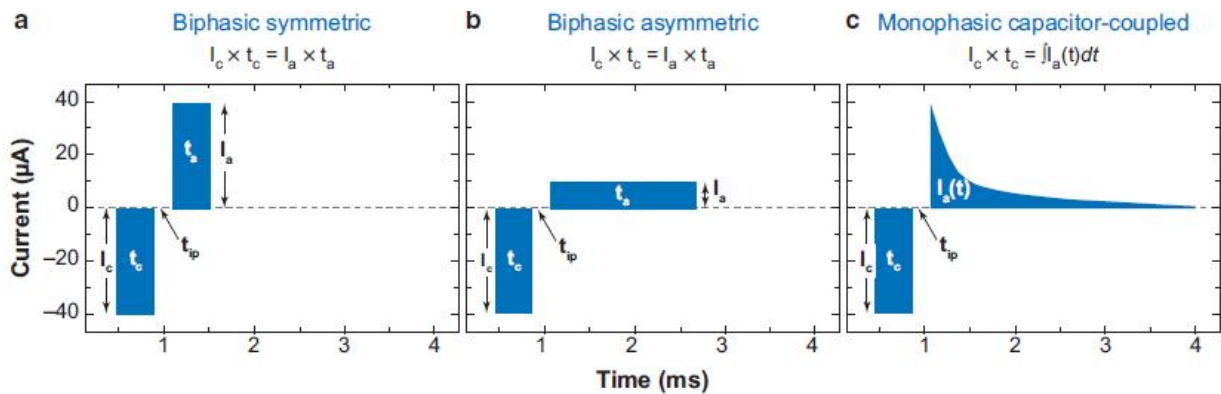


Figure 1

Typical charge-balanced, current waveforms used in neural stimulation. The parameters vary widely depending on the application and size of the electrode. Waveform parameters usually falling in the range of I_c (cathodic current), $1 \mu\text{A} - 10 \text{mA}$; I_a (anodic current), $1 \mu\text{A} - 10 \text{mA}$; t_c (cathodic half-phase period), $50 \mu\text{s} - 4 \text{ms}$; t_{ip} (interphase dwell), $0 - 1 \text{ms}$; and t_a (anodic half-phase period), $50 \mu\text{s} - 10 \text{ms}$.

Figure 1.3: Ionic flow between electrodes [7]. The positive and the negative phase are shown on each graph. An equilibrium is made to get an overall zero net charge flow for each pulse. The type of stimulation varies widely with applications.

Neural activity is recorded through the extracellular potential (produced by the action potential, see section 2.3.1) by microelectrodes in the vicinity of the target neurons. The major difficulty in a single-unit recording² is to measure the action potential with a signal-to-noise ratio (SNR) that is sufficiently high (typically, at least 0.5). The amplitude of the change of internal voltage relative to the extracellular fluid is in the order of $100mV$ [12]. However, the amplitude of the signal present in typical extracellular neural recordings ranges from $1\mu V$ to $500\mu V$, depending on the type of electrodes used and conditions in which they are used. The average is $100\mu V$ [14]. Since the signals are small in amplitude, noise sources that can be usually ignored play an important role here and have to be taken into consideration.

Electrodes are the direct interface with biological structures. Several properties must be taken into account and weighed with regard to the biocompatible necessity in order to obtain an optimal stability, efficacy and lifetime with minimum toxic damage to biological tissues. Those properties can be summarized as followed [14]:

- Small electrode surfaces;
- Small creation of irreversible reaction products that could cause inflammation;
- Low frequency dependence;
- Long term stability, i.e., minimal or no corrosion and excellent biostability;
- Material tolerated by the body to reduce tissue reactions.

Recent research in the neuroprosthetics field led to the development of micromachined multielectrode arrays as small as a human hair. An example of this technology is the Utah Electrode Array (figure 1.4). This 10×10 array of platinum-tipped silicon electrodes measures $4 \times 4 \times 1.5mm^3$ [12].

Most electrode arrays possess a small number of large surface area electrodes which prevent them from selectively modulating the electric field and from restricting its distribution only to the desired anatomical target [22]. However, fine-grain stimulation and recording in deeper brain regions is achievable with a 2D-array of small electrodes for selective and targeted interaction on the level of single neurons. The surface of an electrode should be no larger than $2000\mu m^2$ in order to obtain single-unit recording [7]. Also, the development of probes providing a closed-loop approach (recording-stimulation-recording) would allow for adjusting and fine tuning of the required stimulation pattern [27].

²Single-unit recording is the use of an electrode to record activity from a single neuron.

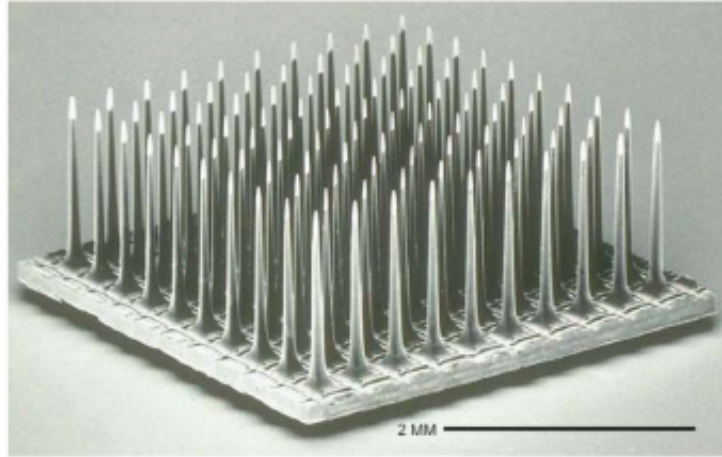


Figure 1.4: Utah Electrode Array [12].

1.2.2 The electronic implant

The electronic implant plays several distinct roles:

- Analog to digital conversion and vice-versa;
- Communication with the external control block. For example, in wireless applications, modulation and demodulation of the signals by a coil interface;
- Control of the electrode array.

Being the object of the current work, the analog and digital conversions are explained in more details in following sections. Weak neural signals must be first amplified and then processed (filtered and digitized) using very low-noise circuits. However, power dissipation must be strictly limited to prevent tissue damage³ and a trade-off between noise and silicon area might be an issue.

The first component of the electronic implant is very often a front-end selector. This selector results from a trade-off: many recording sites are necessary for correct neurophysiological studies but only a small subset of them can be processed given the limitations in both power dissipation and chip area. Moreover, the selector can be used to move the recording sites electronically and to permit both depth scanning and field zooming. Ji & al.[17] give an example of a selection of eight electrodes out of the thirty-two available.

³Cells die if they are exposed to elevated temperatures for a long period of time. The precise limit to power dissipation is difficult to establish but a chronic heating to less than 1°C is achievable [12].

The selector is composed of a grouping network, eight 4-to-1 multiplexers (the thirty-two electrodes are divided into eight groups of four and only one out of the four sites is selected at a time) and a shift register. The shift register controls the selection of one out of the four electrodes for each 4-to-1 multiplexer (see figure 1.5).

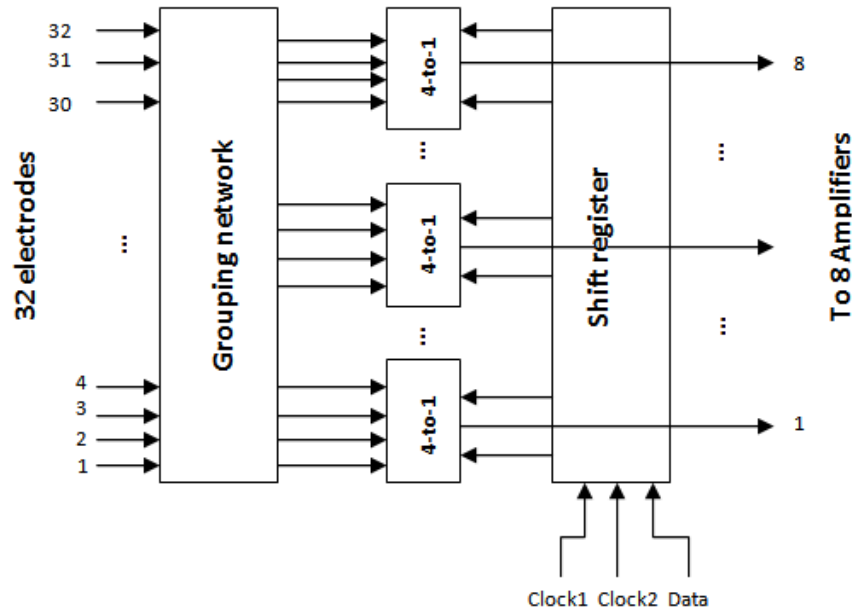


Figure 1.5: Illustration of a front-end electrode selector [17]. This selector selects eight electrodes out of the thirty-two available and is made of a grouping network, eight 4-to-1 multiplexers and a shift register.

After this first stage, a bank of low-noise amplifiers must be used in order to increase the amplitude of the very weak signals. Each selected electrode corresponds to its own dedicated amplifier. It would be tempting to use an analog multiplexer but time constants in the amplifier dynamics are typically much longer than the multiplexer switching time required to catch brief neural activity across an array of many electrodes [12]. Furthermore, a multiplexer would be another source of noise, which is to be avoided at all costs. This array of amplifiers will consume a relatively large chip area and energy.

The amplified signal is then filtered in order to avoid aliasing. The signal is digitized because digital transmission is more robust than analog, if a proper choice of source coding and carrier modulation is made. After digitization and for wireless applications only, the signal is compressed into a single serial data stream and sent to a radiofrequency modulator for transmission to an antenna outside the body.

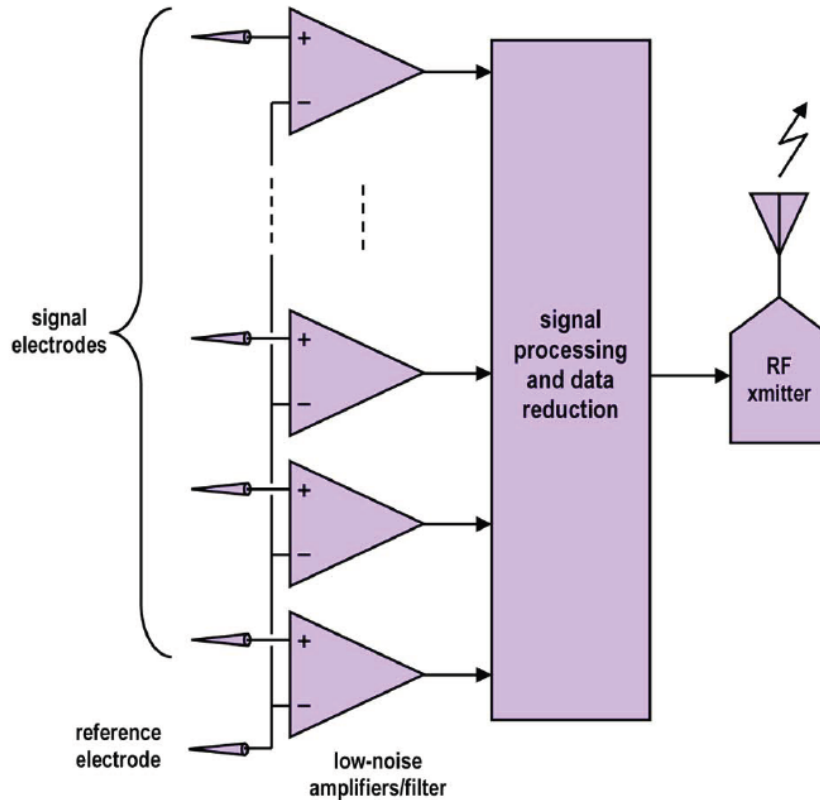


Figure 1.6: Block diagram of wireless neural recording device - implanted part [12].

1.2.3 The external block

Very often, the communication between the internal and external blocks is made through a radio frequency (RF) link⁴. This RF transmission of data over a wireless transcutaneous link is very difficult to handle in small, implanted systems especially if they are power dissipation limited. In addition, the RF link is weakened by the fact that the absorption power of electromagnetic radiation of the biological tissues follows an f^2 law. That is why a dedicated relatively low-frequency band of $402 - 405MHz$ has been allocated for RF transmission of active medical implants [12].

One of the roles of the external block is to supply the implant with sufficient power. Batteries' limitations in both time and size prevent the use of traditional power supplies. A possible solution is to handle the power supply by an air-tissue transformer. An RF signal is applied to the external coil (transmitter) which induces current in the internal coil (receiver), and the current carries both power and data. This phenomenon results from

⁴The two blocks could also be wired.

the variation of the magnetic field generating an induced current to oppose any change causing it (*Lenz' law*) [13] [30]. However, this system is dependent on a large-capacity external power and, moreover, as the size of the implant acts smaller, the magnetic coupling between the two coils declines rapidly. To maintain a sufficient amount of power and reliable communication, a strong signal must be delivered by the primary coil, which increases the risk of tissue damage due to RF absorption [30]. Other solutions must thus be foreseen.

Using a battery to power neural implants is a major drawback because surgery is required for its replacement. Nevertheless, in some low-power consumption applications, it might be the easiest and most robust solution. Another approach to deliver energy to neural implants is to take advantage of the abundant supply of energy from the food we eat (for example, the approximative power consumption of the brain for one minute is 20W [30] and even a small fraction would be sufficient to power the neural implanted device). This idea leads to the design of biofuel cell (BFC) which will not be addressed in greater detail in the current work.

The other main role of the external block is wired or wireless data transmission in two directions. In the wireless case, this is achieved by the exact same mechanism as for the power supply, namely by the air-tissue transformer [13]. Another possibility is to take advantage of the volume conduction property of biological tissue to form a natural cable available for wireless data communication [30]. Data transmission allows the external block to control the implant and to receive the measured signals. As such, the external block provides the interface with the human user.

1.3 The research environment

This project was undertaken at the imec research center in the *Bio-Electronic Systems Group*. This group is part of the *Bio-Nano Electronics department*, a subdivision of the *Smart Systems and Energy Technology (SSET)* division. The department currently consists of two groups (FNS and BES)⁵.

1.3.1 FNS-group (Functional Nanosystems)

The FNS group works on the development of nanodevices for biological applications such as biosensors and integrated lab-on-a-chip systems. All activities of the group are mingled but can roughly be divided in following activities:

- Biomagnetism: magnetic sensing and bead actuation on chip;

⁵This entire section is based on the *working in the biolabs brochure* [35].

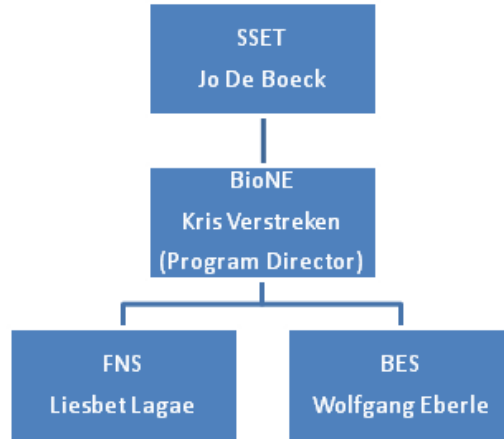


Figure 1.7: Organization chart of the Bio-Nano Electronics department [35].

- Plasmonics: optical related sensing mechanisms and devices;
- Nanofluidics and -ionics: nanopore fabrication and research;
- Nanoparticle synthesis: core-shell particles;
- 2D and 3D surface functionalization: assay design and optimization.

1.3.2 BES-group (Bio-Electronic Systems)

The BES-group works on the development of cell-IC interfacing technologies in the nano- and microdomain, including microsystems and implants. Group members have an engineering/physics or life science/medicine/biochemistry background. The group works on theoretical and experimental techniques with a strong focus on validation of technological developments in a realistic biological context (cultured cells, cultured tissue slices, acute slices, *in vivo* small animals). Activities can be largely subdivided into:

- Microelectrode-based cell-IC, array-based sensor and actuator systems (*in vitro*);
- *In vitro* assay development for drug discovery and drug testing;
- Microelectrode-based implantable sensors, actuators, and microsystems (*in vivo*);
- Realistic *in vitro* and *in vivo* characterization and modeling of electrode interfaces;
- Multi-modal cell-IC interface systems (optoelectric, chemical, microfluidic).

The current study is part of a project from the microelectrode-based cell-IC array-based sensor and actuator systems.

1.4 Ethical considerations

The major promise of deep brain stimulation is that lost functions could be recovered by artificially recreating or bypassing the neural substrate lost. However, considering the risks of any invasive intervention, patients and physicians must foresee what, if any, alternatives exist. Indeed, behavioral side effects such as apathy, hallucinations, compulsive gambling, cognitive dysfunction, and depression are reported in the literature [38].

There exist different opinions about brain implants. Transhumanists see them as part of the next phase of human evolution. On the contrary, bioconservatives view them as step on the path to mind control or other drastic technical changes to the human race. What is sure is that certain factors should be taken into consideration before any intervention [1]:

- Patient selection: having a well-defined procedure for patient selection based on carefully chosen criteria;
- Informed consent: the patient is able to make his or her decision based on a reasonable understanding and appreciation of the risks and benefits of a procedure;
- Public understanding: demystifying miracle-like stories and providing balanced public information;
- Identity: thinking ahead about the the appearance or reappearance of psychiatric symptoms after the implant in illnesses such as Parkinson's and the impacts on psychic health.

1.5 The study

1.5.1 Main purpose

This thesis aims at the realization of a custom multi-channel read-out and stimulation system for neural applications. The read-out will condition and digitize a large set of channels (eight channels) and provide the digitized output to an existing TI MSP430 based micro-processor system for wired or wireless data handling. In the other direction, a bank of current/voltage sources will allow for programmable electrical stimulation.

The BES-group (see section 1.3.2) developed multiple generations of silicon-based multi-electrode neural probe arrays for *in vivo* selective neuronal recording and stimulation [22][23][27]. As an example, the first-generation probe has a $2mm$ long shaft and $200 * 200\mu m^2$ cross-section [22] and contains a resistive four-terminal temperature sensor to record temperature changes in neural tissue especially during stimulation. The probe is carried out on a $650\mu m$ thick silicon wafer with $250nm$ thermal oxide on both side. Metal

interconnects are made of titanium/platinum leading to platinum contacts of $50\mu\text{m}$ diameter. The biocompatible insulation material used is the Parylene C. The electrode plating is nickel covered with a stack of titanium/gold for improved biocompatibility [22]. The process flow is shown on figure 1.8.

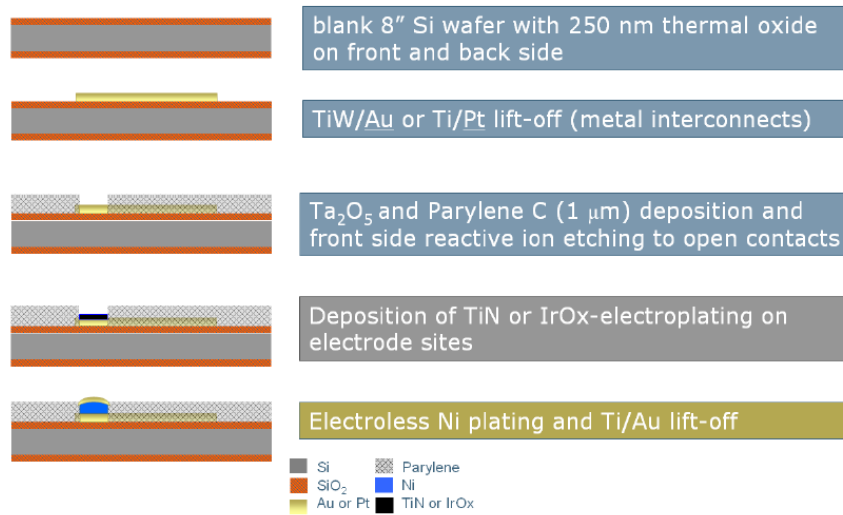


Figure 1.8: Neural probe fabrication: design of the process flow [22].

Custom silver/silver chloride reference electrodes were created to be co-implanted with the probes. These have the advantage of having higher stability and reliability than plain platinum or stainless steel commercial reference electrodes. Connectivity to external instrumentation is carried out using a flat ribbon-cable inserted into a FPC (flexible printed circuit) connector (OMRON connector). Photographs of the fabricated probe assembly are shown on figure 1.9.

Several experiments in the cortex of an anesthetized rat were performed with this probe. Recordings were performed in the motor cortex with the implant position controlled through a stereotactic frame with an external reference system [22]. The obtained SNR was acceptable (approximately 3:1) and the brain activity was detectable: noise level was approximately $20\mu\text{V}_{pp}$ while spike amplitudes were up to $80\mu\text{V}_{pp}$ [22][27]. The reference electrodes' average drift ranges from $10.3 \pm 0.1\text{nV/s}$ to $33.9 \pm 0.6\text{nV/s}$ [23] which leads to an observed DC⁶ offset of a few millivolts, level acceptable for the envisaged purpose. Moreover, the

⁶DC stands for direct current. In engineering, DC refers to the constant local mean value of a voltage or current. On the contrary, AC stands for alternating current and refers to the variation of voltage or current around the DC value.

MRI compatibility of the probe was tested and validated [27] which could offer a valuable research tool for studying mechanisms of deep brain stimulators more deeply. An example of *in vivo* recording is given in figure 1.10.

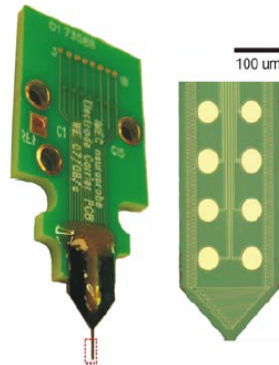


Figure 1.9: The fabricated probe assembly: photograph of the packaged neural probe on the left. The probe tip is marked by a dashed rectangle. Photomicrograph of the probe tip on the right. Contact sizes are $50\mu\text{m}$ [27].

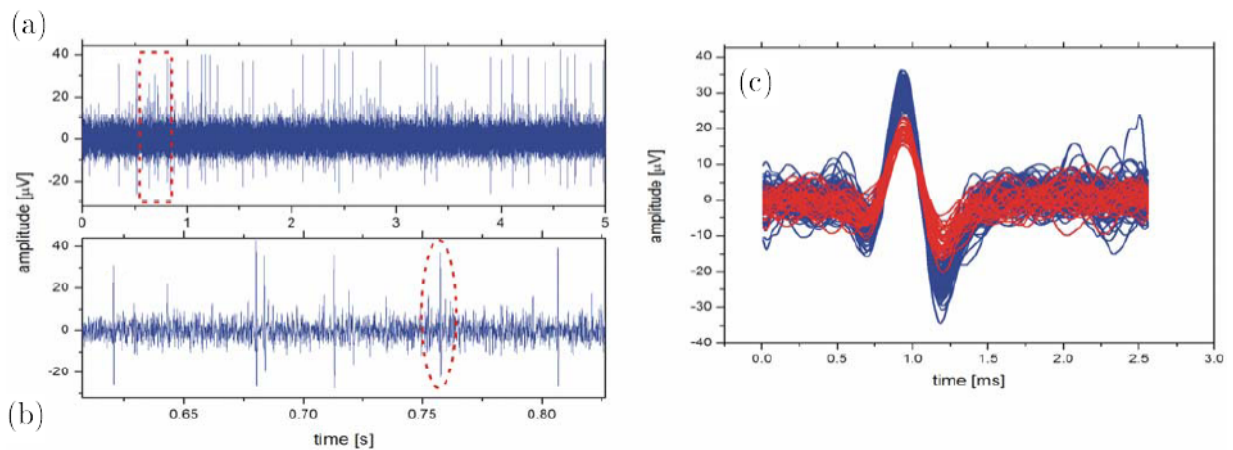


Figure 1.10: *In vivo* cortical recording [27]. Representative cortical recording traces performed by the BES probe. (a), (b): Two traces of band-pass filtered raw signal. (a): 5s recording trace. (b): A magnified stripe (see insert in (a)). One representative spike is outlined. (c): Neuronal action potentials (spikes) detected automatically using the software Osort, a freely available online spike-sorting algorithm. Two different spike waveforms are apparent.

The major development in the thesis is on the analog multiplexing, filtering, and digitization of multiple channels for the read-out using already a miniaturized SMD design style. Special attention should be given to the miniaturized connections as well. Adapting the control software in the MSP430 and generating the wireless data handling is part of the thesis. The resulting platform will be used as a prototype for extensive experimental testing by biomedical scientists from the BES-group.

1.5.2 Organization

This report is divided into six major parts:

- Brief overview of necessary background useful for the project. This consists of short background on the brain, the mechanisms involved in the brain, and, in somewhat greater detail, a consideration of the concept of neuron and cell excitability.
- Theoretical considerations for recording a multi-channel system for neural applications. This step is of the highest importance because it allows us to refute or accept a set of electronic components according to specific criteria. A parameter exploration is performed to accept a final design.
- Hardware design. The purpose of this section is to identify issues such as connector placement, form factor and size of the printed circuit board (PCB). Low-pass filters, connections to other boards and power supply considerations are addressed in this section.
- Software design. This section describes the code implemented in the microcontroller MSP430 with a distinction between the recording of a single channel and the recording of the eight channels sequentially.
- Wireless link. Description of the wireless link created for the application from a software and hardware point of view.
- Description of the testing procedure and analysis of the results. This part describes the different instruments used to test our design as well as the practical considerations taken in order to test the device in conditions as close as possible to the real ones. The PCB provides us with practical means to verify our parameter exploration results and to identify whether our circuit is suitable for its application or not. An analysis of the outputs and the performance is carried out. This part of the study allows us to determine what should figure on a final PCB for future work.

Chapter 2

Background

This study focuses on processing signals generated by the brain and more specifically by neural cells. This is why it is important to recall some major concepts and definitions about the brain's organization and the nervous system. Our description begins from a macroscopic point of view and will continue with microscopic phenomena. The neuron's excitability is detailed more precisely because it constitutes the main feature useful for our study.

2.1 The nervous system

All we know about the external world, and all we can do about it, depends on our nervous system. The nervous system is divided into the central nervous system (CNS) and the peripheral nervous system (PNS). The CNS is the portion composed of the brain and the spinal cord. It is responsible for the reception, processing, integration and emission of nervous signals. The way we move, the way we eat, the way we breathe and the way we think are all determined by the CNS. On the other hand, the PNS takes care of cutaneous and proprioceptive sensation, motor control and the autonomic nervous system. It is made of sensitive and motor nerves coming from the spinal cord and the cerebellum. The neurons in the PNS send the nervous signals to the spinal cord, signals which are then processed by the CNS [14].

The nervous system works in the following way: in the spinal cord, the neurons transfer the nervous signal (either proprioceptive or exteroceptive) captured by sensors sensitive to pressure, temperature, touch, pain or stretch. These stimuli inform the brain, consciously or not, of what is happening in the body and the environment and generates a response. In the other direction, the neurons transport motor stimuli towards the muscles thanks to the motor nerves or the (para-)sympathetic system (part of the autonomic nervous system). A representation of the nervous system is given in figure 2.1.

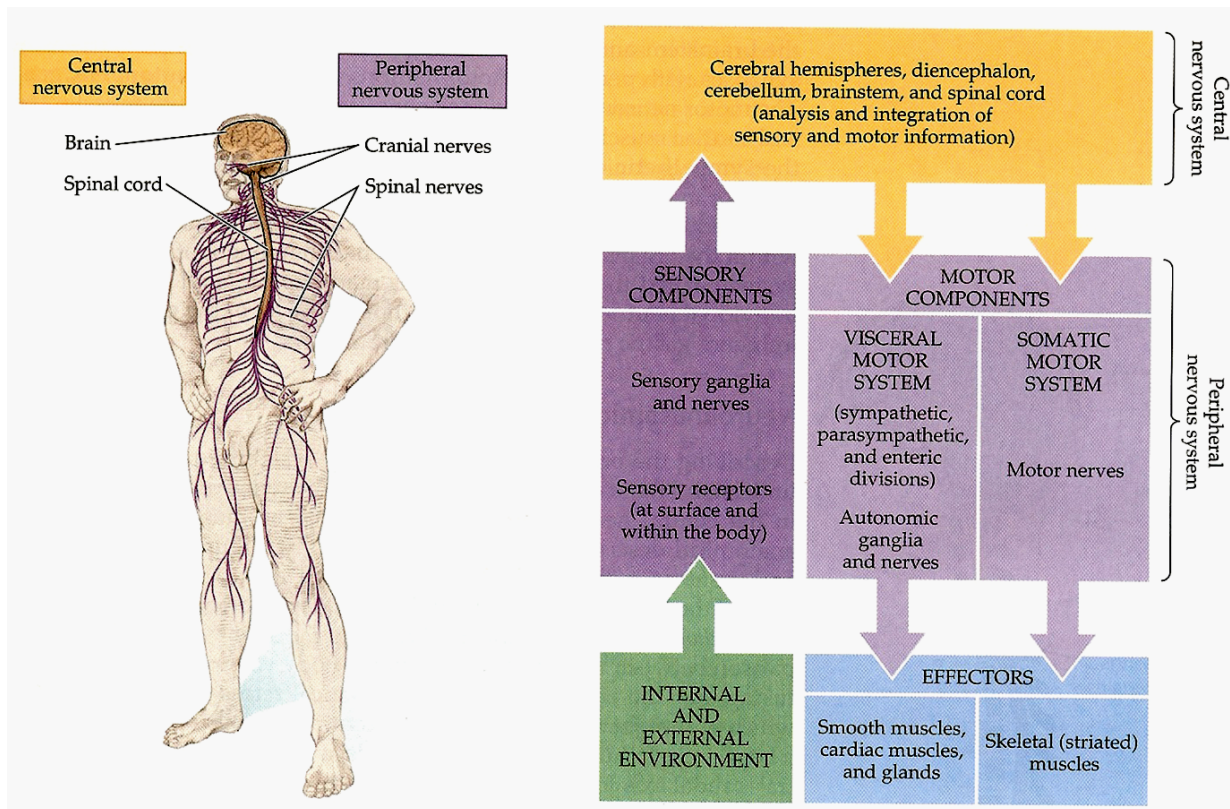


Figure 2.1: Representation of the nervous system [18]. The central nervous system is distinguished from the peripheral nervous system. For each of them, components, functions, and interactions, are detailed.

2.2 The brain

2.2.1 Macroscopic description

The brain can be viewed as a huge network, composed of different entities, which process, in real-time, all the signals to maintain bodily health and to perform specific tasks [11]. The principal entities composing the brain are: the spinal cord, the brainstem, the cerebellum, the thalamus, the basal ganglia, and the primary somatosensory and motor cortex [14]. A representation of the brain is shown on figure 2.2.

2.2.2 Microscopic description

The CNS is composed of two main cell types: neurons and glia. Neurons are responsible for electrical impulse conduction and are detailed more precisely in section 2.3. The large

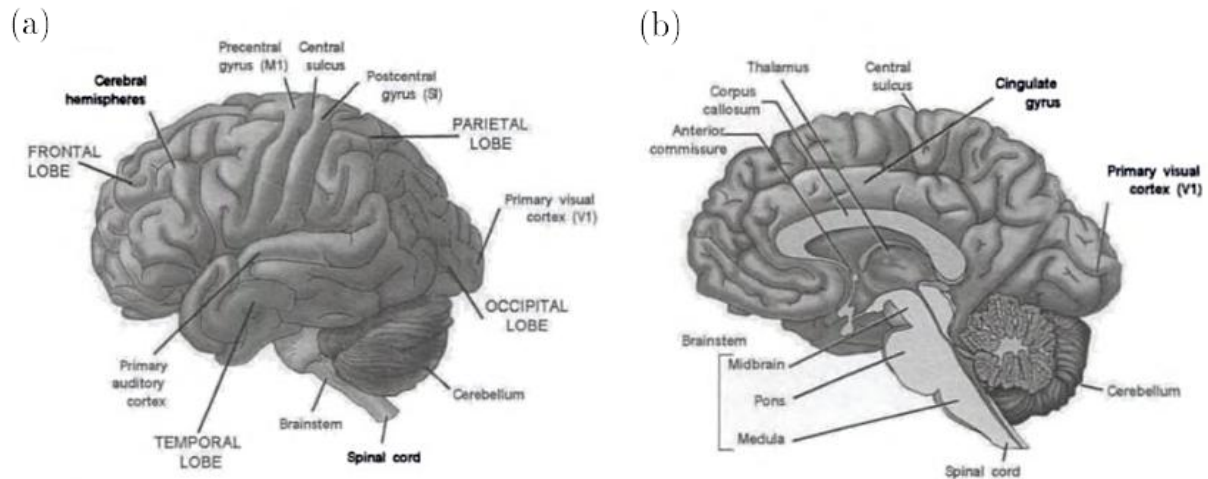


Figure 2.2: Gross anatomy of the brain (a) lateral view (b) medial view [14]. The principal entities composing the brain are shown (spinal cord, brainstem, cerebellum, thalamus, basal ganglia, and primary somatosensory and motor cortex).

majority of neurons are interneurons meaning that their axons do not exit the CNS. Other neurons are the motor or sensory neurons: their cell body is located in the brain or in the spinal cord but they extend their axons outside the SNC to form the efferent and afferent components of peripheral nerves. Glial cells constitute the support matrix for neurons and take care of the provision of insulation for some axons.

2.3 Neurons

As stated in section before, the nervous system contains a huge number of neurons. These cells are the elementary entities in the high density network which constitutes the brain. These neurons are responsible for the transport of electrical signals within the nervous system. There are about ten billion neurons in the brain. Each of them is connected through synaptic contacts to other neurons (each neuron has from one thousand to fifty thousand synaptic contacts). A single stimulus uses billions of synaptic contacts for its propagation and the message is, thanks to this process, transported from the spinal cord to the brain [18].

A neuron is composed of three major parts (shown on figure 2.3):

1. A cell body;

2. An axon;
3. Dendrites.

There exist various morphologies for neurons and they can possess different electrophysiological properties.

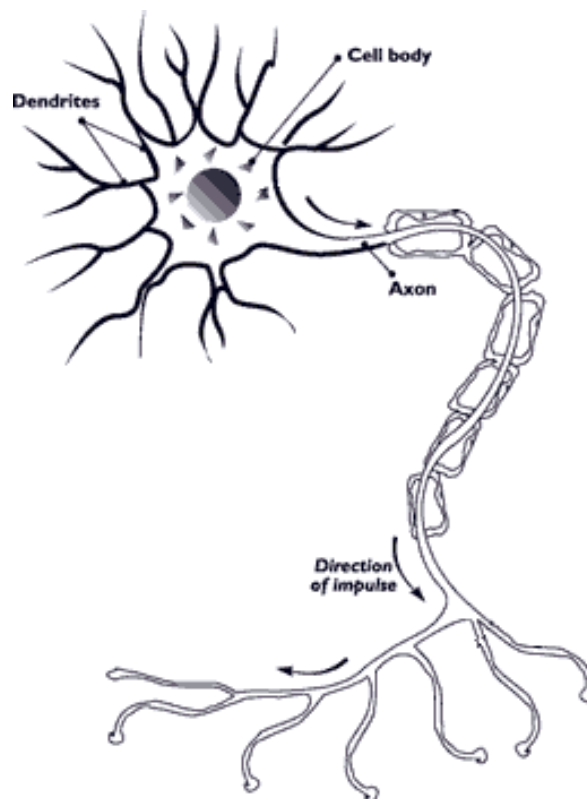


Figure 2.3: A simple description of the neuron architecture [18]. A neuron is composed of a cell body, an axon and dendrites.

The main particularity of neurons is that they are *excitable*, meaning they can be activated by the process of initiating the cell's electrochemical activity, i.e., *excitation*. Excitability is the ability to transmit biological information thanks to a signal called the *action potential* [14].

2.3.1 Action potentials

The action potential represents the cell's activity and can be recorded as a change of potential difference across the cell membrane. This process travels over the cell membrane

to other parts of the cell or to other cells.

When an excitable cell is in a resting state, its transmembrane potential is comprised between -50 and $-100mV$ (depending on the cell type). The cell membrane is thus *polarized*, the inner side being negative relatively to the outer side. This property is due to the ion selective permeability of the cell membrane and to the fact that the membrane is crossed by selective ion channels. Therefore, it is possible for certain ions to cross the membrane easily, whereas for others, it is an effective barrier. The resting potential of an excitable cell depends on several factors, the most important of which are [14]:

- Differences in various ion species' concentration between the inner side and the outer side of the membrane;
- Presence of intracellular charged proteins that cannot pass through the cell membrane;
- Ion selective permeability of the cell membrane;
- Existence of active ions pumps.

There exist two driving fields that act on the ions in each space (intra and extracellular): the *concentration gradient*, giving rise to *diffusion*, and the *electric field*, giving rise to *migration*. With the active transport of ions through the membrane thanks to ion pumps, those driving fields equilibrate each other and the resting membrane potential ($V_m = V_i - V_e$) is computed using Goldman's equation [14]:

$$V_m = -\frac{RT}{F} \ln \frac{P_{K^+} [K^+]_e + P_{Na^+} [Na^+]_e + P_{Cl^-} [Cl^-]_i}{P_{K^+} [K^+]_i + P_{Na^+} [Na^+]_i + P_{Cl^-} [Cl^-]_e} \quad (2.1)$$

where

R is the gas constant

F is Faraday's constant

T is the temperature in Kelvins

P_X is the ion X 's permeability

$[X]_e$ is the extracellular concentration in ion X

$[X]_i$ is the intracellular concentration in ion X .

When a cell is activated, an action potential develops across the cell membrane: the inner side becomes first less negative and afterwards even slightly positive (known as the *depolarization* process). After this slightly positive value, the polarization of the membrane is restored back to normal, to its resting state (the *repolarization* process). For neurons, this process typically lasts from 0.5 to 1ms. During the action potential and even slightly after the action potential, the cell is no more excitable by a new stimulus. This is called the *absolute refractory period*. This period is followed by a time duration when the cell is less excitable, the *relative refractory period*. This entire process lasts about 2ms in neurons.

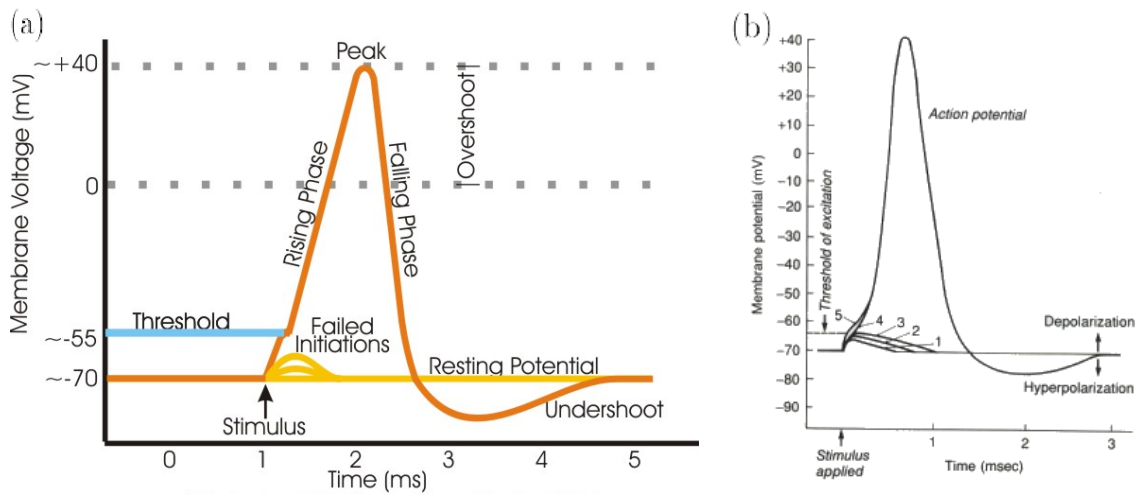


Figure 2.4: Transmembrane action potentials of (a) a skeletal muscle [14] (b) a nerve [4]. The depolarization and repolarization are given as well as the refractory period. The threshold level is indicated on both graphs. The action potential lasts around 5ms for skeletal muscles and 2ms for nerves.

A cell is activated if a stimulus, internal or external, brings the membrane potential up to a *threshold* (the threshold potential is about $-55mV$). The action potential is thus an all or nothing phenomenon. As soon as the membrane potential crosses the firing threshold, the action potential is initiated and sent down the neuron's axon.

The action potential is initiated in the cell body and travels down the axon until it reaches the synapses, where it causes the release of neurotransmitters. These neurotransmitters reach the dendrites of another neuron in the vicinity of the synapse of the first neuron. In response, the target neuron will have either a decrease or an increase of its membrane's potential. An increase of the potential corresponds to excitation of the neuron; in the other case, it is an inhibition. If the change in the target neuron causes the membrane potential to pass the potential threshold, an action potential is initiated and the entire cycle is repeated.

The propagation of the action potential along the axon is performed as a voltage spike. As a section of the axon undergoes the depolarization process, it increases the membrane potential of the neighboring section and, if the threshold is exceeded, a new action potential is initiated in the new section. It is noteworthy that, when a neuron is activated, the action potential is the same regardless of the amount of excitation received from the inputs. What matters is the rate of firing (i.e. the number of times a neuron fires for a given time period) and not the amplitude of the action potential, which is a constant. A weak stimulus will cause a low rate of firing, whereas a strong stimulus will have a high rate as illustrated on figure 2.5.

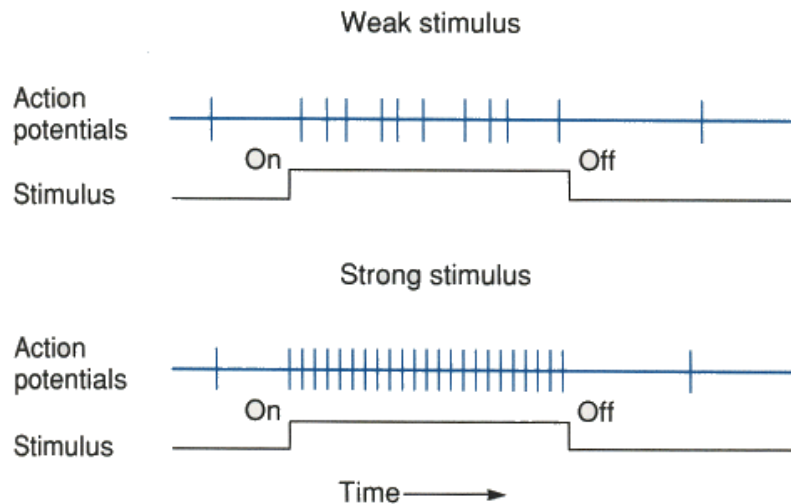


Figure 2.5: Illustration of neuron firing rate law [4]. A weak stimulus leads to a low firing rate (upper curve) and a strong stimulus to a high firing rate (lower curve).

In brief, neural cells take a weighted sum of the incoming signals carried by the dendrites and produce an output signal, transported by the axon, if this weighted sum overpasses the threshold.

Our action on the neuron activity is divided into two possibilities: we can either induce an electric current in the body through electrodes or by application of a varying magnetic field, or measure the electrical activity of a nerve. This is why excitable cells can either serve as electrical stimulation targets or as current sources for recording purposes.

Thanks to the previous explanation of the activity of neural cells, we can deduce that there

exist physical limits to neural signals' amplitude and frequency. Ji et al.[17] set typical limits for extracellular neural signals recording for a single spike from about $100Hz$ to $6kHz$ for the frequency components and about 0 to $500\mu V$ for the amplitude. This order of magnitude is very common in the literature. For local field potentials¹ (LFPs), numbers are quite different: the amplitude can be as large as 1 to $2mV$ and the frequency range is comprised between 10 and $200Hz$ [12].

¹*Local field potentials arise from the synchronous activity of many neurons in one region of the brain. These neurons are too distant from the electrode for their individual action potentials to be resolved, but the crowd noise of many neighboring cells creates a large signal that is easily detected [12].*

Chapter 3

Recording: theoretical considerations

The very first step in our study is the design of the analog-to-digital converter (ADC). This section covers the different validity criteria evaluated in order to establish our ADC design, the choice of the electronic components we made as well as the reasons for this choice and a parameter exploration for the electronic components chosen.

3.1 Problem description

As stated in the previous section, neural signals have a very low amplitude. Furthermore, these signals are very noisy. Indeed, noise sources that can normally be ignored cannot be overlooked any more. Typical sources of noise include [12]:

- Intrinsic noise: thermal noise, Junction noise;
- Electrical noise: line noise, switching noise, digital noise, RF noise;
- Chemo electric noise: overpotentials, corrosion;
- Biological noise;
- Mechanical noise: microphonics.

To be able to detect the amplitude of a very weak signal lost in a dramatic amount of noise, it is necessary to amplify this signal by a significant factor and to limit the noise amplification. However, to neural signals is very often added an offset voltage sometimes reaching amplitude up to $300mV$. To avoid saturation of the amplifier in order to remain in the linear domain, the amplifying factor can not be as high as desired for the AC signal alone. In addition, to extract a correct digitized signal, an offset compensation is necessary.

This offset compensation can be carried out either before the signal amplification, in order to avoid saturation, or after the amplification stage, to limit the amplified noise.

For our study, we consider a signal of interest ranging from $20\mu V$ to $100mV$, an snr ¹ for the input signal of 0.5, a DC-offset of maximum $300mV$, and a measurement bandwidth of $100kHz$. As explained in section 2.3.1, the highest action potentials' frequency is bounded by $10kHz$. A convenient sampling rate is for example $30kHz$, rate which respects the *Nyquist-Shannon sampling theorem*:

Theorem 1.

$$f_{sampling} > 2 * f_{max} \quad (3.1)$$

where f_{max} represents the highest frequency in the original signal. This theorem ensures the exact reconstructability from samples obtained at the uniform sampling rate $f_{sampling}$.

3.2 Validity criteria

The purpose of this section is to design an ADC with an SNR acceptable at the end of the processing chain (0.5 is an acceptable value for the digitized snr). The entire system must remain in the linear domain, i.e, saturation is prohibited by all means. Active offset compensation should be an option.

The two validity criteria we will look after are:

- An snr higher than 0.5;
- A linearity constraint along the entire chain.

3.3 Noise

For the rest of this section, a brief reminder on the noise and noise's computation is necessary. Indeed, we will focus on the SNR and on the different sources of noise we find in our design. This is why a brief recall is not superfluous and more information can be found in appendix A.

The noise is *an undesirable random signal, intrinsically linked to the physical nature of the components and present in all components. Its instantaneous amplitude follows a zero mean Gaussian law* [34]. Here, we consider that the only noise present is of the *white noise* type. Indeed, most noises are white noises and any *pink noise* (or $\frac{1}{f}$ noise) can be

¹Square root of the SNR.

approximated, in the region of interest, by a white noise (see figure 3.1). A white noise is a random signal which power spectral density is independent of the frequency f [25].

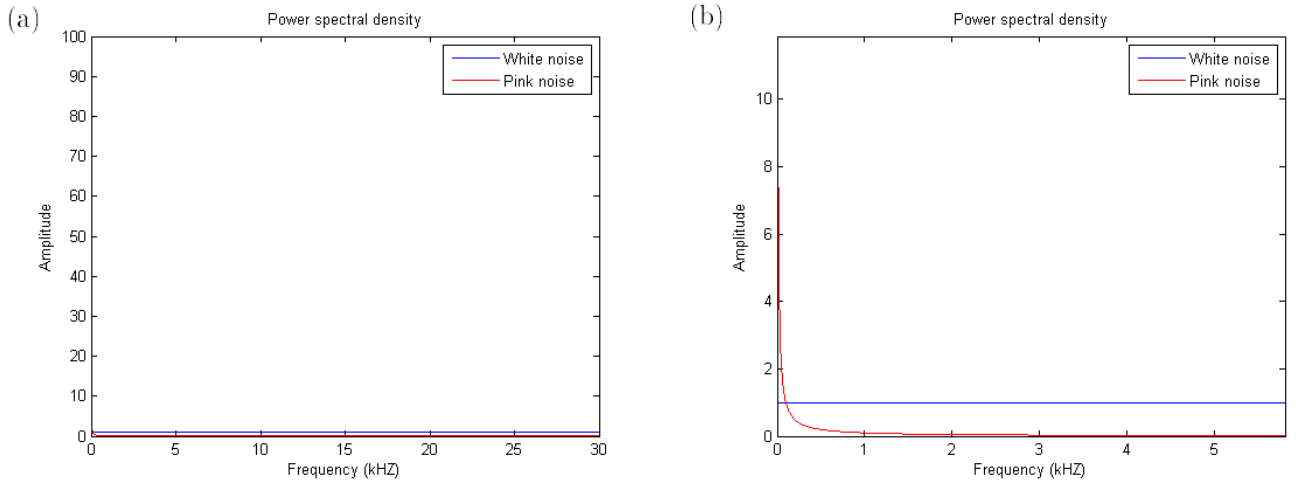


Figure 3.1: Graph of the power spectral density of a white noise and a pink noise with a zoom for (b)

3.4 Electronic components

The different components of a neural recording implant were described in section 1.2 and are reminded on picture 3.2. For our particular design, we need:

- Eight low-noise amplifiers to amplify the eight signals of interest and limit the noise effects;
- An ADC to convert the amplified signal;
- A digital-to-analog converter (DAC) to handle the active offset compensation.

We made the choice to make an active offset compensation rather than a traditional high-pass filter (a resistor and a capacitor). Indeed, this system would have a very high time constant τ and would damage our measures. The low cut-off frequency should be below $10Hz$ for LFPs recording and corresponds to $\frac{1}{2\pi\tau}$. From this formula, we immediately deduce that $\tau = \frac{1}{2\pi f_c}$ and equals around $16ms$ for the desired cut-off frequency. In comparison with the dynamic of the observed phenomenon, it is absolutely too high to be acceptable.

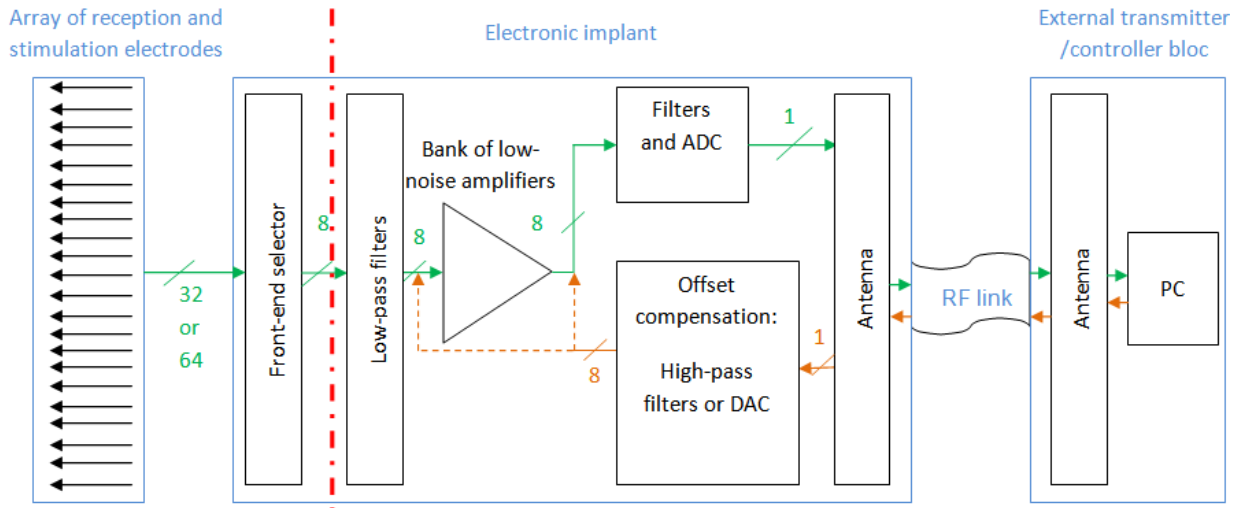


Figure 3.2: Schematic representing the different components of a neural implant for neural recording. In green is represented the flow chart for the signal we get from the electrodes, and in orange, the flow chart for the signal we get from the controller block. The red dotted line makes a separation with, on the right, the part concerning our project.

3.4.1 High level design

We carried out a first study with the basic components we knew were necessary (see precedent section 3.4). This study is done at a very high level and is carried out in order to decide which components meet the validity criteria imposed previously.

Schematic: high level view

A very first design was carried out with the following components:

- Two AD8334: each AD8334 is a quad-channel, ultra low-noise amplifier with variable gain. This device is responsible for amplifying the signals of interest and limiting noise amplification;
- One AD7856: the AD7856 is a 14-bit, 8-channels ADC that operates from a single 5V power supply. This part of the circuit makes the actual analog to digital conversion of the amplified signals;
- One AD5392: the AD5392 is a complete single-supply, 8-channel, 14-bit DAC. This DAC is used in order to compensate for the offset;
- An offset compensation switch to be able to determine what is the best place for the offset compensation (before or after the bank of amplifiers);

- Digital connections to a computer to process the digital data.

The different components and the interconnections are shown on figure C.1 in appendix C.

3.4.2 Parameter exploration

We did a first parameter exploration to decide whether our component choice was justified or not and whether the validity criteria could be reached. The different graphs needed for this purpose are: a representation of the noise varying with the input signal and the input offset, a representation of the corresponding gain and offset compensation voltage. To simplify the analysis and to spare computational time, only the graphs for the positive values of the input signal and the input offset are represented. By symmetry, the graphs for negative values of the two inputs can be established. There is no use to compute the case where only one input has a positive value because the SNR will always be higher than in the two extreme cases: if the signal input is positive while the offset input is negative, the possible amplification is bigger and thus the SNR achieves better results. This very same phenomenon happens if the signal input is negative and the offset input positive.

The first step in this part of the study is to draw up a table of all the static and dynamic parameters. The different parameters are classed according to their dynamic or static nature and to their belonging to a specific component class. This table is shown on figure 3.3.

The exploration is carried out by varying the dynamic parameters. The sampling frequency is chosen at $30kHz$ as discussed in section 3.1. Therefore, only gain and location for offset compensation are modifiable. The evaluation of each possible case is performed thanks to the MATLAB[®] software. The two cases of offset compensation were done in different files. In each file, the gain was determined in order to maximize the SNR while remaining in the linear domain. The MATLAB[®] script is composed of four different functions:

1. $[n1, n2, n3, n4] = noise()$: this script outputs the different noise levels introduced by the different steps in the circuit. This script and the noise computation are addressed in greater detail further.
2. $[Nout, Oout, Sout, sat] = transfertfonctions(gain, Sin, Oin)$: this script computes for a given gain, input signal and input offset amplitude, the output noise, offset, and signal amplitudes as well as whether there is saturation or not.
3. $[g, SNmax] = optimum(Sin, Oin)$: this script computes the optimal gain in the possible gain range and the corresponding *snr* for given input signal and offset amplitudes. The optimum is the gain value for which there is no saturation and for which the *snr* is maximum.

	Amplifiers		ADC	Offset compensation		
Static parameters	VCM Bias LNA	pin LMD tied to ground to center the output common-mode	Reference Input/Output	pin REFIN/REFOUT set to explore the entire digital	Reference Input/Output	pin REFOUT/REFIN set to 2.5V
	Gain Select for Postamp	pin HILO tied to a logic high or low for a gain select	Master clock signal for the device	pin CLKIN sets the conversion and calibration times	Analog supply pins	pins AVDD set to 5V to obtain a maximum offset
	Gain Control Slope	pin MODE tied to a logic low to have a positive gain control slope				
Dynamic parameters	Gain Voltage Control	VGAIN (between 40mV and 1.0V) controls the gain with a positive 50dB/V slope	Serial Port Clock	the user must provide a serial clock on this input	Interface Clock Input Pin	the user must provide a serial clock on this input
					Asynchronous Clear Input Switch	pin to stop the offset compensation choose the place to realize the offset compensation

Figure 3.3: Table representing the static and dynamic parameters. The parameter exploration is carried out by varying the dynamic parameters.

4. *graph_lowerlimit()*: this function explores the entire input signal and offset range and calls the *optimum* function to represent a graph of the optimum gain, *snr*, and amplitude of the offset compensation voltage. In black, on the graph representing the maximum *snr* obtained for given input signal and offset amplitudes, the lower limit of 0.5 is highlighted.

Noise determination This part of the exploration makes up the fundamental computation². For this parameter exploration, four sources of noise are considered:

1. **Intrinsic noise of the input signal**: the snr_{max} is given and is of 0.5. This means that, in the worst case (the smallest input signal), we have an *snr* of 0.5. Thus the

²For any practical computation, see appendix A.

worst root mean square voltage noise is given by:

$$\begin{aligned} snr &= \frac{v_{rms,signal}}{v_{rms,noise}} \\ &= 0.5 \end{aligned} \quad (3.2)$$

$$\begin{aligned} v_{rms,signal} &= \frac{V_0}{\sqrt{3}} \\ &= \frac{20\mu V}{\sqrt{3}} \\ &= 0.0115mV \end{aligned} \quad (3.3)$$

$$\begin{aligned} v_{rms,noise1} &= 2 * v_{rms,signal} \\ &= 0.0230mV \end{aligned} \quad (3.4)$$

2. **Noise of the low-noise amplifier:** from the data sheet, we know that the input voltage noise³ for 14dB gain is $0.8nV/\sqrt{Hz}$. From equation A.9, we have:

$$\begin{aligned} v_{rms,noise2} &= 0.8\sqrt{f_{max} - f_{min}} \\ &= 0.8\sqrt{100kHz - 0} \\ &= 253nV \\ &= 0.0002mV \end{aligned} \quad (3.5)$$

3. **Noise of the ADC:** the data sheet gives us the information that the positive full-scale error is of $\pm 3LSB$. We know that the maximum output voltage reaches 5V. Thus $1LSB = \frac{5V}{2^{14}} = 0.3052mV$ and $v_{rms,noise3} = 3 * 1LSB = 0.9155mV$.

4. **Noise of the DAC:** in the data sheet, we find that the output voltage is $100nV/\sqrt{Hz}$. Thanks to the same computation as for equation 3.5, we get $v_{rms,noise4} = 0.0316mV$.

The actual noise computation depends whether the offset compensation is made before the bank of amplifiers or not. Indeed, either the offset compensation is executed before the amplification stage and the DAC noise is amplified or the offset compensation is executed after the amplification stage and the DAC noise suffers no amplification. In the first case, we get (using theorem 2):

$$v_{rms,signal}^{out} = \sqrt{G^2(v_{rms,noise1}^2 + v_{rms,noise2}^2 + v_{rms,noise4}^2) + v_{rms,noise3}^2} \quad (3.6)$$

³We consider the input voltage noise because the source resistance is negligible compared to the input resistance of the amplifier (see theorem 3).

In the second case, we get (using theorem 2):

$$v_{rms,signal}^{out} = \sqrt{G^2(v_{rms,noise1}^2 + v_{rms,noise2}^2) + v_{rms,noise3}^2 + v_{rms,noise4}^2} \quad (3.7)$$

The final *snr* is computed, using equations A.7 and A.11, for each possible input value:

$$snr = \frac{\frac{G*inputvoltage}{\sqrt{3}}}{v_{rms,signal}^{out}} \quad (3.8)$$

3.5 Determination of the offset compensation

As stated before, the parameter exploration is carried out for an input signal ranging from $20\mu V$ to $100mV$ and an input offset ranging from $0mV$ to $300mV$. The possible gains are deduced from the AD8334 data sheet specifications:

$$GAIN(dB) = 50(dB/V) * V_{GAIN} - 6.5dB, (HILO = LO) \quad (3.9)$$

$$GAIN(dB) = 50(dB/V) * V_{GAIN} + 5.5dB, (HILO = HI) \quad (3.10)$$

Knowing that the gain control range is $40mV$ to $1V$, we get a minimum gain of 0.60 and a maximum of 595.66. We choose a variation step for the gain of one except if the optimal gain is smaller than 10. In this case, it is reevaluated with a variation step of 0.1. If the result is smaller than the integer, it is again reevaluated with a variation step of 0.01.

The clamping effect brought by the amplifier is taken into account by limiting the amplifier output to $2V$ because the clamping effect restrains the output for the entire input range in $0.5V$ to $4.5V$. However, we only compute the output for the positive inputs. We are thus restricted in the $[2.5V; 4.5V]$ region. This means that the maximum offset compensation voltage is also $2V$ which can be easily delivered by the DAC.

We have two very different cases to consider:

1. Low-noise configuration;
2. High dynamic range configuration.

For the first configuration, the offset compensation is made after the amplification in order to avoid amplifying the DAC noise. The problem, in this case, is that the offset is amplified without any previous compensation. Given the amplitude ratio between the signal of interest and the offset, this could lead to a very significant offset at the amplifier's output. We do not have the possibility to amplify the input signal by a significant gain because of this offset and the saturation limit of the amplifier. The second case consists of the other

way around: the offset is first compensated, and then, the signal is amplified. The signal is thus noisier but the amplification of the signal of interest can attain a higher level because it is not limited by the offset amplification.

Results for the two considered cases are shown on figure 3.4. As expected, we get in the left column (low-noise configuration) a better *snr* with a smaller gain, and in the right column, we get a smaller *snr* with bigger gains (this is especially noticeable in the case of small signals of interest). On the right, the gain remains constant for a given input signal because it is not influenced by the offset which has already been removed. In this same column, the offset compensation voltage is linear for the reason that this offset undergoes no processing before compensation. What is important to notice is the fact that the amplification of the offset is not to the detriment of the *snr*. This important aspect was the one we wanted to verify by the first step of our study.

Our choice of configuration leans toward the low-noise configuration. To be sure about this preference, we still need to check that in the critical region, this configuration gives really better results than the high dynamic range one. The critical region is the one with very low input signal but high offset. This region, for the two possible configuration, is given in figure 3.5. In black is represented the lower limit admissible for the *snr* (i.e. 0.5). We immediately see from those graphs that the low-noise configuration is the more appropriate one for this region as well. When the compensation is carried out before the rest of the processing, the noise is constant for the entire range of offset because the gain is constant itself as explained before. What we also notice is that the worst case happens for a very weak signal and a large offset. Indeed, with those parameters, the amplification of the total input can not reach a high enough level to favor the signal of interest over the noise. The clamping effect prevents the system from producing an acceptable result.

3.6 Definitive components

As discussed in the previous section, our choice of configuration settled down on the low-noise configuration. The major problem at present consists of the fact that the first low-noise amplifier has an input voltage range of $\pm 275mV$. However, without offset compensation, the total input range should range from $-400mV$ ($-100mV - 300mV$) to $+400mV$ ($+100mV + 300mV$). The low-noise amplifier AD604 meets those specifications; it is an ultra low-noise, very accurate, dual-channel, linear-in-dB variable gain amplifier. Its input-referred noise voltage reaches $0.8nV/\sqrt{Hz}$ which allows us to achieve the same level of accuracy as with our previous amplifier. A new schematic was created with the change of amplifier plus a new component responsible for the summation of the amplified signals and the offset compensation voltage. This offset compensation voltage is generated either positive or negative for the specific case and thus we only need one additional component

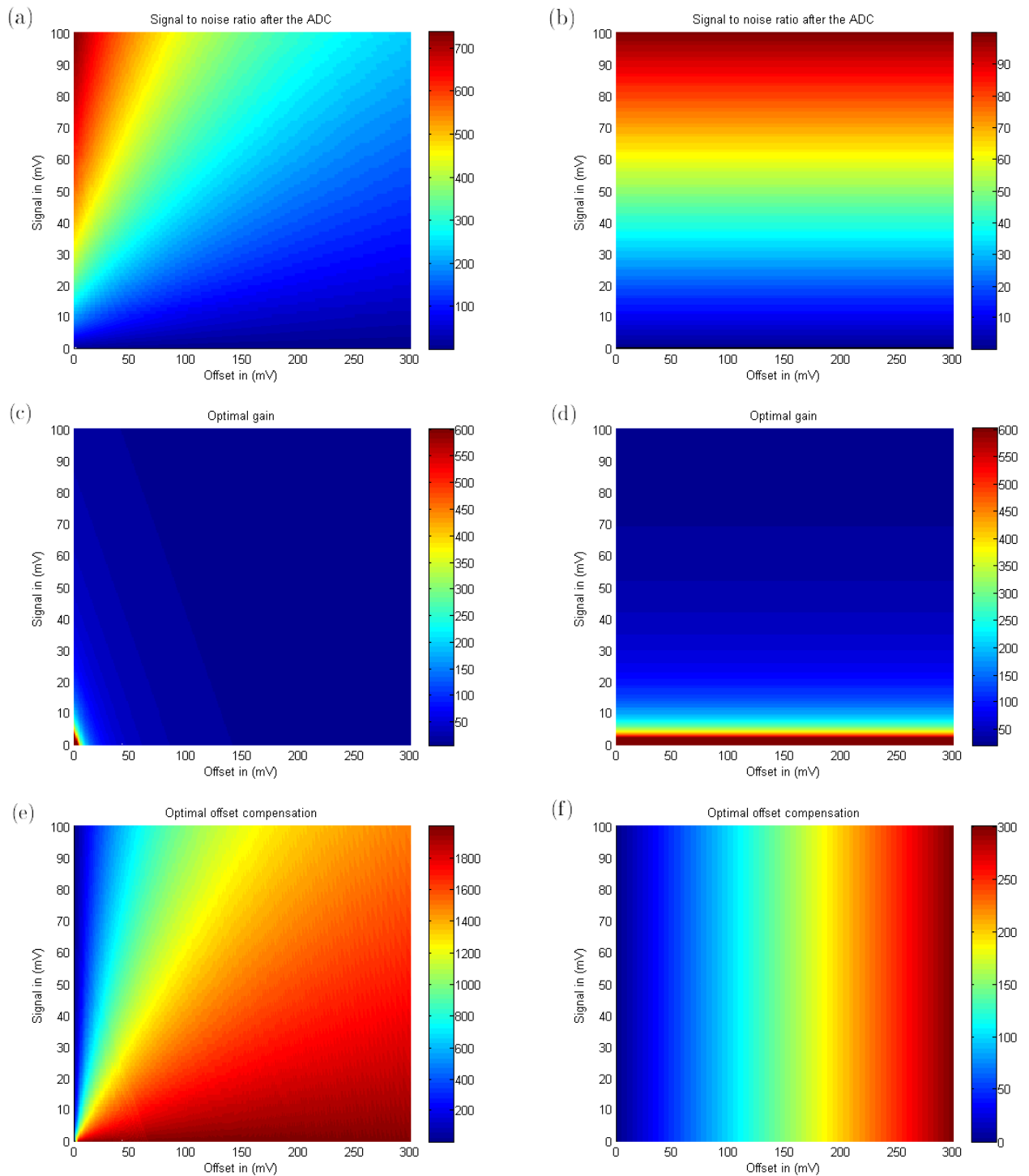


Figure 3.4: Results of the parameter exploration. Each column corresponds to one case with the low-noise on the left and the high dynamic range on the right. (a) et (b) show the snr , (c) and (d) the gain in absolute value, (e) and (f) the offset compensation voltage in mV .

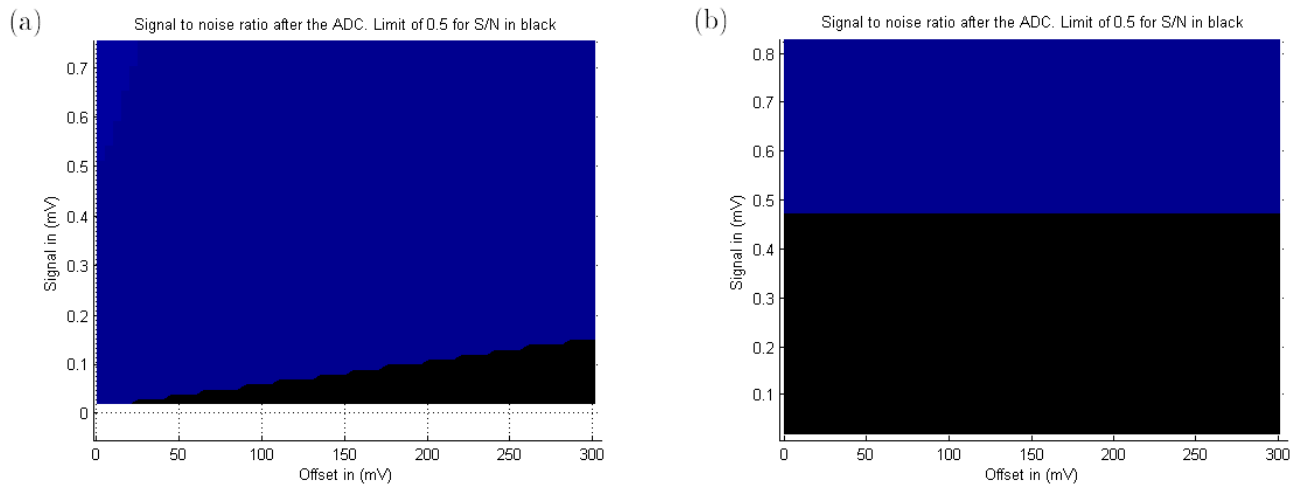


Figure 3.5: Zoom to the region of interest for the two considered cases. (a) is for the low-noise configuration and (b) for the high dynamic range configuration.

to fulfill the summing function. A simple summing amplifier setting was made with an operational amplifier (LM324). The new schematic is shown on figure C.2 in appendix C and the summing amplifier setting on figure 3.6.

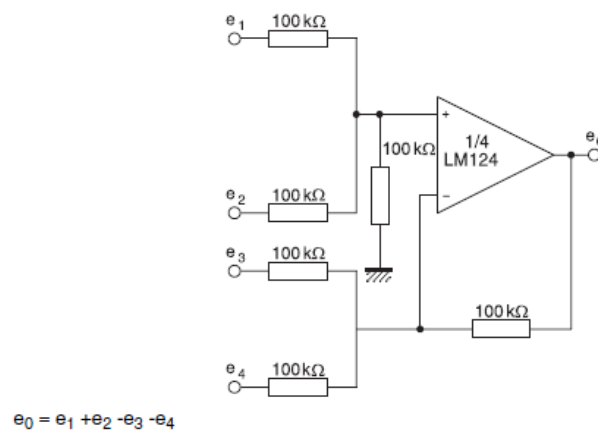


Figure 3.6: Summing amplifier setting from the LM324 data sheet.

The next step was again to draw up a table with the new static and dynamic parameters. Most of them remain the same as in table on figure 3.3 but parameters concerning the amplifier are completely new. For this reason, only this column is represented on figure

3.7. From this table, a new parameter exploration is performed.

		Amplifiers
Static parameters	Preamplifier	pin shorted to the corresponding
	Feedback Input	PAO to have 14dB gain for the preamplifier and a peak input voltage of +400mV
	VREF	input to this pin sets gain scaling for both channels. Tied to 2.5V => 20dB/V
	VOMC	input to this pin defines the common mode of the output at OUT1 and OUT2. Connect to ground by a capacitor to have half the supply voltage
Dynamic parameters	Gain Control Input and Power-down Pin	VGN(between 0.25V and 2.65V)controls the gain according to the slope set by gain scaling(20dB/V)

Figure 3.7: Table representing the static and dynamic parameters for the new amplifier.

This time, we have to take into account the noise introduced by the operational amplifier LM324. From the data sheet, we get the information that the input voltage noise is $40nV/\sqrt{Hz}$. For the same frequency bandwidth as before, and using the same procedure as for equation 3.5, we get:

$$\begin{aligned}
 v_{rms,noise5} &= 40\sqrt{f_{max} - f_{min}} \\
 &= 40\sqrt{100kHz - 0} \\
 &= 12649nV \\
 &= 0.0126mV
 \end{aligned}
 \tag{3.11}$$

3.7 Parameter exploration

3.7.1 Optimum parameters

We execute the exact same functions as in section 3.4.2 with the MATLAB[©] software, except here, the noise functions possess five output arguments and the noise determination

corresponds to the following equation:

$$v_{rms,signal}^{out} = \sqrt{G^2(v_{rms,noise1}^2 + v_{rms,noise2}^2) + v_{rms,noise3}^2 + v_{rms,noise4}^2 + v_{rms,noise5}^2} \quad (3.12)$$

The variation range for the gain is brand new and is determined in the following way:

$$GAIN(dB) = gainscaling(dB/V) * VGN(V) + (PreampGain - 19)(dB) \quad (3.13)$$

$$= 20(dB/V) * VGN(V) - 5dB \quad (3.14)$$

with VGN ranging from $0.25V$ to $2.65V$. Thus the maximum gain is 251.1886 and the lowest one 1 in absolute value. Moreover, the clamping effect is less present than before and the amplifier output is limited to $+2.5V$.

The scripts for the different functions are joined to this work in the attached CD-ROM. The results are shown on figure 3.8 with a zoom on the critical region. The “wave” compartment noticeable especially for the offset compensation is due to a lack of accuracy in the input offset, input signal, and gain. Indeed, if we had a continuous variation for all these variables, we would have, for a given input signal of interest, a linear reduction of the gain with an augmentation of the input offset. The same phenomenon would happen for a given offset and increasing input signal. The lack of accuracy is not a problem to conclude that, for most of the inputs, the system behaves well enough. This accuracy is critical in the region with low input signal of interest and high DC offset. In this region however, the gain resolution is of 0.01.

From graph (d), we know that an input signal with amplitude higher than $90\mu V$ is processed with an acceptable snr . For smaller signals, it depends on the amplitude of the offset. In this analysis, we considered the worst cases possible. For example, the ADC noise is not very precisely stated in the data sheet. An error of $\pm 1/2LSB$ is more common for this type of component and the results for this consideration are more acceptable as shown on figure 3.8(e). Signal inputs higher than $30\mu V$ are processed effectively.

3.7.2 Limitations

Another parameter exploration is performed to determine whether it is possible or not to limit resources of the different components. This consideration comes from the fact that an snr of 10 is a sufficient value for our purpose. Indeed, if our circuit reaches such results, it means that, after processing and using equation A.6, we get a signal power one hundred times bigger than the noise power:

$$SNR = \frac{P_{signal}}{P_{noise}} = 100 \quad (3.15)$$

$$\Rightarrow P_{signal} = 100P_{noise} \quad (3.16)$$

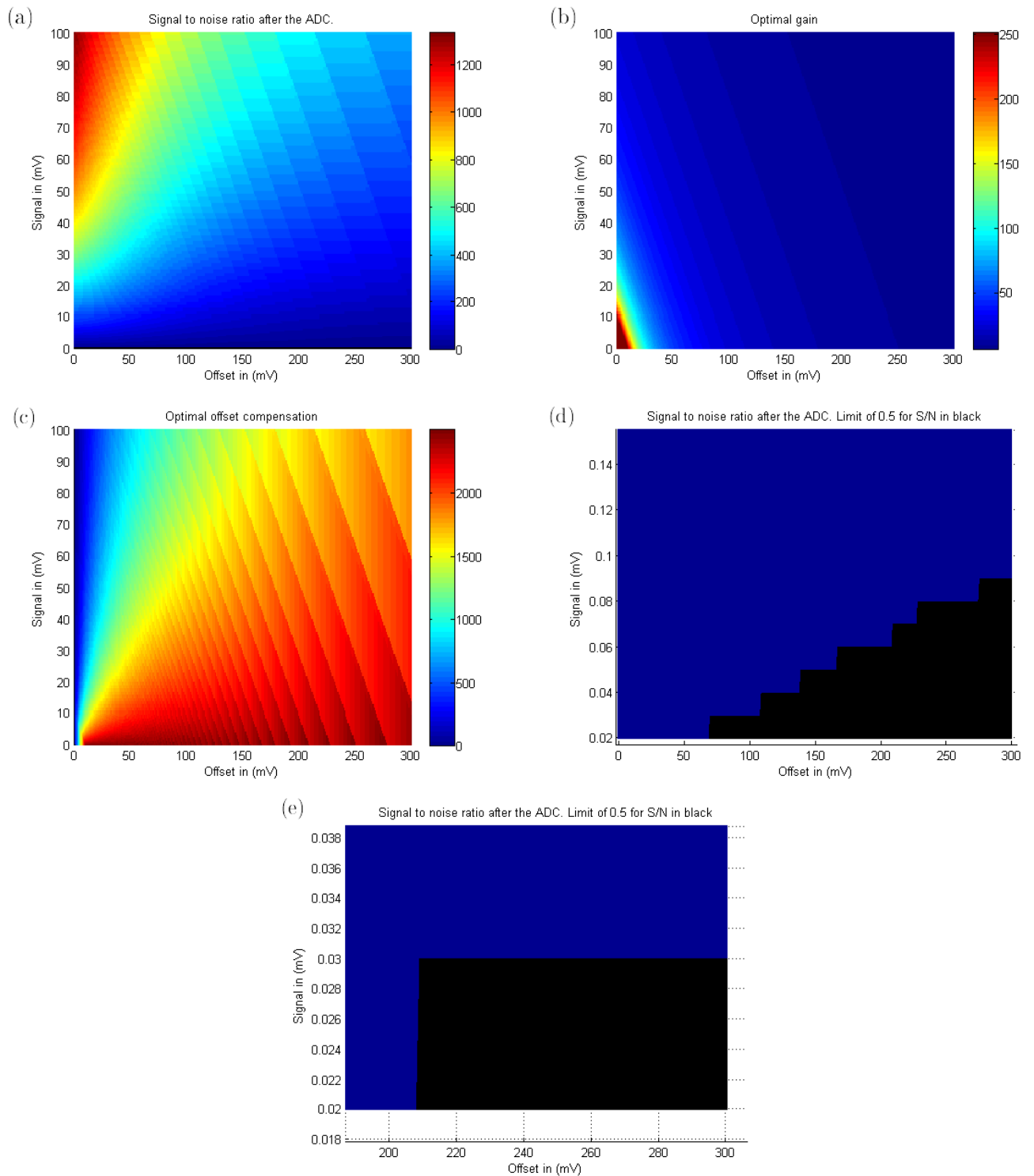


Figure 3.8: Results of the parameter exploration. (a) the *snr*, (b) the gain, (c) the offset compensation voltage and (d) a zoom on the critical region. (e) for an error of $\pm 1/2LSB$ considered for the ADC.

or expressed in root mean square:

$$SNR = \frac{v_{rms,signal}^2}{v_{rms,noise}^2} = 100 \quad (3.17)$$

$$\Rightarrow v_{rms,signal} = 10v_{rms,noise} \quad (3.18)$$

This ratio is sufficient to detect correctly the signal of interest and might be achieved with a smaller gain and thus smaller offset compensation voltage. The script for the analysis is very similar to the one for the optimum parameters except the *optimum* script is replaced by the function $[g, SNmax] = optimum_limit_ressources(Sin, Oin)$ which computes the *snr* for variable inputs but when the *snr* is higher than 10, it returns to the previous *snr* computed, i.e. the one closest to 10 but strictly lower. Due to the discretization of the parameters, this level might be already archived for the very first variable combination. In this case, the closest *snr* to 10 is chosen but it is then slightly above the threshold. The script is also available on the CD-ROM. The graphical results are provided on figure 3.9.

From these graphs, we see that the *snr* is actually limited to 10. Once again, the discretization of the input arguments leads to graphs with horizontal levels instead of a continuous variation. For the problematic region (small input signal amplitude and large offset), we get the exact same result as in the previous section. The gain varies still in its entire range but most of the gain is below the level of 50. If we look into more details, we notice that the gain takes high value for very small input signal and offset. In this same region, the *snr* attains acceptable values. We tried to limit the gain to an absolute value of 100 and got the result on figure 3.10. We can deduce from this observation that the gain does not need to vary up to 251.1886 but resources can be limited to maximum a value for the gain of 100.

From the offset compensation graphs, we observe that the offset compensation voltage reaches high value only for input arguments in the critical region. This means that no resources can be subtracted at this level otherwise we would not be able to detect the neural spikes anymore.

Eventually, we know that the only limitation in resources which can be performed is a limitation in gain. This actually does not save much of power supply or other resources but we could envisage to use an amplifier with lower range gain values. However, very low-noise amplifiers are not legion and we decided to keep the AD604.

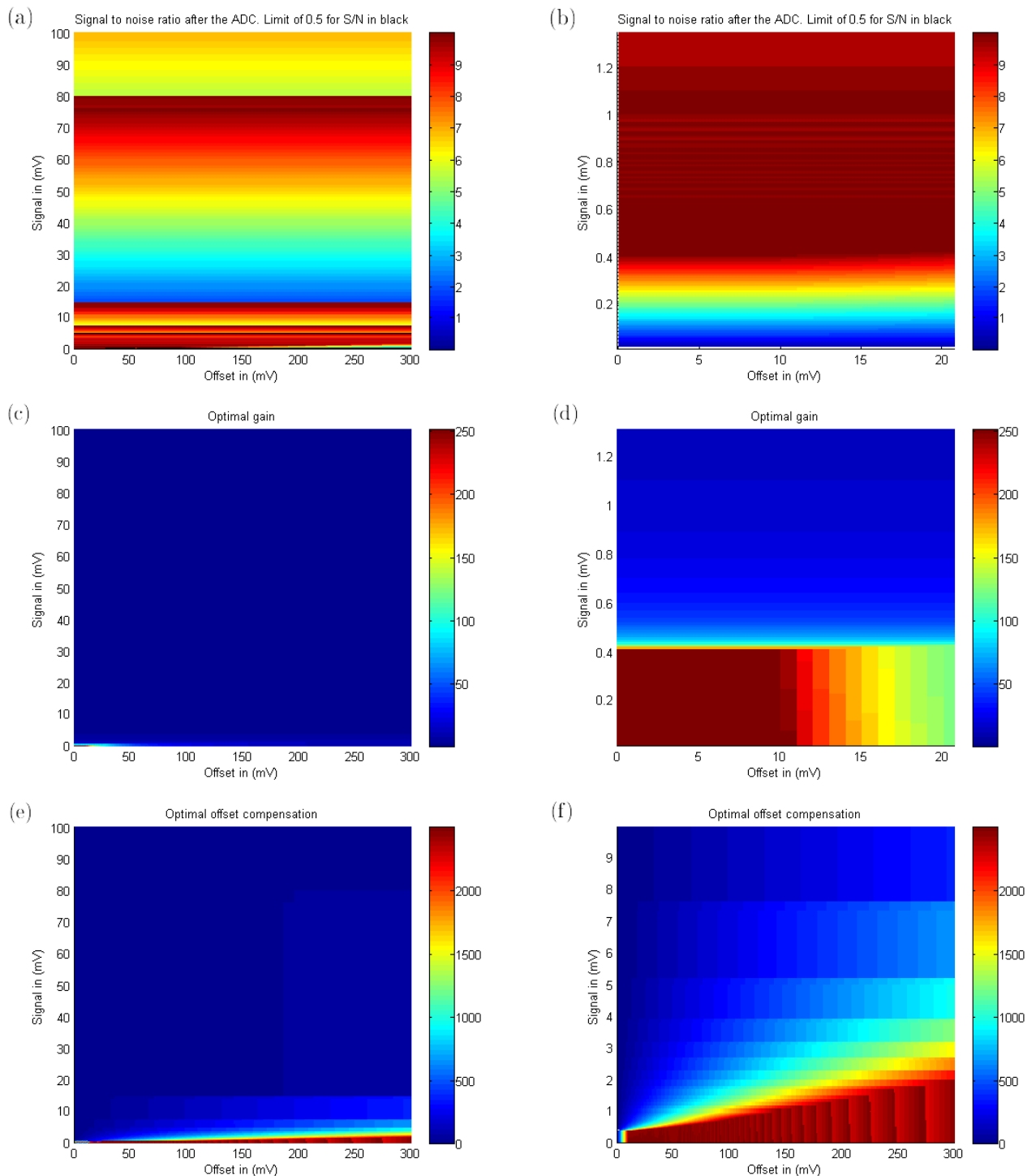


Figure 3.9: Results of the parameter exploration with resource limitation. In the left column are the global results and in the right column a zoom to a particular region of interest. (a) and (b) represent the snr , (c) and (d) represent the gain, (e) and (f) represent the offset compensation voltage in mV .

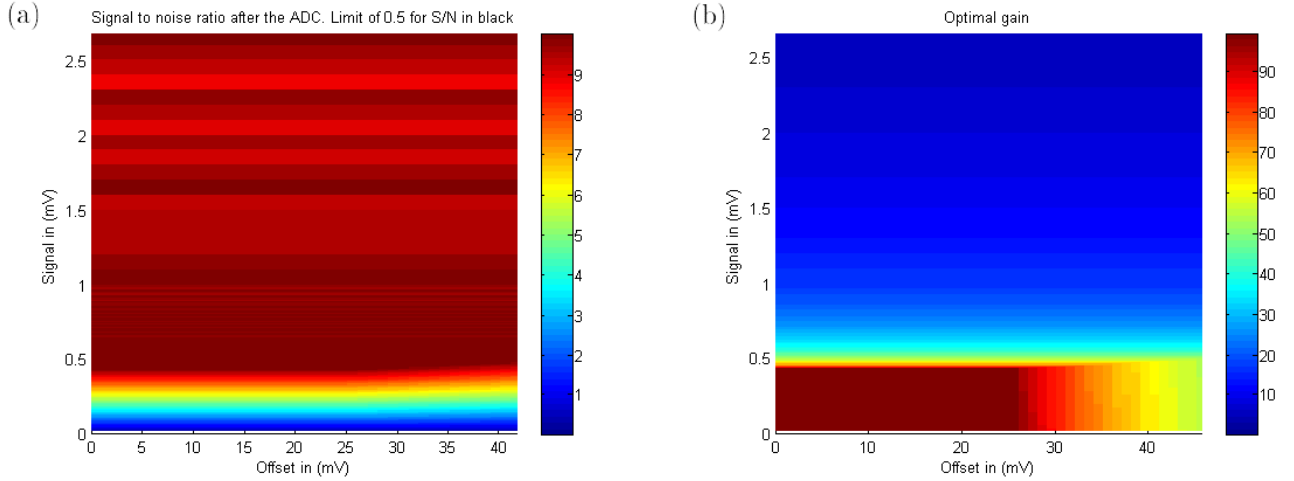


Figure 3.10: Results of the parameter exploration with gain limited at 100. Zoom to the problematic region for (a) the *snr* and (b) the gain.

3.7.3 Algorithm

The last part in this chapter is the design of an algorithm able to deduce the optimal gain and offset compensation voltage from digital data. This algorithm will be implemented on the computer responsible for detecting neural pikes. This algorithm is composed of two MATLAB[®] functions: $[V_{out}, N_{out}] = \text{computation}(S_{in}, O_{in}, \text{gain}, \text{offsetc}, p)$ and $[\text{gain}, \text{offsetc}, V_{out}] = \text{algorithm}(O_{in}, p)$ which scripts are to be found in the attached CD-ROM. The purpose of each function is detailed here after:

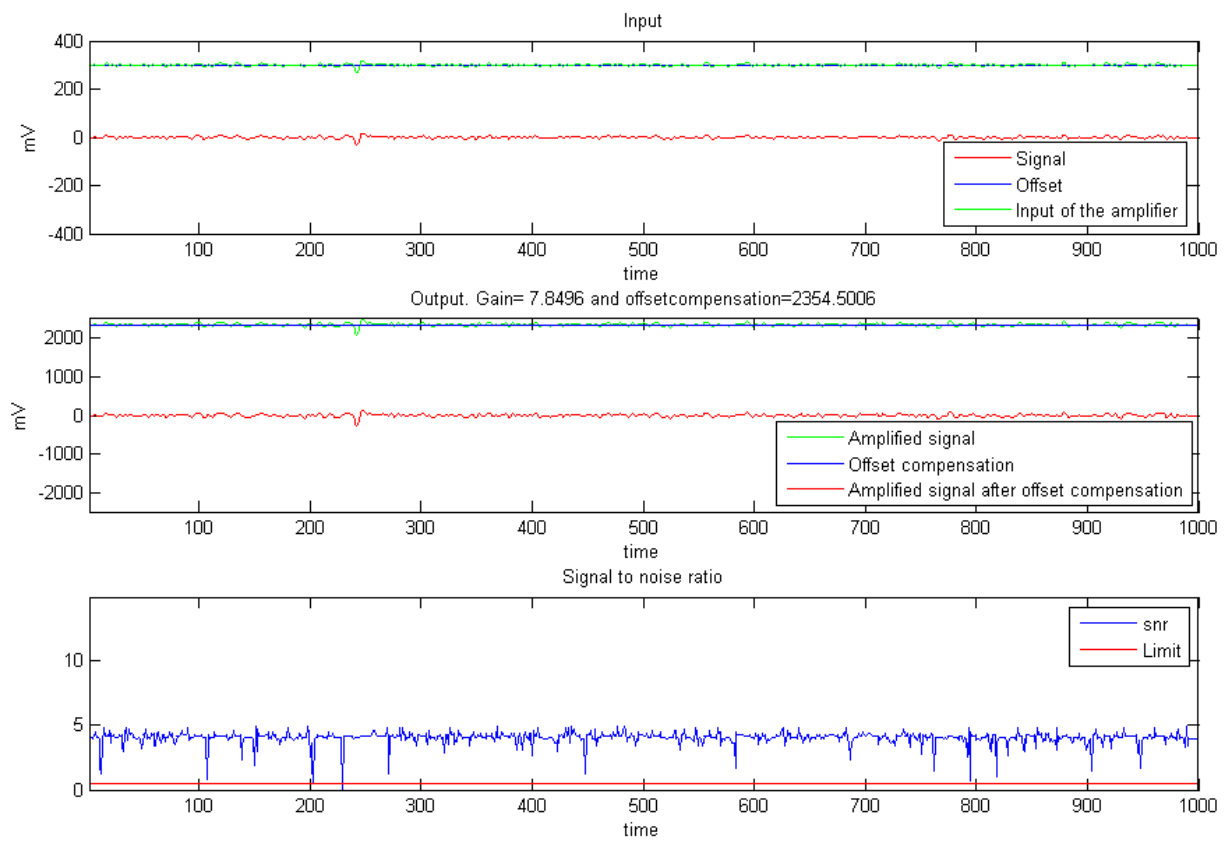
- *computation*: this function computes the outputs of the processing chain, i.e. the digital input signal and the digital input noise and thus the digital data available. This signal is the summation of the signal of interest and the offset multiplied by the gain. The DC offset can be added or subtracted depending on the value of the parameter p to include all the possible cases. Afterwards, the signal is limited to $\pm 2.5V$ because of the amplifier saturation. The computed offset compensation voltage is then withdrawn. The output noise is computed as given in equation 3.12.
- *algorithm*: this function determines the optimum gain and offset compensation voltage for a digital input. Three different graphs are produced:
 1. the inputs of the processing chain (signal of interest, offset, and summation of the two);
 2. the output of the low-noise amplifier and the signal after offset compensation as well as the offset compensation voltage;

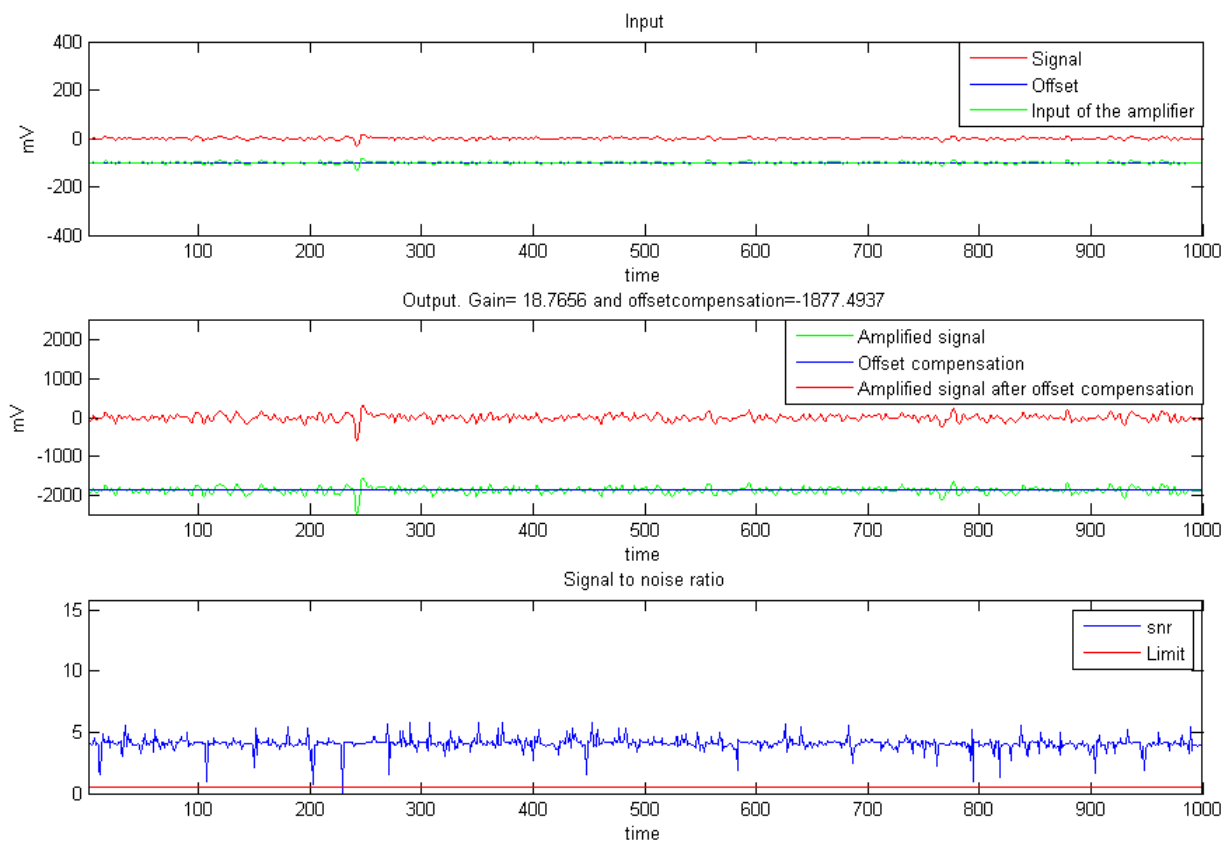
3. the *snr* plus the limit of 0.5.

At the beginning, the gain is maximum (gain=251.1886) and the offset compensation voltage minimum (null). The first step is to reduce the gain until the maximum amplifier output is smaller than $2.5V$ and the minimum is bigger than $-2.5V$ (the saturation limits). This reduction is executed by dividing the gain at each step by a factor 2. To gain in accuracy, the gain is afterwards augmented while remaining in the non saturation domain by the formula $gain = gain + gain/2^l$, l increasing at each loop. The increase stops when the amplifier output reaches $\pm 2.48V$ (chosen arbitrarily but is different from $\pm 2.5V$ to avoid being too close of the saturation region). Then the offset compensation voltage is computed thanks to the signal's *mean* and *standard deviation*. The idea is to restrict the values at each loop to the interval $[Mean - Standarddeviation, Mean + Standarddeviation]$ and to recompute the new *mean* and *standard deviation*. When all the values are in the interval, the mean corresponds to the offset compensation voltage provided it is in the offset compensation range, i.e. $[-2.5V, 2.5V]$. With the computed *gain* and *offset compensation* parameters, the output is deduced and we check whether each value is in the non saturation interval or not. If it is not the case, then the offset compensation voltage is recomputed by withdrawing the excess. After this step, the *snr* is computed (the noise considered is the real noise and the offset which has not be compensated).

The results for different offsets are given in the present report in figures 3.11 and 3.12. In the first case, we have a $300mV$ positive DC offset. The optimum gain we get is 7.8496. The offset compensation voltage should thus reach $7.8496 * 300 = 2354.9mV$ instead of $2354.5mV$ which means a very weak error of 0.017%. In the second case ($100mV$ negative DC offset), the gain is 18.7656 and the offset compensation voltage is $-1877.5mV$ instead of $18.7656 * -100 = -1876.6mV$ which leads to an 0.0479% error. Our algorithm seems very efficient and, in both cases, only one digital value gives an *snr* lower than 0.5. When we check, we notice that this poor result is obtained with an input signal of $0mV$, a value effectively below our domain of interest and obviously leading to an *snr* of 0.

From all these analyses, we see that the offset compensation does not need to be carried out in the analog circuit. In order to spare space on the PCB, the offset compensation can be handle digitally. To be able to check this conclusion but simply our circuit, we keep the summing circuit in our design but we won't use a DAC to create the offset compensation voltage (it will be directly generated as an analog signal).

Figure 3.11: Graphs for a 300mV positive DC offset.

Figure 3.12: Graphs for a 100mV negative DC offset.

Chapter 4

Hardware design: printed circuit board design

In the previous chapter, we made our decision concerning the major components' choice and analyzed the region in which they could give satisfactory results. To those components, we must add a power supply management circuit, analog and digital connectors plus an RF component for wireless data transmission from and to the PC. The RF link is provided by the "eZ430-RF2500 Development Tool", whose functions and utilization will be described in details later in section 4.3. First of all, we describe the overall concept and the refinement of the schematic. Then, each subcircuit is described independently with its specific functions and organization. In a second part, the actual PCB is detailed and particularly the important aspects such as components placement, analog connections, signal path, and analog to digital separation.

4.1 Schematics

Our PCB is based on the high level schematic of section 3.6. However, as explained in the previous chapter, our parameter analysis allows us to let go the active offset compensation. To be able to refute or verify this conclusion, we keep the summing amplifier setting with the LM324 but we won't use a DAC to produce the offset compensation voltage which will be produced directly analogically. We still need a DAC to produce the voltage gain, i.e. the voltage necessary to control the gain of the amplifiers.

Our schematic is shown on figure C.3 in appendix C. We first have the analog connector, then the bank of low-noise amplifiers before the operational amplifiers for summing purposes. Signals coming out the summing circuit are sent to the ADC. The DAC is connected to the low-noise amplifiers as it controls the gains. We also have a component

responsible for the connection between components on the board and the microcontroller on the eZ430-RF2500 Development Tool, and therefore, connection to the PC via UART. The last block on our schematic is the power supply management circuit.

4.1.1 Low-noise amplifiers

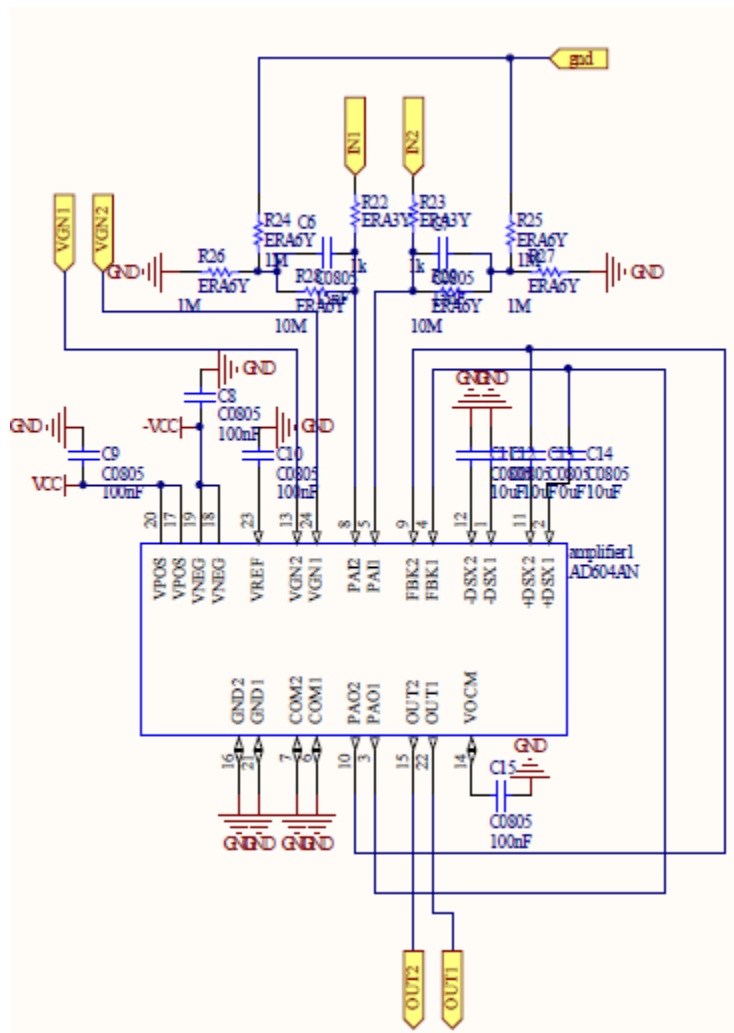


Figure 4.1: Low-noise amplifier’s connections.

The low-noise amplifier is the first active component of our circuit. The AD604 is made of two low-noise amplifiers. Provided we want to process eight different channels, we need four times two amplifiers. To avoid amplifying high frequency noise and undesirable signals, we place at their inputs a low-pass filter composed of a resistor and a capacitor. We decided

to sample at a frequency of $30kHz$ (see section 3.1) and this first low-pass filter possesses a cut-off frequency of $10kHz$ (below half the sampling frequency):

$$\tau = R.C = 1 * 10^3 \Omega * 15 * 10^{-9} F = 15.10^{-6} s \quad (4.1)$$

$$f_c = \frac{1}{2\pi\tau} = \frac{1}{2\pi * 15 * 10^{-6}} = 10.610kHz \quad (4.2)$$

In addition, the $1k\Omega$ resistor plays the role of ESD caution resistor. In parallel with the capacitor, we place a high value resistor in order to dissipate the power possibly stored in the capacitor. This resistor needs to be of very high value respectively to the ESD caution resistor (at least a factor 100) to avoid a significant potentiometric division which would degrade our signal. In our case, we choose to use a $10M\Omega$ resistor leading to the potentiometric factor:

$$\frac{10M}{10M + 1k} = \frac{1}{1 + 10^{-4}} \approx 1 - 10^{-4} \approx 1 \quad (4.3)$$

We use a single-ended input amplifier and not a differential one. This prevents us from taking into account any change in the reference electrode and thus in the background of the region of interest. Moreover, we are more susceptible to coupling-noise and DC offsets. To compensate for these disadvantages, we use an “external ground” signal. Furthermore, this helps in limiting capacitive coupling as discussed in section 4.1.6. A maximum noise rejection would be achieved with fully-differential inputs [19]. Therefore, we construct “pseudo-differential” inputs: *Pseudo-differential inputs are similar to fully-differential inputs in that they separate signal ground from the ADC ground, allowing DC common-mode voltages to be canceled (unlike single-ended inputs). However, unlike fully-differential inputs, they have little effect on dynamic common-mode noise* [19]. Thanks to this method, we amplify the DC common-mode voltage rejection but not the AC one.

The user can choose which configuration he or she wants. If the single-ended input configuration is adequate, the capacitor and resistor are tied to the analog ground, the same one as the one for the ADC. In the case of high DC common-mode voltage or high DC offset, the pseudo-differential mode is preferred and the two components are tied to the external ground signal. The two possibilities are shown on figure 4.2.

Because we can process every input ranging in $[-400mV, 400mV]$ and we do not introduce a bias, we need two power supplies: $-5V$ for the negative supply and $+5V$ for the positive one¹. As suggested in the data sheet, both power supplies are decoupled with a $100nF$ capacitor to stabilize the entries. The gain of each channel is controlled by the *VGN* pin

¹What matters, in fact, is having 10V range available. Without any bias, the range midpoint value is the ground.

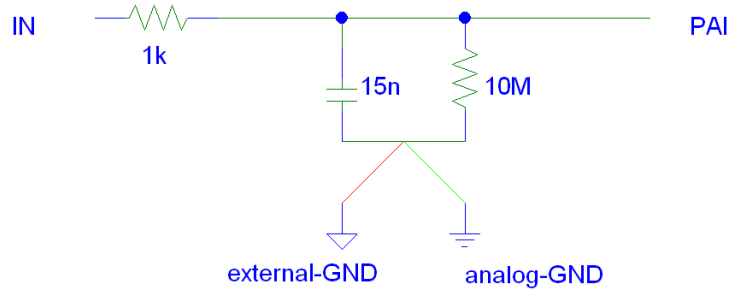


Figure 4.2: Single-ended or pseudo-differential input. For a single-ended single, the green wire is used; for the pseudo-differential one, the red wire is used.

with an analog signal produced by the DAC (section 4.1.4). $VREF$ and $VCOM$ are decoupled to ground, minimizing interchannel crosstalk. In this mode, the gain scaling and the DC level voltage are determined by the midpoint between $VPOS$ and GND which is $2.5V$ leading to a $20dB/V$ gain scaling. Outputs vary in the $[0V, 5V]$ range with a common mode voltage of $2.5V$.

After careful considerations, we realized that the AD604 is unusable without a high-pass filter. Indeed, *the DSX portion of the AD604 is a single-supply circuit and, therefore, its inputs need to be AC-coupled to accommodate ground-based signals. Two external capacitors level shift the ground referenced preamplifier output from ground to the DC value established by VOVM (AD604 data sheet).* If we try to bypass those high-pass filters, we impose a V_{bias} to the differential ladder composing the DSX portion and the output we get is completely false. The input resistor to the resistive ladder network is 175Ω . Thus, in order to obtain a cut-off frequency low enough, we need high value capacitors. For example, $10\mu F$ capacitors give the following results:

$$\tau = R.C = 175\Omega * 10 * 10^{-6}F = 175.10^{-5}s \quad (4.4)$$

$$f_c = \frac{1}{2\pi\tau} = \frac{1}{2\pi * 175 * 10^{-5}} = 90.94Hz \quad (4.5)$$

which leave most of our signal's frequency range unaffected if we consider only action potentials. For LFPs, the cut-off frequency should be lower than $10Hz$ which requires higher value capacitors and leads to a very long time constant as stated in section 3.4.

4.1.2 Summing amplifiers

For the summing amplifier circuit, the non-inverting input is the amplified signal and the inverting one, the analog offset compensation voltage. This one is either positive or negative, depending on the compensation needed and computed. Again, we need a low-pass

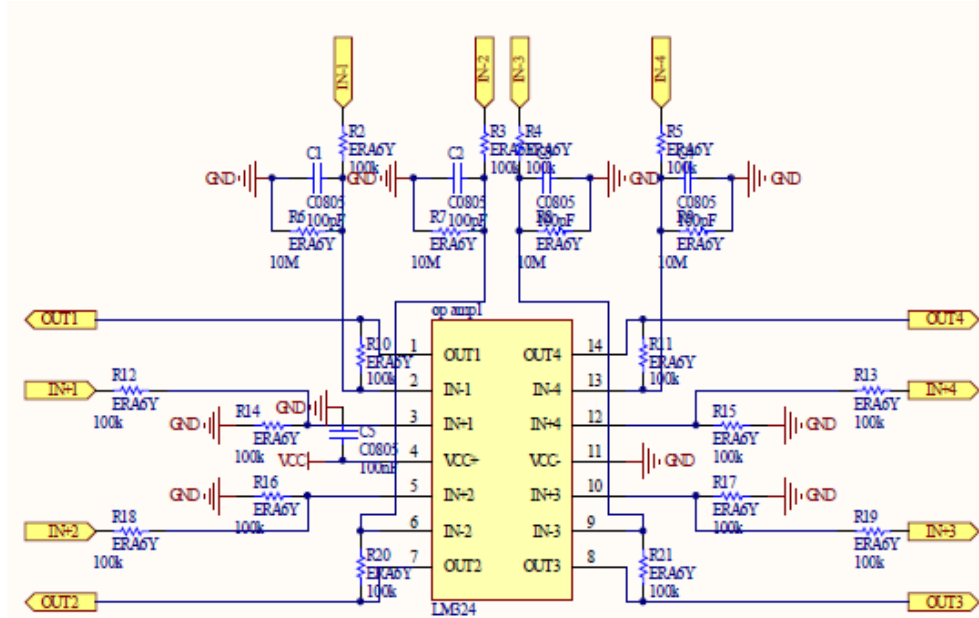


Figure 4.3: Summing amplifier's connections.

filter and ESD caution structure for the analog inputs. The signal has a DC characteristic and the cut-off frequency can be very close to zero. $10M\Omega$ resistors are used as before and lead to a $1 - 10^{-2} = 0.99$ potentiometric division factor. The ESD caution is carried out by the $100k\Omega$ resistors (we still have a factor 100). For the non-inverting inputs, no filter is needed because, being the low-noise amplifiers outputs, they have already been filtered. The $100k\Omega$ resistors are used in order to construct the summing circuit proposed on figure 3.6 adapted for the LM324. We use a single-supply made of a positive supply voltage capacitively coupled to the ground by a $100nF$ capacitor.

Because the inverting input is tied to the output in the summing amplifier structure, the cut-off frequency can not be as close to zero as expected at first. Indeed, the output is an AC signal and the inverting input's filter acts on it as well. For this reason, we chose to use a cut-off frequency of $15kHz$ thanks to $100pF$ capacitors.

4.1.3 Analog to digital converter

Once again, we need a low-pass filter in order to stabilize the analog signal prior to conversion. The cut-off frequency is chosen at $15kHz$ in order to respect Nyquist's theorem (theorem 1). This filter suppresses new noises introduced by the processing components and, furthermore, attenuates high frequency noises which have not been attenuated com-

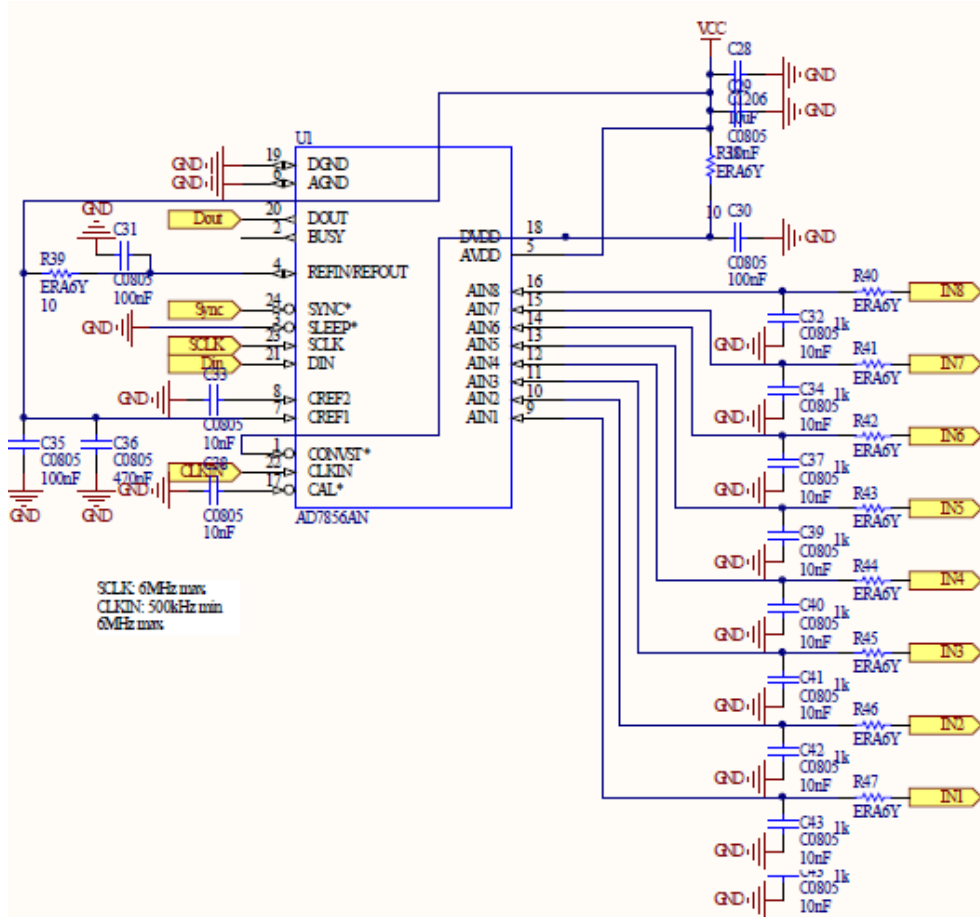


Figure 4.4: Analog to digital converter's connections.

pletely by the first low-pass filters. We can not introduce a second $10kHz$ cut-off frequency filter because it would create a second-order filter and degrade our signal in the passband at a higher degree.

We set a standard three-wire SPI interface (see section 4.1.6 for more details). The three digital inputs are $SCLK$, DIN , and \overline{SYNC} and the digital output corresponds to $DOUT$. As for each analog and digital application, the digital and analog ground are separated to avoid high currents from the digital circuit to disrupt analog components. The connection between the two is made at a single point, the closest possible to the analog part of the circuit [34]. Connections to the C_{REF1} , C_{REF2} , and REF_{IN}/REF_{OUT} pins are the ones in order to get a reference voltage as high as AV_{DD} as explained in the data sheet.

From the data sheet, we know that a conversion takes 20 or 21 $CLKIN$ cycles. When

a conversion is completed, the result of the conversion can be read by accessing the data through the serial interface. Two *CLKIN* periods are needed for the acquisition time, giving a full cycle time of 23 *CLKIN* cycles at most. To extract the digital data, one needs 16 *SCLK* cycles because the data output is supplied as a 16-bit serial word. The *CLKIN* needs to be continuous. Thus, connecting it to *SCLK* pin is not an option because the *SCLK* is produced by the controller and is active only during SPI transfers. For our design, *CLKIN* will be provided either externally (function generator) or by the microcontroller thanks to the timerA toggle mode function. The maximum frequency both for the *SCLK* and *CLKIN* is 6MHz.

4.1.4 Digital to analog converter

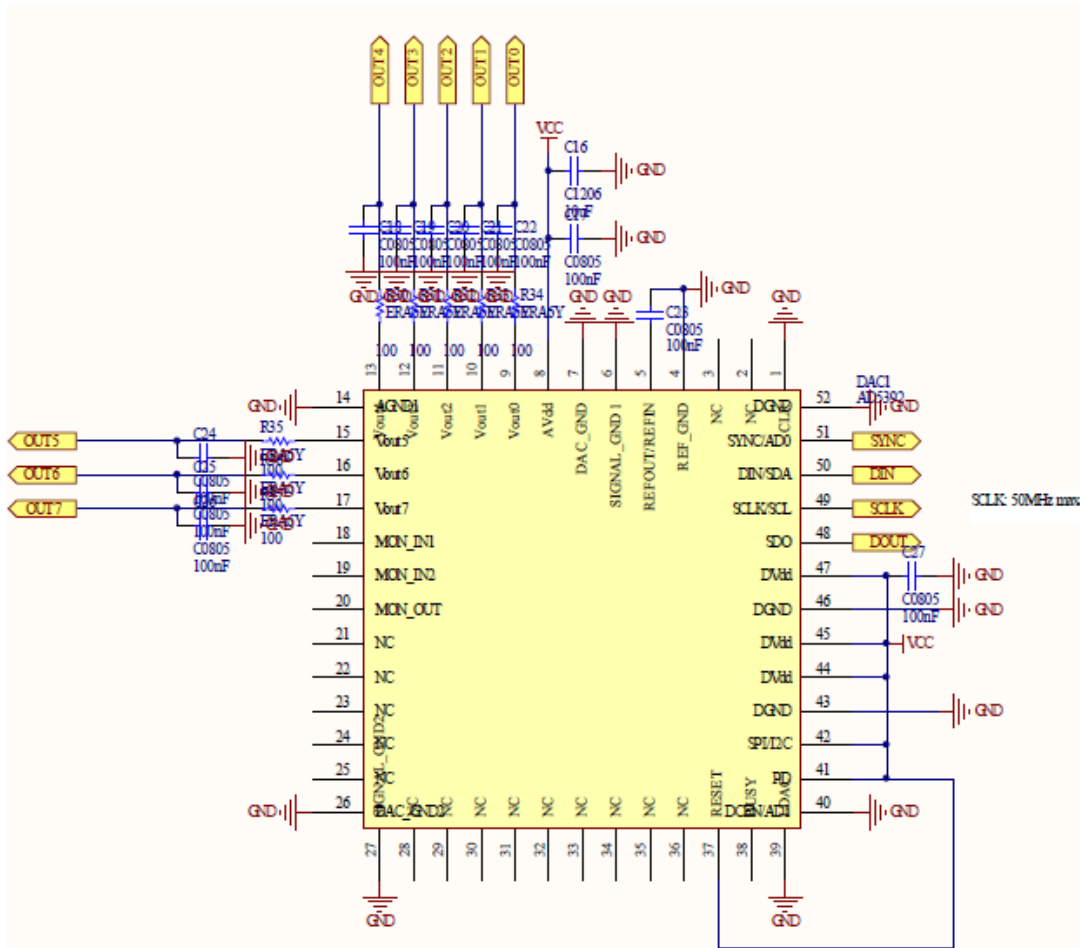


Figure 4.5: Digital to analog converter’s connections.

Like the ADC, the DAC possesses a SPI interface with three digital inputs and one digital output. Once again, the analog and digital ground are separated. The analog outputs, corresponding to the gains, are filtered with a low-pass filter of $15kHz$ cut-off frequency:

$$\tau = 100\Omega * 100 * 10^{-9}F = 10^{-5}s \quad (4.6)$$

$$f_c = \frac{1}{2\pi * 10^{-5}} = 15.915kHz \quad (4.7)$$

The maximum clock frequency is $50MHz$. The data-word format for the serial interface is 24-bit, so it takes 24 clock pulses until the 24 bits are clocked in.

4.1.5 Power supply

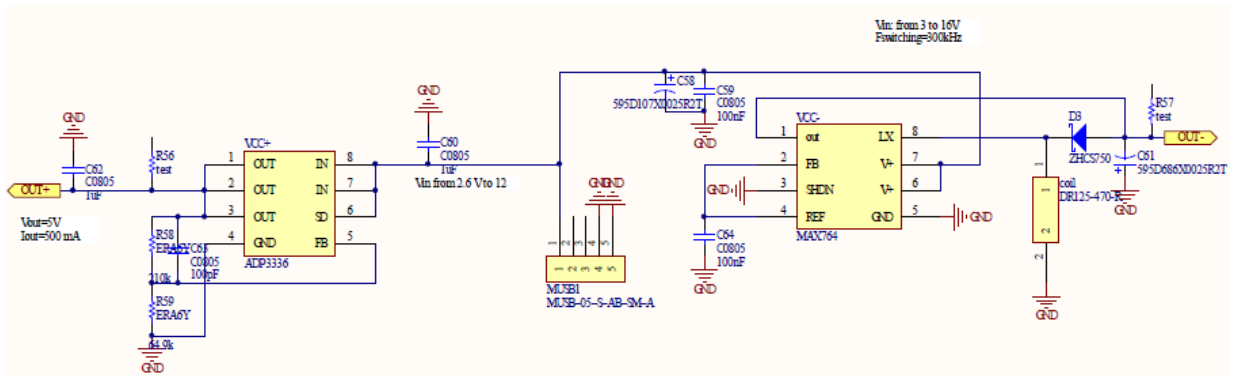


Figure 4.6: Power supplies' connections.

Actually, we need two power supplies: a positive one ($+5V$) and a negative one ($-5V$). We first look for the negative power supply to deduce what we need for positive power supplier.

Negative power supply The MAX764 is a $-5V / -12V / -15V$ or adjustable DC-DC inverter. Its switching frequency is $300kHz$ which is bigger than twice the ADC frequency of $30kHz$ ². The output current produced by the inverter must be higher than the supply currents required by the amplifiers. Having eight amplifiers, each one requiring $15mA$ at most, we need an output current bigger than $8 * 15 = 120mA$. The MAX764 output current reaching $250mA$, this inverter is adequate for our application.

²This is important to notice because DC-DC inverters introduce a lot of noise at half their switching frequency. Having one order of magnitude difference between the two frequencies is sufficient for us to know that the DC-DC inverter will weakly disturb our signal of interest.

For a fixed voltage application, the input voltage must be ranged between $3V$ and $15V$ and the FB pin is tied to REF . The data sheet recommends us to choose a $47\mu H$ coil, a $68\mu F$, and a $100\mu F$ low-ESR capacitors plus a Schottky diode. The “Rtest” resistor is used to check the real voltage we get on our PCB.

Positive power supply For the power supplier, we need a low dropout regulator. The ADP3336 fills this function and delivers a continuous load current up to $500mA$. The total amount of current needed is detailed in table 4.1 which is lower than the possible load current. It is important to leave a safety margin because we did not consider the resistor and the capacitor for our computation. For a continuous load current up to $500mA$, the ADP3336 delivers a dropout voltage of maximum $400mV$. The supply for the entire circuit must be at least of $5.4V$, which is compatible with the negative power supply.

Component	Supply current
Low-noise amplifiers	$8 * 36mA = 288mA$
Operational amplifiers	$8 * 0.375mA = 3mA$
ADC	$12mA$
DAC	$8 * 0.25mA = 2mA$
Total	$305mA$

Table 4.1: List of the different supply currents and the total supply current for the positive power supply.

The adjustable output voltage can be set by an external resistor divider (R_1 and R_2). In order to have the lowest possible sensitivity of the output voltage to temperature variations, it is important that the parallel resistance of R_1 and R_2 is always $50k\Omega$. Also, for more accuracy over temperature, the feedback voltage should be set at $1.178V$. After computation and to get an output voltage V_{OUT} of $5V$, we need $R_1 = 210k\Omega$ and $R_2 = 64.9k\Omega$.

To further reduce the noise by $6dB - 10dB$, a noise reduction capacitor (C_{NR}) can be placed between the output and the feedback pin. Low leakage capacitors in the $100pF - 500pF$ range provide the best performance.

Overall power supply The overall power supply is carried out thanks to a mini-B USB connector. A USB connector provides a single $5V$ supply on pin number 1 from which connected USB devices may power themselves. Supplied voltage is between $4.75V$ and $5.25V$ and a given segment of the bus is specified to deliver up to $500mA$ which is more than the current needed by the two power supplies: $120mA + 305mA = 425mA$.

The pins diagram is explained in table 4.2. In our application, we only need to connect pin 1 and pin 5. Pin 4 may be not connected, connected to *GND* or used as attachment identification. For simplicity, we decided to connect it to *GND*.

Pin	Name	Description
1	V_{CC}	+5V
2	D_-	Data -
3	D_+	Data +
4	ID	permits distinction of Micro-A- and Micro-B-Plug
5	GND	Signal Ground

Table 4.2: Pins table for Miniplug/Microplug [38].

To achieve the necessary power (5V and 500mA), we can not use a USB port on a computer³. The solution consists of using either a USB-hub (connecting five ports of the computer together) or a USB charger able to deliver at least 500mA. We choose the second solution for practical reasons (we already use one USB port for the eZ430-RF2500 Development Tool).

4.1.6 Connectors

In our project, we have two types of connector: analog and digital. For each one, we need to pay attention to very different aspects.

Analog connector To be compatible with what is already used in the BES-group, this connector should be an OMRON connector, i.e. a super low profile board to FPC connector. We need seventeen analog input signals:

- Eight analog signals for our signal of interest;
- Eight analog signals for possible offset compensation;
- One analog signal corresponding to the external ground and necessary for the pseudo-differential configuration of the low-noise amplifiers.

We decided to use a twenty-contact connector to take advantage of the necessary external ground to reduce capacitive coupling. Indeed, as shown on picture 4.7, every two connections of the signal of interest, we insert an external ground connection. All the ground

³A regular USB port is only capable of producing 5V and 100mA.

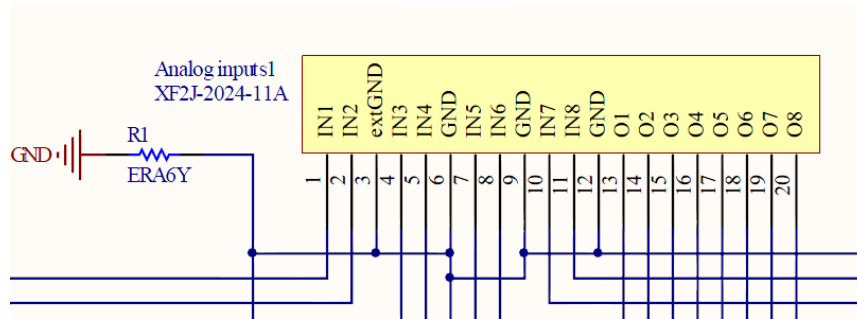


Figure 4.7: Analog connector.

connections can be either tied to the real board analog ground ($R1$ is set) or to the external ground ($R1$ is not set) if we decide to use the pseudo-differential configuration. The choice is possible thanks to the $R1$ resistor which can be soldered and disordered as convenient. This configuration allows a high symmetry and thus identical coupling for each analog channel.

For the offset signals, such a consideration does not matter because accuracy is not the priority and no amplification is made on these signals. If there was high frequency coupling, it would be filtered by the low-pass filtered at the operational amplifiers' inputs.

Digital connector For this one, we need five channels as it is shown on figure 4.9. The digital connections are connected to the available development pins on the eZ430-RF2500 Development Tool. The *Serial Peripheral Interface Bus (SPI bus)* is a synchronous serial data link standard named by Motorola that operates in full duplex mode [15]. Devices communicate in master/slave mode where the master device initiates the transaction. Multiple slave devices are allowed with individual slave select lines.

The SPI bus specifies four logic signals⁴ [15]:

- SCLK: Serial Clock (output from master);
- MOSI/SIMO: Master Output, Slave Input (output from master);
- MISO/SOMI: Master Input, Slave Output (output from slave);
- SS: Slave Select (output from master).

⁴Alternative naming is also used: DIN: Data In; SDO: Serial Data Out; DOUT: Data Out; SYNC: Serial Interface Pin.

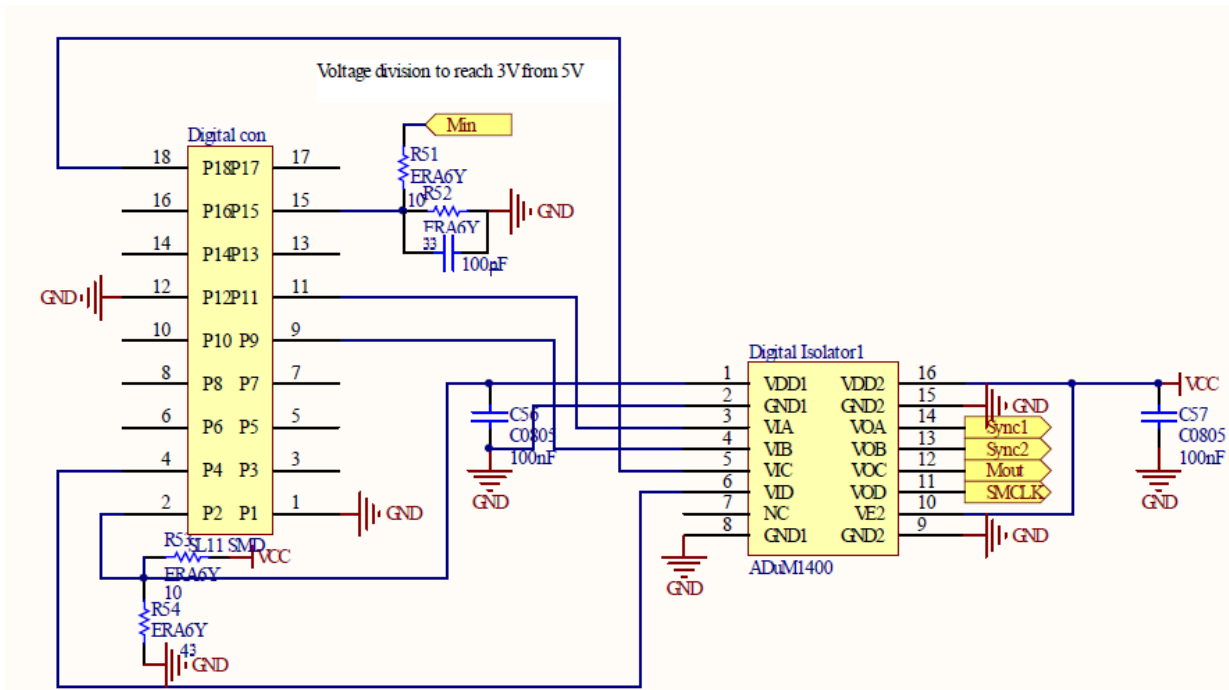


Figure 4.8: Digital connector.

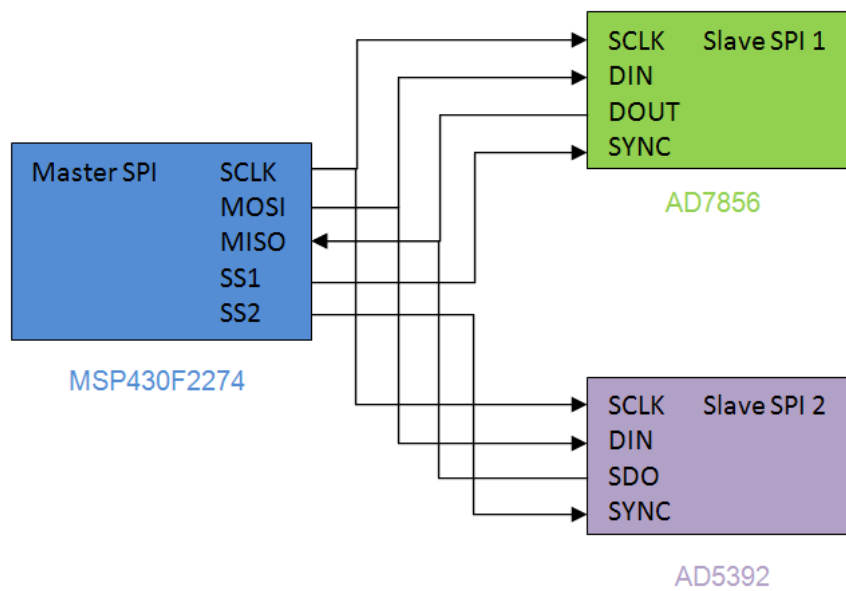


Figure 4.9: Typical SPI bus: master and two independent slaves.

The different pins for the SPI slaves are already examined in each specific section. For the SPI master, we need five pin connections:

- SCLK: pin P3.3 is used (master out in SPI mode) as the serial clock generated from the SMCLK (Sub-system Main Clock). We have the possibility to divide the MCLK (Master Clock) frequency by a factor of 1, 2, 4 or 8. The recommended operating conditions for the MCLK frequency is $16MHz$. To get the highest SCLK in the possible range⁵, we must provide a $12MHz$ MCLK and divide it by a factor 2 to get a $6MHz$ frequency clock⁶;
- MOSI: pin P3.1 is used (master out in SPI mode);
- MISO: pin P3.2 is used (master in in SPI mode);
- two SS: general-purpose digital I/O pins are used.

Nevertheless, there is a difference in voltage range for digital inputs and outputs between the components on the board and the MSP430F2274 on the eZ430-RF2500 Development Tool (see next section 4.3). For the AD5392 and AD7856, we find in the data sheet the informations resumed in table 4.3. However, for the MSP430F2274, we know that the maximum voltage applied to any pin ranges from $-0.3V$ to $V_{CC} + 0.3V$ with V_{CC} at a maximum of $3.6V$. It is thus neither possible to produce as an output from the MSP430F2274 a high enough voltage to be compatible with the AD7856 nor to connect directly AD5392 and AD7856's outputs to the microcontroller without exceeding the absolute maximum ratings.

Component	Logic level	Limitations
AD5392	Input High Voltage	$2V$ min
	Input Low Voltage	$0.8V$ max
	Output Low Voltage	$0.4V$ max
	Output High Voltage	$V_{DD} - 1V$ min
AD7856	Input High Voltage	$V_{DD} - 1V$ min
	Input Low Voltage	$0.4V$ max
	Output Low Voltage	$0.4V$ max
	Output High Voltage	$V_{DD} - 0.4V$ min

Table 4.3: Logic input and output voltages for the SPI slaves. V_{DD} is close to $5V$.

⁵The higher the frequency for the SCLK, the faster the conversion and it is then possible to obtain a $30kHz$ sampling frequency as discussed in section 4.2 .

⁶This is the upper limit for the AD7856.

For this reason, we need to use some tricks to reduce the voltage in one direction and to increase it in the other. Reducing the voltage is easily made with a potentiometric divider. The resistor choice is the following one: 10Ω and 33Ω in order to get almost $3.6V$ from $5V$:

$$V_{div} = \frac{33}{33 + 10} * 5V = 3.84V \quad (4.8)$$

Furthermore, to have a time constant sufficiently small, we need to add a capacitor in parallel with the 33Ω resistor. Without this fixed capacitor, we do not control the capacitive coupling and we get a relatively high time constant compared to the digital signals frequency ($6MHz$). With a very low capacitor ($100pF$), we manage to bring this time constant in a convenient range⁷:

$$\tau = 10\Omega * 100 * 10^{-12}F = 10^{-9}s \quad (4.9)$$

In the other direction, we need to pull up $3.6V$ to $5V$. This can be made thanks to a digital isolator. The ADuM1400 isolator provides four independent isolation channels based on the *iCoupler*[®] technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives, such as optocoupler devices [36].

iCoupler[®] isolators are magnetic couplers based on chip-scale transformers. Circuitry on one side of the transformer encodes the input logic transitions into $1ns$ pulses, which are then passed through transformers. Circuitry on the other side detects them and recreates the input signal [36]. For a falling edge, a single pulse is created whether for a rising edge double pulses are generated.

iCoupler[®] products possess tremendous advantages over traditional optocouplers in terms of power consumption (two orders of magnitude improvement in power dissipation), signal bandwidth (twice faster than the fastest optocouplers), robustness, and ease of integration (*iCoupler* technology[®] can be embedded with other data acquisition and control ICs⁸ in a very small area) which make them ideal choices for isolation applications [5].

4.2 Clock frequency

We need to check whether a serial clock of $6MHz$ is a high enough frequency for our application:

⁷The frequency of $6MHz$ leads to a period of $166,7ns$ which is two orders of magnitude bigger than $10^{-9}s = 1ns$.

⁸IC stands for integrated circuit.

- As stated in section 4.1.3, we need 23 CLKIN cycles to execute a conversion. We handle the read/write operation at the same time and it takes 16 SCLK cycles. For each read/write operation, we update in the **Control Register** the three bits *CH0*, *CH1*, and *CH2* to select the channel on which the next conversion will be performed. We also rewrite the **Conversion Start Bit**. A logic one in this bit position starts a single conversion, and this bit is automatically reset to 0 at the end of the conversion. We can perform the conversion and the read/write operation at the same time giving a full cycle time of $3.83\mu s$. We have eight channels and we want to read the conversion results from all eight channels consecutively. The full operation lasts $8 * 3.83\mu s = 30.66\mu s$ and we can reach $32.609kSPS$ ⁹ throughput rate, i.e. each channel is sampled at maximum frequency of $32.609kHz$. In addition, we need to add time for software instructions between conversions which leads us close to $30kHz$.
- In section 4.1.4, we stated that a write operation to the DAC was made through a 24-bits words. With a clock frequency of $6MHz$, it lasts $4\mu s$.

It is thus impossible to execute at the same time the voltage gain update and the conversion for all eight channels while remaining at a sampling rate of $30kHz$. A solution is to carry out the gain update regularly but not between each sampling step. One update after a certain number of samples (thirty for example) is a good trade-off. To these considerations, we must add the wireless transfer duration plus the UART communication which require a high number of software instructions. This point will be addressed in greater detail in the following chapter.

In addition to the serial clock for SPI communication, we need a continuous clock delivered to the ADC. This clock needs to be close to $6MHz$ as well in order to ensure that the **Control Register** write operation extends beyond the falling edge of BUSY (BUSY high indicates that either a conversion or calibration is being performed). Because we did not expect the serial clock to stop between each communication, we did not include this clock in the digital signals in the previous section. This is why this clock can either be produced externally (by a function generator) or by the timerA toggle mode function at half the frequency of the SMCLK ($6MHz$) on pin P2.2. but won't be elevated to 5V leading to a lack of accuracy.

4.3 eZ430-RF2500 Development Tool

The eZ430-RF2500 is a complete USB-based wireless development tool providing all the hardware and software to evaluate the MSP430F2274 microcontroller and CC2500 $2.4GHz$

⁹SPS stands for samples per second.

wireless transceiver. The eZ430-RF2500T target board is an out-of-the box wireless system that may be used with the USB debugging interface, as a stand-alone system or, which interests us more, may be incorporated into an existing design. For this purpose, the eZ430-RF2500T target board may be detached from the debugging interface and integrated into another design by removing the plastic enclosure. The target board features an MSP430F2274 and most of its pins are easily accessible. The eZ430-RF2500 is capable of remotely sending and receiving data from a PC using the MSP430 Application UART [31].

The hardware kit content is the following one (see picture 4.10):

- Two eZ430-RF2500T target boards;
- One eZ430-RF USB debugging interface;
- One AAA battery pack with expansion board.

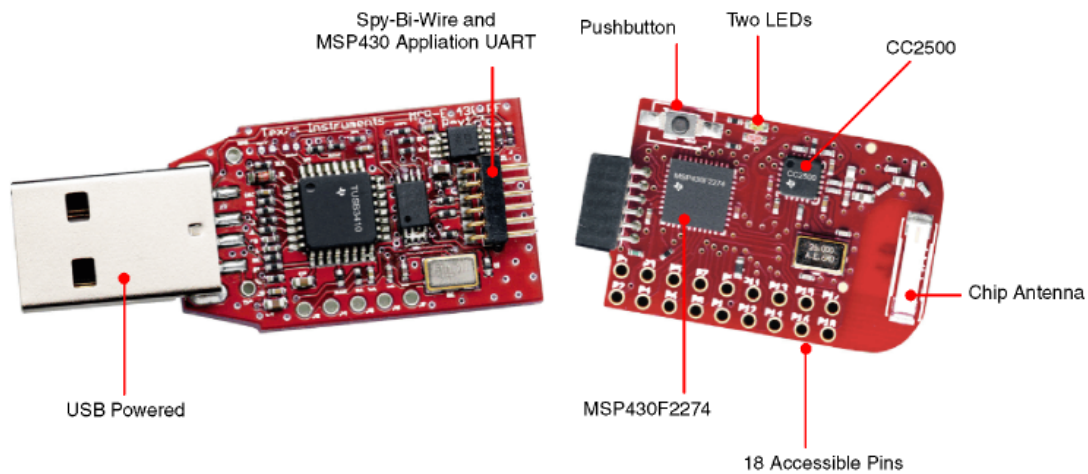


Figure 4.10: eZ430-RF2500 debugging interface (left) and target boards (right) [31].

For our application, the connections are shown on figure 4.11. We have access to eighteen development pins of the MSP430F2274. Pins that are useful for our project are examined in section 4.1.6. The physical connection between the eZ430-RF2500T target board and the PCB is carried out thanks to a simple male header connector with a 2.54mm pitch.

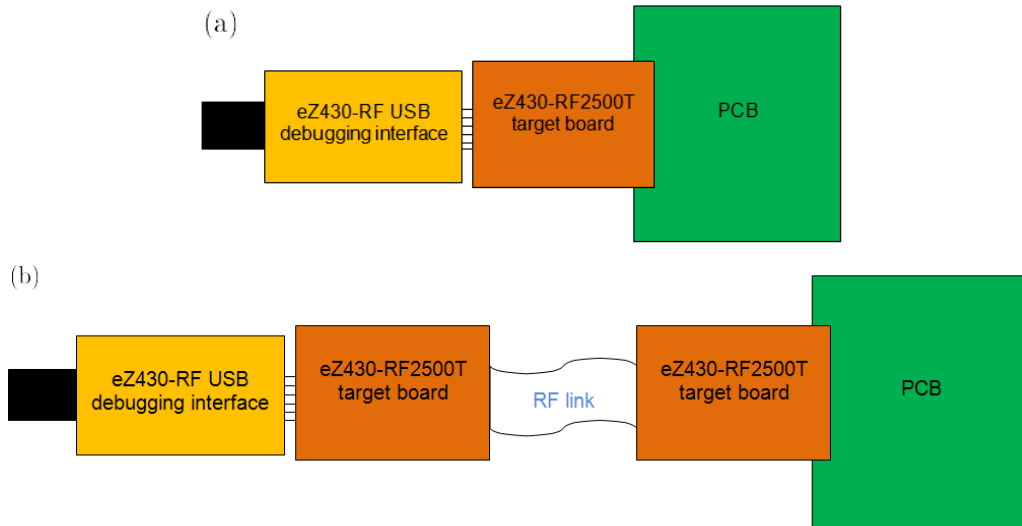


Figure 4.11: High level connection between the PCB and the eZ430-RF2500 Development Tool for (a) the wired and (b) the wireless configuration.

4.4 Printed Circuit Board

The first step in this part of the study consists of a components count (see appendix E) in order to get a first overall idea of the PCB size as well as of the form factor. From this table, we know the importance of passive components over active ones: out of the two hundred thirteen components, only fourteen are different from a resistor or a capacitor and possess a much bigger size. The PCB can thus be reduce to a very limited size especially if both sides are used.

The second step is a first components placement. Only active components and connectors are positioned on the PCB and attention to leave enough space for resistors and capacitors is primordial¹⁰. The signal's path is the criteria of interest with an adequate analog to digital separation. On figure 4.12 is shown this first components placement. The green line represents the separation between the analog part of the circuit and the digital one, the analog part being in the upper region. The red color stands for pins on the top layer and the blue color for pins on the bottom layer. One can observe that most components were placed on the top layer partly due to the analog to digital separation constraint. It is possible to design a much smaller PCB but it is not the most significant aspect in this part of the project and needs to be considered in future work.

¹⁰Typical space to save for resistors and capacitors is of 50% both for height and width.

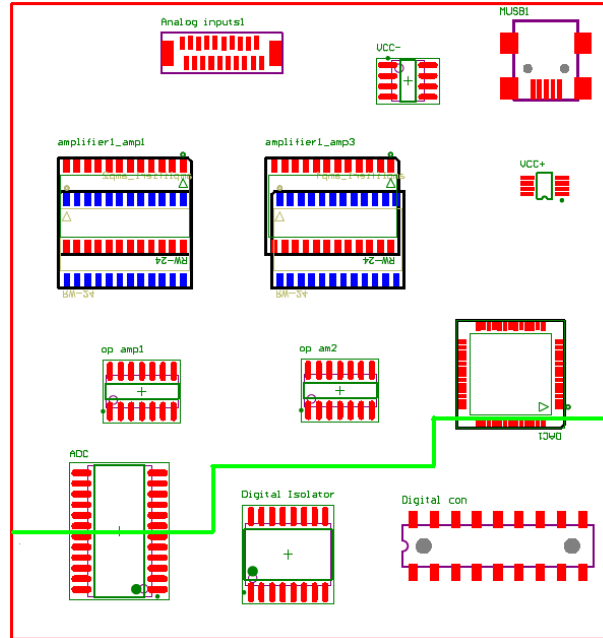


Figure 4.12: Active components placement, analog to digital separation (in green) and signal's path considerations.

The analog signal enters through the upper side by the *Analog inputs1* to reach one amplifier. The first four analog inputs go to the amplifiers on the left, whereas the last four analog inputs go to the amplifiers on the right. The output of those amplifiers head to the operational amplifiers, keeping their side. Signals to be digitized enter the ADC by the upper part of the component, avoiding the digital region. For the gain control, the digital signal comes from the digital connector, heads towards the DAC and the analog converted signal exits the DAC to join one of the amplifiers. Thanks to this design, few signal crossings are required and most of all, analog signals are isolated from digital perturbations.

Afterwards, the remaining components are placed and routing is performed. Special care must be given for analog routing, especially before amplification. Indeed, this part of the circuit is the most sensitive to perturbations and any capacitive coupling has significant effects on our signal of interest. Analog connections between the analog inputs and the low-noise amplifiers must thus be as much symmetrical as possible.

Our PCB is made of four different layers: the top layer is a signal layer with most of the signal path. The second layer is a ground layer with the analog ground and the digital ground, the two connected at a single point. The third layer is the power supply layer which possess much wider net than the signal layers. On this layer, we have three differ-

ent power supplies: the positive power supply, the negative power supply and the overall power supply. The fourth and last layer is another signal layer with fewer nets than the top one. No ground isolation is performed on this layer and thus care is to be given to avoid capacitive coupling between this layer and the power supply layer. The total size of the PCB is $7.5 \times 7.8\text{cm}^2$ and the final result is presented on figure D.1 in appendix D. Pictures representing the two sides of the PCB with components soldered are given in figure 4.13.

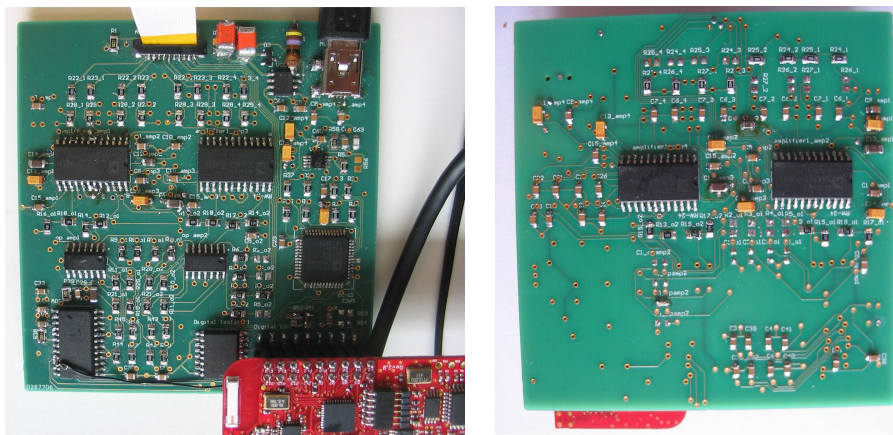


Figure 4.13: Pictures of the top (left) and the bottom (right) side of the PCB with soldered components. On the left picture one can identify the FPC connector, the USB cable and the eZ430-RF2500T target board. As expected, the bottom side counts more free spaces than the top side.

Chapter 5

Software design: microcontroller programming

This section describes the code implemented in the microcontroller MSP430 with a distinction between recording a single channel or eight channels sequentially. The MSP430's function is primarily SPI communication with both the ADC and DAC as well as the UART communication with the PC. In this section, we will not explain the principles for the wireless communication. For this purpose, the codes were updated to carry out the RF modulation and are detailed in section 6.

5.1 General description

The MSP430 is the link between our PCB and the computer. In this project, there is no digital processing on the computer. The only digital processing is carried out in the microcontroller itself and consists of adapting the gains to avoid saturation of the amplifiers' outputs. The gains are adapted according to the same procedure as the one developed in the MATLAB[®] script in section 3.7.3. The PC only stores the digital data for future use and allow UART interaction with the microcontroller.

Two different codes were created: one for the analysis of a single channel and one for the analysis of the eight channels concurrently. The procedure is basically the same in the two files but, due to time constraints, little changes are made for the actual sampling. The two codes are provided in the attached CD-ROM and are explained in following sections.

The development tool used for this project is the *IAR Embedded Workbench Integrated Development Environment (IDE)* provided with the eZ430-RF2500 Development Tool. This program allows us to write, download, and debug an application. The MSP430 features an application back channel which enables the eZ430-RF2500 to remotely send and receive

data from a PC. This allows the user to receive serial data in a terminal window (HyperTerminal) at a fixed rate of 9600bps ¹ with no flow control or to send data to the microcontroller.

The codes are largely inspired by files from *MSP430F22x2*, *MSP430F22x4 Code Examples (slac123.zip)*, an ensemble of codes available on the Texas Instruments website for future development codes purposes. The SPI schema is based on the *uscib0_spi_02.s43* code and the UART function on the *uscia0_uart_07_9600.s43* code.

Both for a single channel and eight channels analysis, there exist different codes depending on the complexity of the application desired. The basic code is a code with a fixed gain for each channel and a continuous clock provided externally. Complexity increases with the insertion of the timerA toggle mode function to replace the external clock. The introduction of variable gains after digital processing brings the application a step further. The most complex code introduces the possibility to communicate with the MSP430 to modify the gains thanks to actions on the keyboard.

5.2 Single channel analysis

The code for this section is available on the CD-ROM.

5.2.1 Basic code

The code is divided into three major parts: first of all comes an initialization process, then the main loop, and finally, the different functions needed. The block-diagram for this code is given in figure 5.1.

Initialization The initialization process sets the clock frequency of the Digitally Controlled Oscillator (DCO) at 12MHz and this clock produces both the Master Clock (MCLK) and Sub-System Master Clock (SMCLK) at the same frequency². The direction as well as the function for the different pins are set. The Universal Serial Communication Interface (USCI) is set in UART mode for the USCI_A module and in Three-Pin SPI Master

¹bsp stands for bits per second.

²In theory, we could have used the 26MHz quartz oscillator present on the board thanks to the XIN and XOUT pins of the MSP430 connected to the CC25000 GDO0 and GDO2 respectively and set the clock at 4.33MHz . Nevertheless, two problems appear with this solution: the first one is that the clock generated is not fast enough to manage a 30kHz sampling, and the second is that the PCB traces are not designed appropriately for a crystal oscillator circuit. On the other side, these connections prevent us from using an external crystal oscillator because we would be confronted to the GDO0 and GDO2 signals.

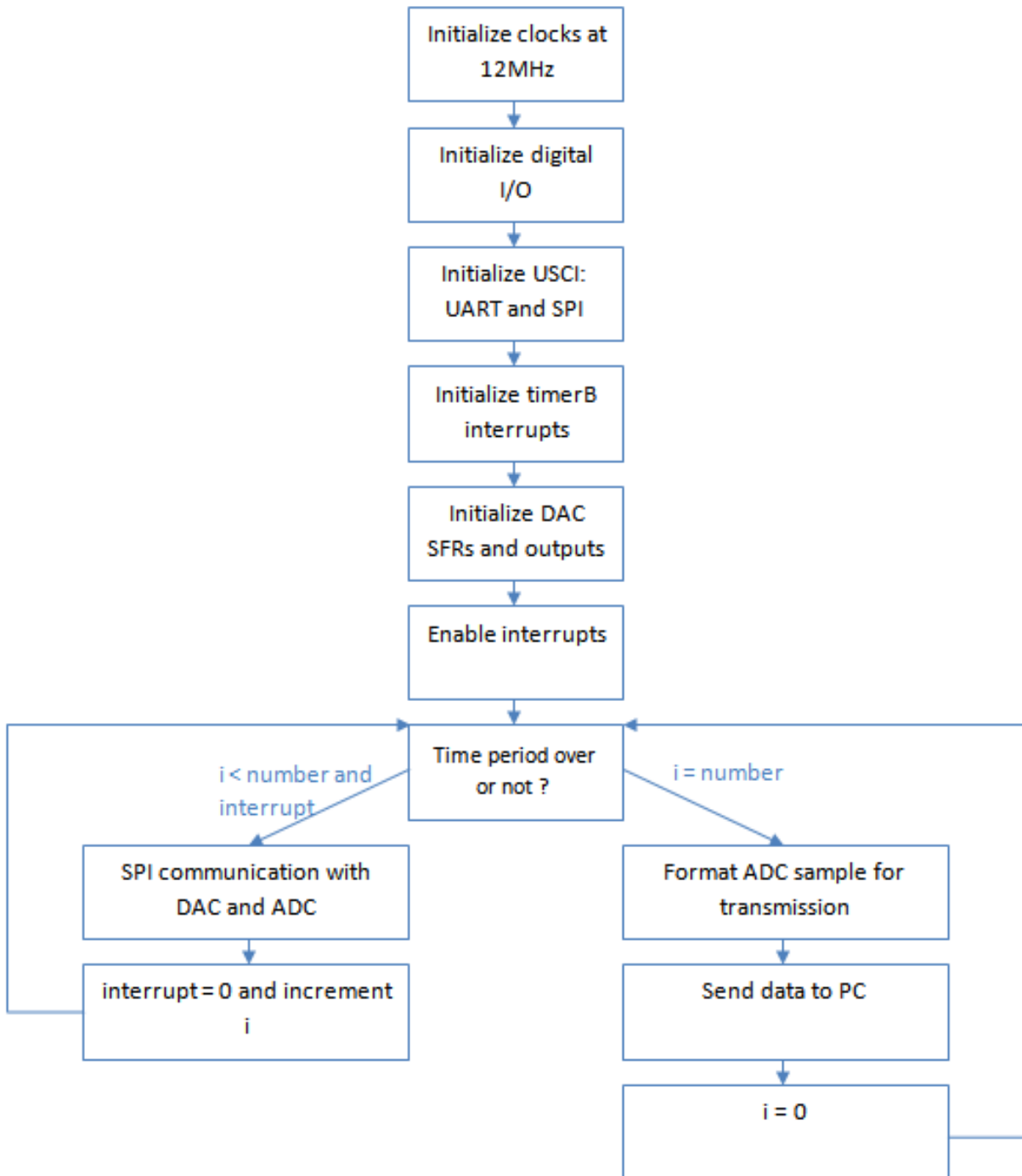


Figure 5.1: Block-diagram for single channel analysis.

Mode mode for the USCI_B module. The baud rate³ for the UART is fixed by the back channel of the MSP430 at 9600bps . For the USCI SPI clock, a frequency of 6MHz is settled as discussed in section 4.2. This also explains the choice of the 12MHz frequency for the DCO because the prescaler value can only be set to an integer value higher than two.

To get the frequency of 30kHz for sampling, timerB is used to generate interrupts at this exact frequency. The time period for observation is chosen at 5ms , which leads us close to the upper limit set by the MSP430 memory capacities. This time period allows one hundred fifty samplings and thus a correct signal reconstruction.

We then configure the DAC as desired (internal reference set at 2.5V and thermal monitor function⁴ enabled) by writing to the special function register to access the control register write. The last initialization consists of setting the gains. In fact, all amplifiers are turned off (VNG is tied to ground by setting the gain to a zero value) except the amplifier for the signal of interest (fixed by the variable *channelint*) which is set to the desired value.

Main loop Because the baud rate is fixed by the back channel UART, it is not possible to sample the signal and send its sampled values at a frequency of 30kHz . Indeed, the digital signal to be sent is composed of two bytes for both the signal and gain value, plus the four bits for the Start Bit, Parity Bit and the two Stop Bits necessary for UART communication. The UART transfer in itself lasts $\frac{4*8+4}{9600} = 3.75\text{ms}$ which is way bigger than the $33\mu\text{s}$ needed for the sampling frequency of 30kHz . This is why we chose to sample the signal for a fixed time period, store the values on the MSP430 and send them all at once through the UART to the PC when the time period is over.

The main loop consists of waiting for a timerB interrupt. When this occurs, the gain for the observed channel is set thanks to the DAC⁵ and the observed channel is sampled. The sampled value and the gain value are both stored in a vector for future reading.

To communicate with the DAC, we need three bytes. Each byte is sent through one SPI transfer and we thus need three SPI transfers for one complete communication. One transfer is performed in the following way: writing the value to transfer in the UCB0TXBUF buffer to start the SPI transfer (activation of the bit clock generator and the data will begin to transmit), waiting for the UCB0RXIFG flag to be set and collecting the data from the UCB0RXBUF buffer. The ADC needs only two bytes for SPI communication

³In this case, the symbol rate (baud[Bd] rate) is equivalent to the bit rate[bps] because we only use one bit per symbol.

⁴This function powers down the device when the temperature exceeds 130°C and protects it against excessive power dissipation.

⁵In this case, it is not necessary to update the gain at each loop but it's convenient for future reuse for more complex codes.

and the same technique is used. In each case, prior to the SPI start, we need to reset the chip select to enable the corresponding device. Furthermore, the two devices do not use the same clock polarity. The SPI clock polarity is therefore changed before any communication by resetting the USCI, changing the clock polarity, and finally initializing the USCI state machine.

After one hundred fifty samplings, the vectors with the signal values and the gain values are sent to the computer via the back channel UART and displayed on the HyperTerminal window. Those values can then be saved in a file for future work. The time counter is set to zero and the sampling process restarts with the last gain value from the preceding sampling period.

For interactive reasons, the red light is on during the sampling period and the yellow light is on during the UART transmission to allow the user to see in which state is the microcontroller.

Functions Four main functions are necessary:

1. TimerB interrupt: this sets the *interrupt* variable to one. This variable is checked in the main loop to detect if an interrupt has arisen. In case it has, the DAC and ADC are activated sequentially and the variable is reset to zero at the end.
2. Conversion from an integer to two characters: this enables to store values in the integer format but to use them in two characters format when necessary.
3. Conversion from two characters to an integer: this reverses the previous function.
4. UART communication: those functions allows the UART transfer following the same procedure as for SPI transfer. On the HyperTerminal window, ASCII characters are displayed and thus a conversion from hexadecimal to ASCII is performed.

5.2.2 TimerA toggle mode function

The toggle mode function allows the output to toggle when the timer counts to the TACCR0 value. The output period is double the timer period. We set the timer period to $12MHz$ and it results in an output period of $6MHz$. The output is accessible on the pin P2.2. The code to add this function is very simple:

```
//TimerA
TACCR0 = 1; // Timer period = SMCLK period
TACTL = TASSEL_2 + MC_1; // SMCLK, upmode
TACCTL0 = OUTMOD_3; // Toggle mode
```

In addition to this code, we need to plan a latent period prior to any SPI communication to allow auto-calibration for both devices. For the AD7856, this period needs to last at least $42ms$. Before, this latent period was unnecessary because the continuous clock was applied externally and thus before the MSP430 programming and the auto-calibration was performed way before the start of SPI communication.

5.2.3 Variable gain

First of all, we tried to implement the same gain adaptation as in section 3.7.3. However, as described in more details in chapter 7, because of the limited digital processing, this method gave very poor results. This is why we implemented a simplified version of this method: initialization of the gain at the maximum value and reduction until reaching a state of no saturation. For the reduction to be adapted to the gain value, we diminish the gain by a certain percentage. What is different from the preceding method is that there is no augmentation of the gain anymore and therefore, the choice of the percentage value is critical. An analysis for this parameter is performed in the results analysis chapter. The code for this section is given in the CD-ROM.

5.2.4 Keyboard control

This section proposes another strategy for fine tuning of the gain: digital signal processing being limited, we allow the user to control the gain through the keyboard. The gain is initialized at its maximum value. If the user wants a reduction of the gain, he or she types the key **m**, whereas if an augmentation is desired, the key **p** is typed. The modification of the gain is carried out as before (percentage of the current gain). Actions on the keyboard trigger an UART interrupt and the variables p and m , which will be checked in the main loop section, are updated. UART interrupts are disabled during the UART sending to the PC to forbid interruption of this process.

To increase the accuracy, the user has the possibility to modify the percentage by which the gain is to be adapted. The choice is given between 1/10, 1/100 and 1/1000 both for augmentation and reduction. Depending on the key typed, a percentage is selected: for an augmentation, **p** is for 1/10, **o** for 1/100 and **i** for 1/1000; for a reduction, **m** is for 1/10, **l** for 1/100 and **k** for 1/1000⁶. The code for this section is given in the CD-ROM.

⁶The choice for these keys has been made because they are adjacent in an AZERTY keyboard.

5.3 Eight channels analysis

The procedure is very close to the precedent except, for eight channels analysis, time considerations are critical to reach the desired sampling frequency. As stated before (in section 4.2), sampling the eight channels already leads us close to the $33\mu\text{s}$ limit. In addition, we need to add between each channel sampling step time for the microcontroller to restart sampling. For example, a *for* loop for channel selection or a *timerB interrupt* take too many instructions to be considered in this part of the program. Despite all our trials, time between two samplings could not be reduced enough to allow a gain update within the $33\mu\text{s}$ time period. This is mostly due to the fact the gain update requires a SPI communication of three bytes.

The program executes the same initialization steps except the timerB is not settled because of the time restrictions discussed just above. The use of numerous constants is interesting because it is less instruction demanding than accessing a variable in a table. Moreover, data are stored as byte and not as an ensemble of two bytes for the same reason. We avoid using a *for* loop for the channel selection by explicitly sampling each channel to remain in the 30kHz sampling domain.

Before the real sampling begins, we need to initialize the ADC. Indeed, instructions given to the converter are sent back only two SPI communications later. For example, when we send bytes to sample the first channel, we do not get in return the sampled value for the first channel. This is explained graphically on figure 5.2. This is why we send, prior to the loop on time, data in for the seventh and the eighth channels. This also explains why there exist a shift between the data sent to the ADC and the data sent through UART.

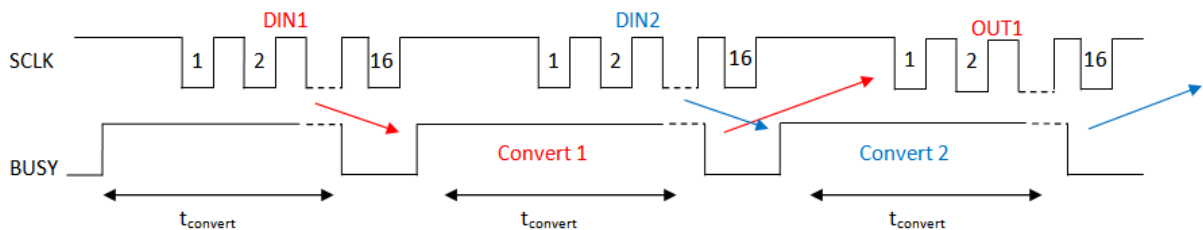


Figure 5.2: Timing diagram for reading/writing during conversion for the AD7856. During the first SPI transfer, writing is performed for the first channel. During the second SPI transfer, the first channel is digitized. During the third SPI transfer, digital data are sent to the MSP430 and collected.

After fifty loops⁷, the UART communication is performed. It displays the sampled values for each channel as well as the gain for that specific channel. The red LED is on during the sampling process and the yellow LED is on during the UART transmission.

We also added the same functionalities to the code as in the previous section. The timerA is settled with the same instructions and gains are updated with the same strategy as in section 5.2.3. As stated before, it is not possible to update gains after each sampling. This is why the update is made at the end of each sampling period in order to update the gains for the next period. After the UART communication, the last sample for each channel is checked to detect whether there is saturation or not. If there is saturation, the gain for that specific channel is updated. Otherwise, the gain remains unchanged. Due to limited digital processing once again, we do not look at the entire signal but only at the last sample and no augmentation is possible.

Interaction with the MSP430 is once more possible through the keyboard. This time, because of the multiple possible channels, the user has to choose which channel's gain he or she wants to modify. This choice is handled by typing the number of the channel of interest on the numeric keyboard. Several channels can be selected at the same time and the action on them will be the same. To deselect the channels, the key `s` is typed. Because UART interrupts are disabled during UART transfer of gains and values, the reaction to keyboard's action is not very sensitive. This is why it is not possible to implement a technique of deselection of a single channel. As in the previous section, it is possible to choose the percentage of augmentation or reduction between 1/10, 1/100 and 1/1000. The code for this section is given in the attached CD-ROM. No block diagram is given because it is very similar to the one for a single channel analysis.

⁷The number of samplings is very low due to memory restrictions from the MSP430.

Chapter 6

Wireless link

We developed a wireless link between our PCB connected to an eZ430-RF2500 target board and the other eZ430-RF2500 target board connected to the eZ430-RF USB debugging interface as shown on figure 4.11 (b). This chapter deals with the design of this wireless link from both hardware and the software points of view.

6.1 Hardware design of the wireless link

As already stated previously, we use the MSP430 wireless development tool, a tool providing all the hardware and software to evaluate MSP430F2274 microcontroller and CC2500 2.4GHz wireless transceiver. Performance of the RF link for one node to the PC was measured indoor and reached a line-of-sight range of more than fifty meters [31].

The CC2500 is a low-cost and low-power 2.4GHz RF transceiver. The main operating parameters and the 64-byte transmit/receive First-In-First-Out's (FIFO) of CC2500 can be controlled via a three-wire SPI interface. The major connections are shown on figure 6.1. On this figure, we recognize the three-wire SPI connections (where CC2500 is the slave) with the USCI_B module already used for SPI communication with the on board ADC and DAC. Attention has to be given to avoid conflicts between different SPI slaves using the same ports. In addition to the SPI connections, we find connections to the external 26MHz crystal oscillator and connections of the general digital output (GDO) pins to two pins on the MSP430. Those GDO pins can output internal status information useful for control software and generate interrupts on the microcontroller. Eventually, two pins are connected to the chip antenna to transmit the RF modulated data in the two directions (RF_P and RF_N are input pins in receive mode and output pins in transmit mode).

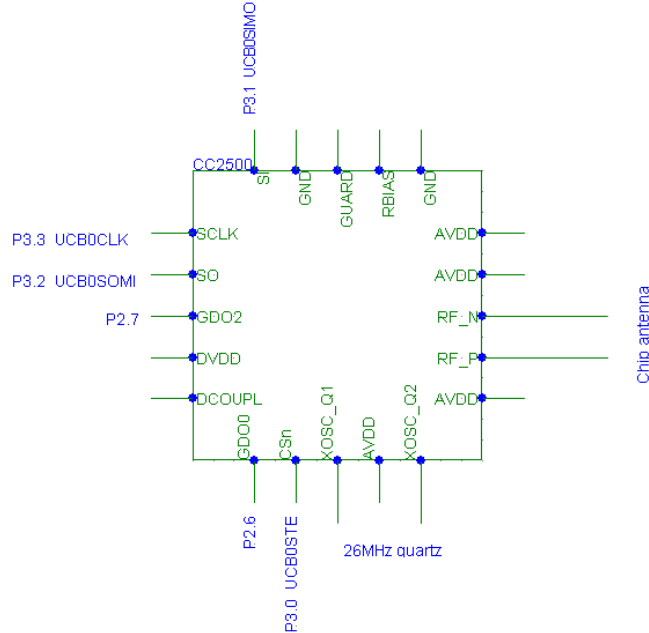


Figure 6.1: Major connections for the CC2500 on the eZ430-RF2500 target board. Connections handle a three-wire SPI communication, an external crystal oscillator circuit, chip antenna interaction and general digital output pins to MSP430.

6.2 Software design of the wireless link

The software for the wireless part is largely inspired from the eZ430-RF2500 demonstration application: a temperature sensor network using the SimpliciTITM network protocol. This section is based on Texas Instruments documentations [31][32][33].

6.2.1 Texas Instrument tools

Two tools provided by Texas Instruments are used to create the software for the wireless link¹:

1. SimpliciTITM network protocol;
2. SmartRFTM Studio software.

SimpliciTITM network protocol is a simple low-power RF network protocol aimed at small RF networks². This protocol is designed for easy implementation and integration on

¹Entire section inspired by [33].

²RF networks are considered small if they possess less than one hundred nodes.

several Texas Instruments RF platforms (such as the MSP430 family and the CC25XX transceivers) and requires minimal microcontroller resources. Small low-power RF networks usually interconnect battery powered devices and care is to be given to battery lifetime, low data rate, and low duty cycle. The SimpliciTITM network protocol allows to take those restrictions into consideration. Despite the minimal resources required, SimpliciTITM network protocol supports End Devices (ED) in a peer-to-peer network topology³ and the option to use an Access Point (AP) for a connection to a PC.

The SmartRFTM Studio software is a Windows application that can be used to evaluate and configure low-power RF components. The application helps designers to easily obtain optimum register settings, and to evaluate performance and functionality.

6.2.2 Network overview

The network is composed of two identical target boards programmed with distinct software to exist as members of the wireless network. The AP manages the network and receives data from the ED⁴. The ED is the board connected to our PCB; it takes care of the SPI communication with the ADC and the DAC and sends the results to the network's AP. Upon receiving the data from the ED, the AP sends it through its application UART to a COM port on the PC for presentation to the user by the HyperTerminal window.

Access Point The first action of the AP is to transmit a start-up splash to the PC (shown on figure 6.2). The AP is then initialized as the network hub and, when the initialization process is over, the AP transmits to the COM port a message notifying completion of the task (see figure 6.2). From now on, the AP is continuously listening for the ED to join the network. When it is done, it waits to receive packages from the ED and sends back a message to the ED whenever it happens⁵. For interactive purposes with the user, the AP toggles its two LEDs: the red LED indicates the transmission to the PC via UART and the yellow LED indicates the reception of a packet from the ED.

End Device When the ED is powered on, it first searches for the AP while toggling both the yellow and red LEDs. When it finds the AP, the ED tries to make a link (at that time, the red LED is on to indicate the link attempt). When the link is created, all LEDs

³A peer-to-peer network topology is a distributed network architecture composed of participants that share a portion of their resources such as processing power, disk storage or network bandwidth [38].

⁴In fact, the AP can manage a network with up to thirty EDs but it is not useful for our application. Therefore, this section focuses on describing a network with a single ED.

⁵Sending back a message to the ED to let it know the message was received and processed is necessary because the RF transmission ($250kBd$) is much faster than the UART one ($9600Bd$). Without the dual communication, the ED would keep sending data, filling up the AP's RX FIFO and create an overflow leading to data lost.

```

eZ430-RF2500
Neuro_reception
Julie Dethier
April 2010
Initializing Network...Done

```

Figure 6.2: Application Start Splash screen (first four lines) and Initialization Completed screen (last line).

are turned off and the ED begins the SPI communications with the ADC and DAC and sends the results to the AP while toggling the yellow LED.

6.2.3 Application software

Access Point This software does not change much from the eZ430-RF2500 demonstration application and is provided in the attached CD-ROM. The flow chart for this node is given in figure 6.3. The code begins with different initializations:

- *BSP_Init()*: initializes both the communication between the microcontroller and the radio (at $250kBd$) and LEDs toggling;
- *Flash address*: creates a random address to keep track of the AP if ever it goes down. The ED can recognize it thanks to this address when it resets;
- *MCU_Init()*: carries out MSP430-specific initializations (DCO, MCLK and SMCLK are set to run at $12MHz$ and USCI_A is in UART mode to communicate with the PC);
- *Splash screen*: sends the Splash message to the HyperTerminal window;
- *SMPL_Init(sCB)*: initializes the network function via the SimpliciTITM network protocol and displays a message on the screen when initialization is completed.

The *sCB* parameter is a function pointer to a callback function (*static uint8_t sCB(linkID_t lid)*) which is responsible for incrementing either the *sJoinSem* or the *sPeerFrameSem* semaphore when the AP receives a packet from an ED. The *sJoinSem* semaphore is incremented when an ED tries to join the AP's network (an ED calls its *SMPL_Init()* for the first time) and the *sPeerFrameSem* semaphore is incremented when the ED is already connected to the AP and sends a packet. Those two semaphores control the main loop.

If the *sJoinSem* semaphore has been set, the AP will listen for a link (*SMPL_LinkListen()*) and increment the *sNumCurrentPeers* parameter when the link is established as well as



Figure 6.3: Block diagram for the Access Point. Functions are represented in red, semaphores in blue and variables in italic.

unlocking the semaphore. Having only one ED in our application, the *sJoinSem* semaphore should be set only once.

If the *sPeerFrameSem* semaphore has been set or incremented, the AP stores the *Received Signal Strength Indicator* (RSSI)⁶, the gain and the ADC sampled value received in a *msg*

⁶The RSSI value is an estimate of the signal level in the chosen channel. It is output as a percentage for readability.

buffer and sends it via UART to the COM port of the PC to be displayed on the screen. When the UART communication is over, the AP sends back the *msg* buffer to the ED to indicate the possibility to process the next values. An illustration of the message displayed on the HyperTerminal window is shown on figure 6.4.

```
New sampling period
Channel:1,Value:1F70,Gain:1000,Strength:060%
Channel:1,Value:1F74,Gain:1000,Strength:060%
Channel:1,Value:1F73,Gain:1000,Strength:060%
Channel:1,Value:1F6F,Gain:1000,Strength:061%
Channel:1,Value:1F6F,Gain:1000,Strength:060%
```

Figure 6.4: Message displayed on the HyperTerminal window. Indication of a new sampling period is shown by the message “New sampling period”. For each sample, information on the channel, value, gain and RSSI (representing the strength of the signal) is given.

End Device In this section, we describe the ED software for a single channel and a fixed gain. Just as in chapter 5, there exist softwares for variable gain and for eight channels analysis concurrently⁷. For this software, we only give the version with timerA toggle mode function as the continuous clock for the ADC. The program is given in the CD-ROM and the flow chart on figure 6.5.

The initialization process is very similar to the one for the AP: initialization of the radio, of the microcontroller plus the DAC special function registers, trials to link to the network by initializing the network and then linking to the AP. The main loop is however very different: if the time period is not over yet (time counter *i* is below *number*), the ED waits for a timerB interrupt. When this occurs, the ED communicates with the DAC and the ADC before returning waiting. If the time period is over, the ED sends one packet of sampled data to the AP, waits for a reply (incrementation of the *sPeerFrameSem* semaphore) and redo the operation. The last packet to be sent is a blank message to display on the window indications that a new sampling period begins.

Keyboard control This function, introduced in chapter 5, is adapted for the wireless application. Only small modifications must be made to the software already detailed. For the AP node, we add an UART interrupt function which is responsible for updating the variables *p*, *m* and *l*. Those three variables are sent to the ED through the necessary reply *msg*. On reception of this *msg*, the ED updates its own *p*, *m* and *l* variables and changes the gain at the beginning of the next sampling period. To avoid disrupting the message displayed on the HyperTerminal window, UART interrupts are disabled during

⁷Because they have already been discussed before, they won't be examined again in this chapter.

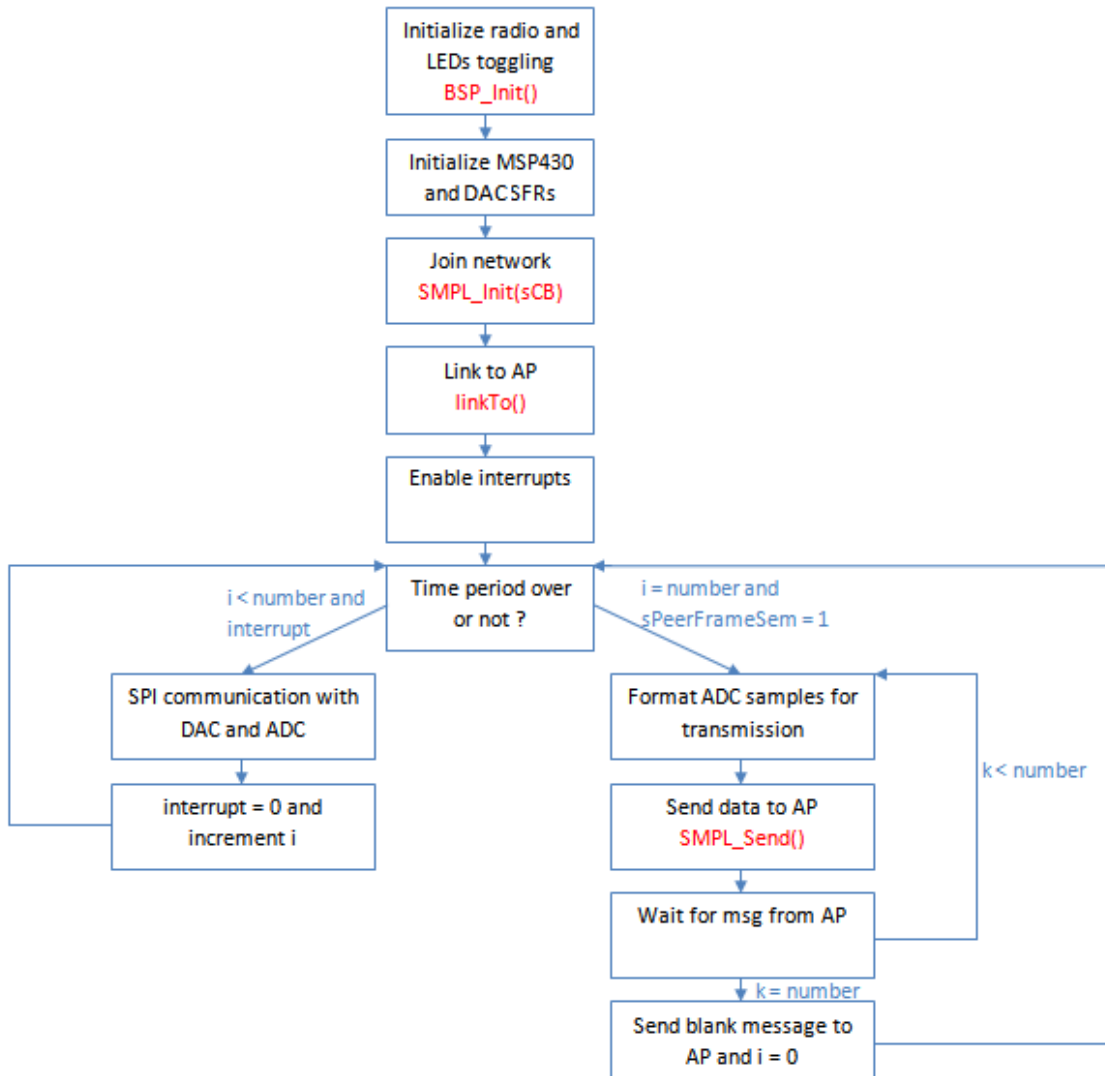


Figure 6.5: Block diagram for the End Device. Functions are represented in red, semaphores and variables in blue.

communication with the COM port of the computer. This explains why gains can only be changed once at the beginning of the sampling period (it results from previous keyboard actions).

Chapter 7

Testing procedure and results analysis

This part of our work consisted of designing a testing environment for our PCB. Due to the numerous signals needed and the weak amplitude necessary, the testing procedure is not straightforward. Three different aspects must be taken into consideration: the connections to the PCB's analog connector, which can not be done with simple banana cables and crocodile clips, the dynamic testing, which needs to be carried out with signals amplitude ranging from $20\mu V$ to $100mV$ at different frequencies ranging from $100Hz$ to $10kHz$, and the generation of DC signals for the active offset compensation voltages. Then, we test our design in various conditions to determine its performance and limits.

7.1 Testing setting

7.1.1 Analog connections to the PCB

Because the probe developed by the BES-group (see section 1.5.1) is connected through a FPC cable and OMRON connector to external instrumentation, we chose for our PCB the same interfacing ensemble. A FPC cable is designed to connect two PCBs together. For this reason, we need to create another PCB for the analog connections.

This PCB is the interface between our circuit and the analog signal generator. We need seventeen analog signals: eight analog inputs, eight analog offset compensations and one external ground. Analog inputs possess very weak amplitudes and, therefore, those signals are very prompt to magnetic perturbations from external circuits. For this reason, the use of shielded cables to protect our signals of interest from external perturbations is performed. A guarded cable is not needed in this situation¹ and would not be connected correctly. Coaxial cables are used as shielding and BNC connectors make the connections

¹The source impedance is small enough to have few impact on the measure.

with the PCB. This way, we also get our external ground². The new PCB is very simple (see appendix C and D): twice eight BNC connectors which ground are tied together and signals tied to an OMRON connector pins. Pictures of the total setting are shown on figure 7.1.

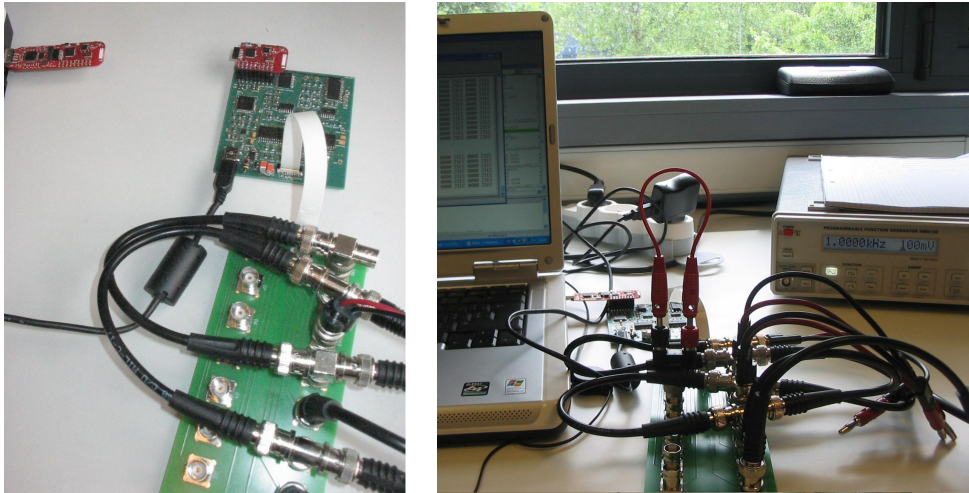


Figure 7.1: Pictures of the total setting. The board is connected wirelessly to the PC via the eZ430-RF2500 Development Tool and to the functions generator via the second PCB and a FPC cable. Coaxial cables are used to limit interferences. The offset compensation inputs are left open.

Having signals with very weak amplitudes, conductors' choice is primordial. We also must pay attention to reject interferences from the external world. Interferences can attack our signal in two distinct manners: magnetic interferences or galvanic interferences. For the first ones, the shielding of the coaxial cable constitutes a good protection. For the second ones, the circuit configuration is what matters: the measurement circuit and the source should not be connected to the same "ground". This point is examined in section 7.2.4³.

7.1.2 Instruments and divider

Three instruments are used to test our board: two function generators (the HM8150 and the TG2000) and one programmable power supply (the HM8143). One of the function generators is used to output the continuous clock and the other one to output the sinus

²The external ground signal is the same as the ground making the shielding. This ground can be very different from the board ground.

³This entire section is based on [34].

wave considered as the analog input. If we use the timerA toggle mode function, the two function generators can be used as analog inputs. The characteristics of each function generator are presented in table 7.1. From this table, we see that the HM8150 presents a better accuracy for small signals but the TG2000, however, is able to produce a smaller voltage ($1mV_{pp}$). This is why we use the TG2000 to generate the analog input signal.

	HM8150	TG2000
Accuracy	$\pm 4\%$	$\pm 3\% \pm 1mV$
Resolution	$1mV$	3 digits
Output voltage	$20 - 200mV_{pp}$	$1mV_{pp} - 20V_{pp}$
DC offset	$\pm 75mV$	$\pm 10V$
Offset error	$\pm 50mV$	$\pm 3\% \pm 10mV$

Table 7.1: Characteristics of the two functions generators. For the HM8150 function generator, the smallest range is used.

From the table, we also see that the two instruments proposed are not able to produce signals with small enough amplitude. To achieve the lower limit ($20\mu V = 40\mu V_{pp}$), we use a divider with very high value (see figure 7.2). On this figure we did not represent the source and the input impedances because they are negligible compared to the divider's values (source resistor is 50Ω , input resistor $300k\Omega$ and input capacitor $8.5pF$). The output voltage is divided approximately by a factor 1000 and the high-pass filter cut-off frequency is $339Hz$. The $1M\Omega$ resistor introduces a lot of noise⁴ and this divider is used only to generate signal amplitude lower than $1mV$ and frequency higher than $500Hz$.

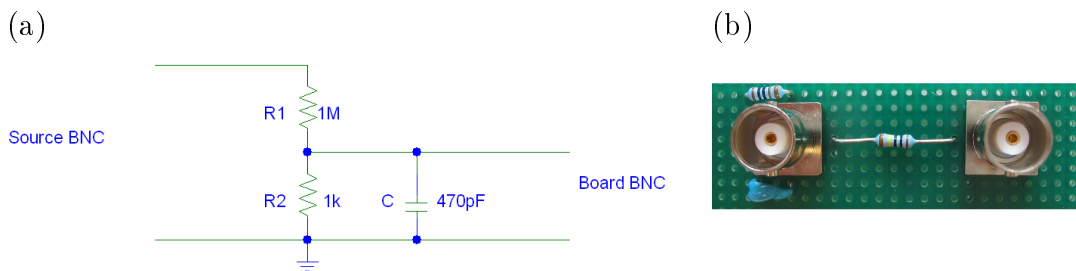


Figure 7.2: Divider's schematic (a) and picture (b) to diminish the amplitude of the input signal. The divider reduces the amplitudes of the signal by a factor 1000 and constitutes a high-pass filter with $339Hz$ cut-off frequency.

⁴For thermal noise: $v_{sd} = \sqrt{4kTR} = 0.128\sqrt{R}$ at ambient temperature. In the present case: $v_{sd} = 0.128\sqrt{10^6} = 128nV/\sqrt{Hz}$.

7.2 Connections and components validity

In this section we analyse whether the different choices made previously carry out the results we desire. It is not yet an analysis but a first step to determine if our design is acceptable or not. All graphs are created thanks to the MATLAB[®] software, the red dots are the digital data displayed on the HyperTerminal window and the blue curve is obtained using a usual reconstruction technique: interpolation of sinus cardinal functions. For curves computed numerically (green curves), an evaluation of the phase shifting is performed in order to produce the curve leading to the smallest difference with the reconstructed curve.

7.2.1 Time analysis

Table 7.2 resumes the different time periods significant for our project. We see that the sampling frequency for a single channel is accurate because it is settled by timerB interrupts, whereas for eight channels, despite all our effort, we do not manage to reach the $30kHz$ frequency. The difference is minime (2%) and it should not matter much.

	one-wired	eight-wired	one-wireless	eight-wireless
Sampling frequency	$30kHz$	$29.4kHz$	$30kHz$	$29.4kHz$
Number of samplings	150	50	150	35
Sampling time period	$5ms$	$1.7ms$	$5ms$	$1.2ms$
Time between sampling periods	$2.26s$	$3.16s$	$8.3s$	$15.5s$

Table 7.2: Time periods for different configurations. Each column corresponds to one configuration: sampling of one channel wired, eight channels wired, one channel wireless and eight channels wireless. The sampling frequency for a single channel is fixed at $30kHz$, whereas for eight channels, it is free. The sampling time period is limited by the MSP430 memory capacity. Time between two sampling periods is mostly set by the UART communication.

Due to the MSP430 memory capacity limits, we are not able to record the signal for $5ms$ in each case. The more data we have to store, the shorter the recording period. From this observation, we notice that the recording period for eight channels is very small especially respectively to a period of a $100Hz$ sinusoid: in this case, a total period lasts $10ms$ and we are only able to observe one fifth or even one eighth of a complete period. For this reason, we analyse in more details the single recording structure because the performance are almost identical but the observation period is much longer.

The time between two observation periods is mostly settled by the UART communication. Indeed, this communication is very slow ($9600Bd$) and significant amount of information

needs to be sent (sampled values, gains plus channel observed and, in the case of the wireless communication, the RSSI). This time period could be shortened by speeding up the baud rate but this one is fixed for the eZ430 application. Even if we manage to augment the baud rate, we are still not able to sample and send data at a $30kHz$ frequency. Another option is to diminish the quantity of information sent (especially for wireless transmission) but then the user interface is less attractive and comprehensive. If we absolutely want to record continuously, in addition to the baud rate speeding up, we must also accelerate the SPI communications, meaning we need to find another ADC. Depending on applications, it might or might not be an option (speeding up communications also means augmenting power consumption).

7.2.2 DC bias levels at the amplifiers inputs

The AD604 is composed of two amplifiers (see figure 7.3(a)): the signal is processed through an ultra low-noise preamplifier whose output enters a differential input exponential amplifier (DSX-AMP). *Because the DSX circuit uses a single voltage power supply, the input must be biased. This biasing is provided by the VOCM buffer driving the MID node (figure 7.3(b)). Two capacitors level shift the ground referenced preamplifier output from ground to the DC value established by VOCM. Without internal biasing, the user would have to DC bias the inputs to the DSX circuit externally. If not done carefully, the biasing network can introduce additional noise and offsets. By providing internal biasing, the user is relieved of this task and only needs to AC-couple the signal into the DSX⁵.*

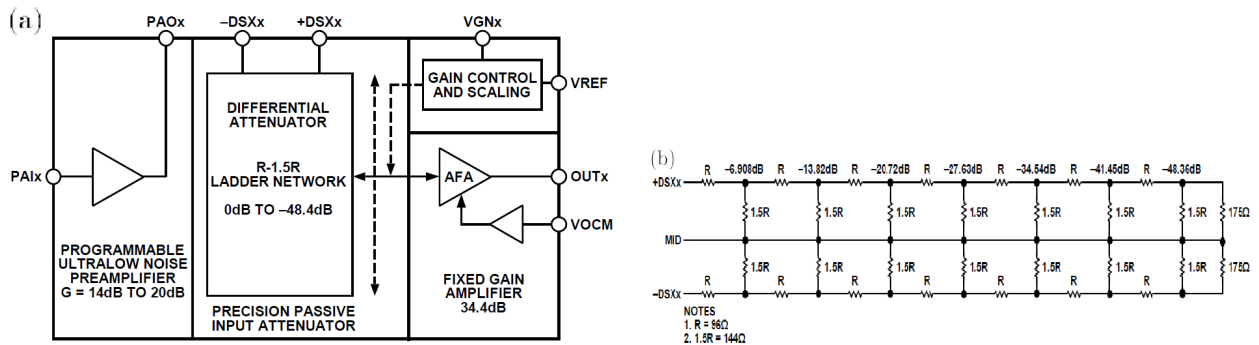


Figure 7.3: (a)Functional block diagram of the AD604. The PAO pin is AC-coupled into the DSX+ pin and the DSX- pin is AC-coupled to ground. (b) Representation of the dual ladder network. Both figures are from the AD604 data sheet.

This is a major observation: because of this particularity, not only the eventual DC offset

⁵Information from the AD604 data sheet.

is suppressed by the AC-coupling (there is thus no need for an offset compensation afterwards) but also the AC-coupling must be made very carefully. In future design, there is no use to include a summing amplifier circuit. This could save a lot of space and, furthermore, reduce the noise (we would reduce the numbers of resistors affecting the signal). For our first trials, the AC-coupling was imperfect leading to tremendous problems: the difference in biasing was greatly amplified and outputs were continuously saturated because of this undesirable offset. This phenomenon was particularly noticeable with higher gain trials as shown on figure 7.4.

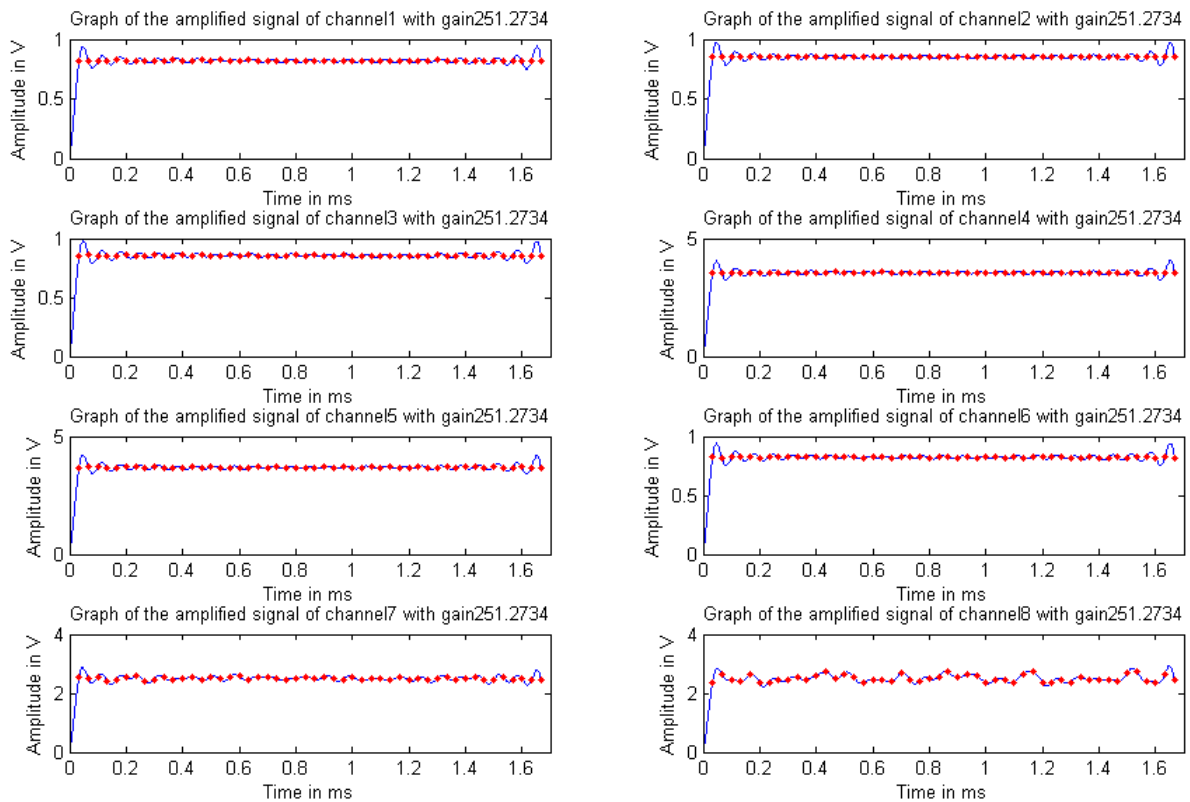


Figure 7.4: Graphs to show the differences in DC bias levels between DSX+ and DSX-. All amplifiers have the same V_{OCM} level (midpoint between the supply voltages $\approx 2.5V$), null input and maximum gain. The difference between the DC bias levels is amplified by the differential input exponential amplifier leading to saturation. This saturation can either be up (channels 4 and 5) or down (channels 1, 2, 3 and 6). If there is no difference, the output remains at the V_{OCM} level (channels 7 and 8).

To compensate for this problem, we replaced the defective capacitors responsible for this

difference. The capacitor to be changed is the one responsible for the AC-coupling to DSX+ if the saturation is down, and the one responsible for the AC-coupling to DSX- if the saturation is up. After replacement, the problem was solved as shown on figure 7.5.

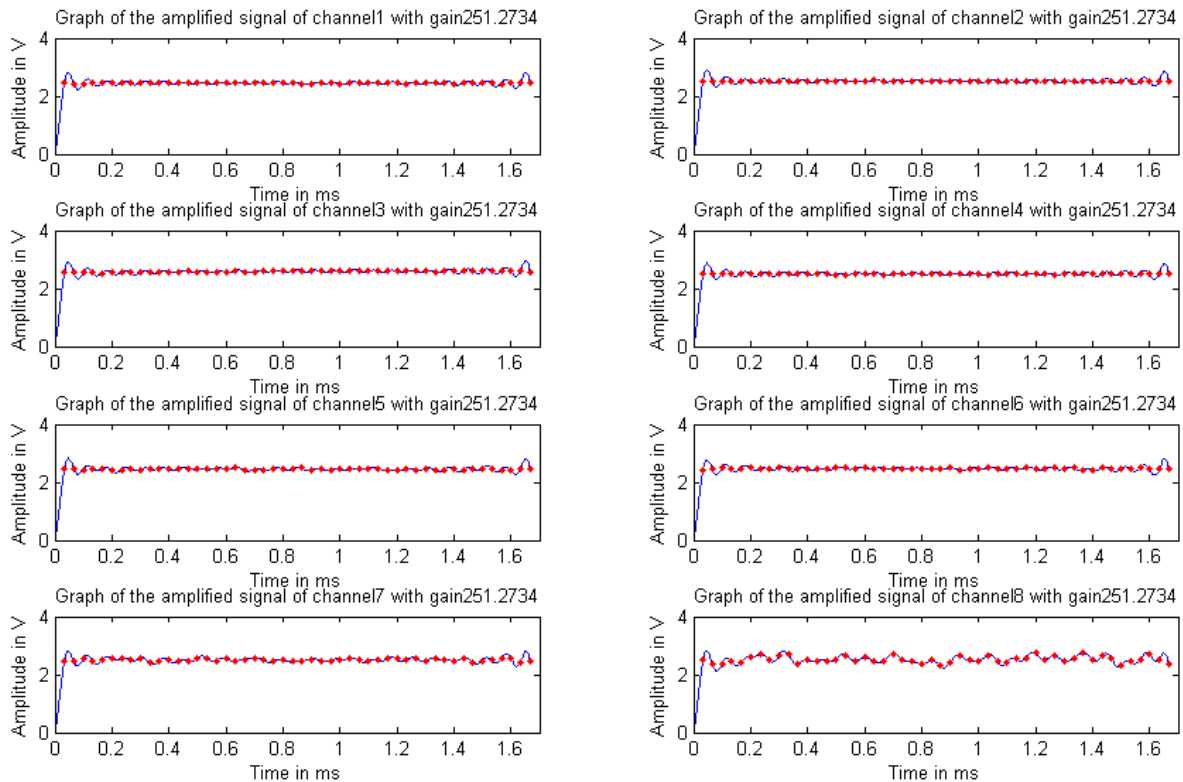


Figure 7.5: Graphs to show the correction for the differences in DC bias levels between DSX+ and DSX-. All amplifiers have null input and maximum gain. The difference between the DC bias levels is minimal because, even with great amplification, there is no level shifting. Saturation is not any more generated by this undesirable offset.

7.2.3 TimerA toggle mode function

As already stated in section 4.2, timerA toggle mode function is used to generate the continuous $6MHz$ clock for the ADC. However, this signal is not pulled up from $3.6V$ to $5V$, leading to possibilities for inaccuracy. From practical testings, we can conclude that this is not the case (see figure 7.6) because we get the same kind of results with the continuous external clock or with the timerA toggle mode function.

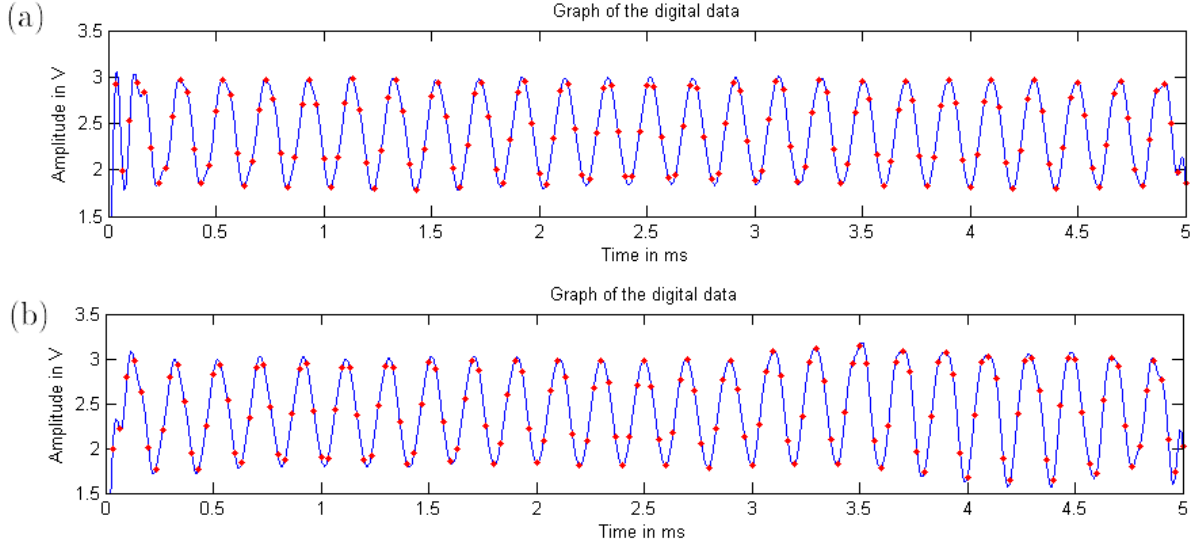


Figure 7.6: Graphs to see inaccuracy introduced by the timerA toggle mode function as continuous clock. Both graphs represent the sampling of a $5kHz$, $100mV_{pp}$ sinus wave with gain of 10. Graph (a) is generated with the external clock source and graph (b) with the timerA toggle mode function.

For the rest of our testing, we use the timerA toggle mode function because it does not degrade the signal and allows us to suppress one function generator or to use it to generate an input signal. In addition, external clock generation is very noisy because it is carried out with banana cables and crocodile clips, leading to great magnetic couplings for the circuit even with the presence of the low-pass filters.

7.2.4 Pseudo-differential versus single-ended inputs

The two situations are represented on figure 7.7. In the single-ended configuration, the source circuit and the measurement are grounded circuit, generating a ground loop. By using the pseudo-differential setting, we bypass the ground loop and avoid having a common mode voltage between the two circuits.

Practical measurements lead to a common mode voltage of $1.325V$ for an DC input signal of $40mV$ and thus an input signal of $1.385V$. Even though this common mode voltage would be filtered by the AC-coupling, it is problematic for the preamplifier because it tolerates a maximum input voltage of $\pm 400mV$. We must thus tie the two grounds together at all times to avoid measuring this common mode voltage. When used with the actual

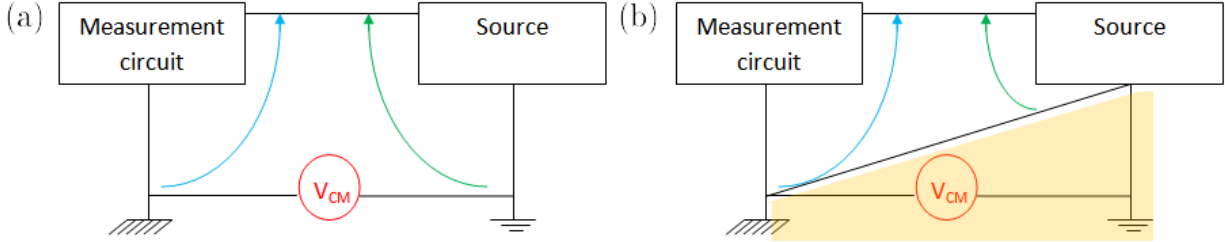


Figure 7.7: Schematics for the two situations. (a) for a single-ended input: source and circuit are tied to “their” ground. (b) for the pseudo-differential input: source and circuit are tied to the same ground. Those schematics are inspired from [34].

probe, the board ground should be tied to the electrode ground.

To keep the board ground and the signal ground separated, we could have tied the COM pins (Signal Ground) of the amplifiers to the external ground. However, this connection is very hard to carry out: due to the very small value of the internal feedback resistors for noise reasons (8Ω and 32Ω nominally), the COM pins need to be connected with as short connections as possible to the ground. Even an excess of 1Ω seriously degrades gain accuracy and noise performance and excessive inductance in this connection can lead to oscillations (AD604’s data sheet).

The best solution to avoid any common mode voltage disadvantages is to use fully-differential inputs. However, this increases the level of noise at the outputs of the amplifiers. Another convenient solution would be to have one of the two circuits floating, i.e. not tied to “its” ground to allow for bias adjustments.

7.2.5 Summing amplifiers

As discussed in section 7.2.2, the summing amplifier circuit is unnecessary because of the AC-coupling compulsory for the functioning of the low-noise amplifiers. For this reason, the analog inputs for the offset compensation are tied to ground for all our testings except the one for the eighth channel to show how the process could be used. Moreover, this circuit introduces a saturation level we did not expect: the low-noise amplifier’s output ranges from $2.5 - 1.5V = 1V$ to $2.5 + 1.5V = 4V$ which constitutes a first reduction (40%) from our study in chapter 3. The second saturation level is introduced by the operational amplifier and diminishes further more the output voltage available: the output voltage swing ranges from $0V$ to $V_{CC} - 1.5V = 3.5V$. Thus the saturation limit for the upper side is diminished by 60% from our expectations. A representation of these upper and lower limit is given in figure 7.8.

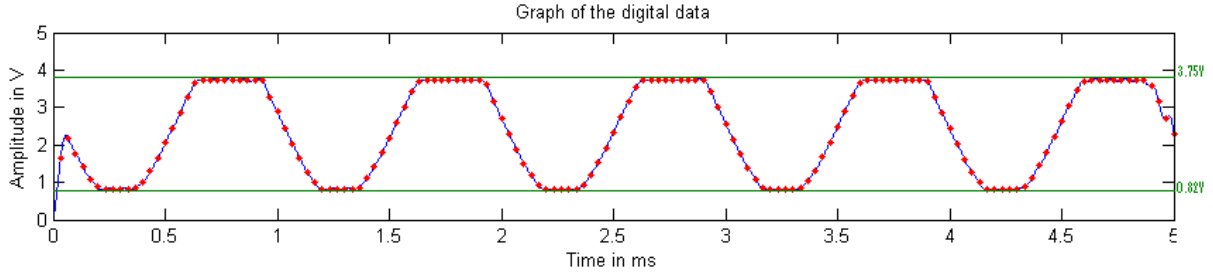


Figure 7.8: Upper and lower limits set by the two amplifiers in cascade for a $1kHz$, $800mV_{pp}$ sinus wave amplified by gain 5. The low-noise amplifier sets the lower limit at approximately $1V$ as well as an upper limit at $4V$. This upper limit is further more reduced by the operational amplifier to approximately $3.5V$.

Thanks to the fact that the DC offset is eliminated, those saturation limits do not introduce a very big performance reduction. Indeed, an amplified signal that reaches those limits is way bigger than the noise component. The only restriction introduced is to limit the gain for bigger signals. For weak signals, even the maximum gain keeps outputs away from the limits.

7.3 Results for the wired design

In this part of the testing, we evaluate the performance of our design with the wired connection. One eZ430-RF2500T target board constitutes the link between our board and the eZ430-RF USB debugging interface connected to the COM port. Sampled data and gains applied are displayed on the HyperTerminal window and converted into a graph via the MATLAB[®] software.

As stated previously, because of memory limitations, we are not able to record the signal for a long period of time. The period of observation is longer for a single channel and, therefore, we analyse the performance in this case. Only the period of observation differs for eight channels and thus conclusions for a single channel can be broadened to eight channels recordings.

7.3.1 Analysis of a single channel

Amplitude limits In this section, we determine what is the lower limit in amplitude for the input signal that still allow us to recognize the signal after processing. Testings

are performed with a $1kHz$ sinusoidal wave. Amplitudes down to $1mV$ are generated by the TG2000. Beyond this limit, the divider described in section 7.1.2 is used. The upper curves on figure 7.10 presents the upper limit in amplitude ($800mV_{pp}$) set by the low-noise amplifier and a $5mV_{pp}$ signal amplified with maximum gain in the nominal operating range. The two signals are reconstructed almost perfectly.

For a $1mV_{pp}$ signal, figure 7.10(c), (d) and (e) illustrates the noise introduced by the divider. Curve (c) is computed numerically and represents the curve we should obtain. Curve (d) is the one obtained with a sinusoid generated by the TG2000 and with the maximum gain in the nominal operating range. The signal is recognizable but not amplified enough to surpass the noise level by a significant factor. Curve (e) represents the same situation except the sinusoid is generated by the divider. As expected, we get a much more noisy signal. The main tendency is still detectable but amplification of the noise perturbs our measure a lot.

For smaller amplitude signals, we use a bigger gain of 446: this is the maximum possible gain but it is out of the nominal operating range. All signals are generated by the divider and the level of noise is thus very high. From figure 7.11, we observe that the noise rapidly surpasses the signal of interest. Indeed, for a $800\mu V_{pp}$ signal, we can recognized the sinus shape, but for smaller amplitudes, the noise is too significant respectively to the signal.

A representation of the superposition of curves computed numerically and curves reconstructed from digital data for the entire amplitude range is given in figure 7.12. From this figure, we again observe that the divider introduces huge amount of noises when comparing the two curves for a $5mV_{pp}$ signal with or without the divider. As expected, the signal component decreases respectively to the noise component with a reduction in amplitude of the input signal.

For curves in the left column, this is due to an increase in gain that amplifies the noise by a greater amount while keeping the signal components quasi identical (amplitude diminishes and gain augments). The input signal noise is supposed to be proportional to the amplitude of the input signal and thus a reduction of the input signal also attenuates the noise. However, the amplifier noise, constant for all gains, is also amplified and its contribution is greater if the gain goes up. To those noise contributions, we must add the noise generated by the ADC, DAC and operational amplifier plus the noise generated by passive components. These noises remain constant and have therefore a greater impact on small amplitude amplified signals than on signals almost reaching the saturation limits.

For curves in the right column, the amplitude is very low and the divider becomes compulsory. In this column, the gain attains its upper limit (446). For a fixed gain, the noise component is not increased (in fact, it should decrease with a reduction in amplitude) but

the signal component weakens leading to this same observation (reduction of the signal component relatively to the noise component with reduction in amplitude) but for another reason. Those observations are represented graphically on figure 7.9.

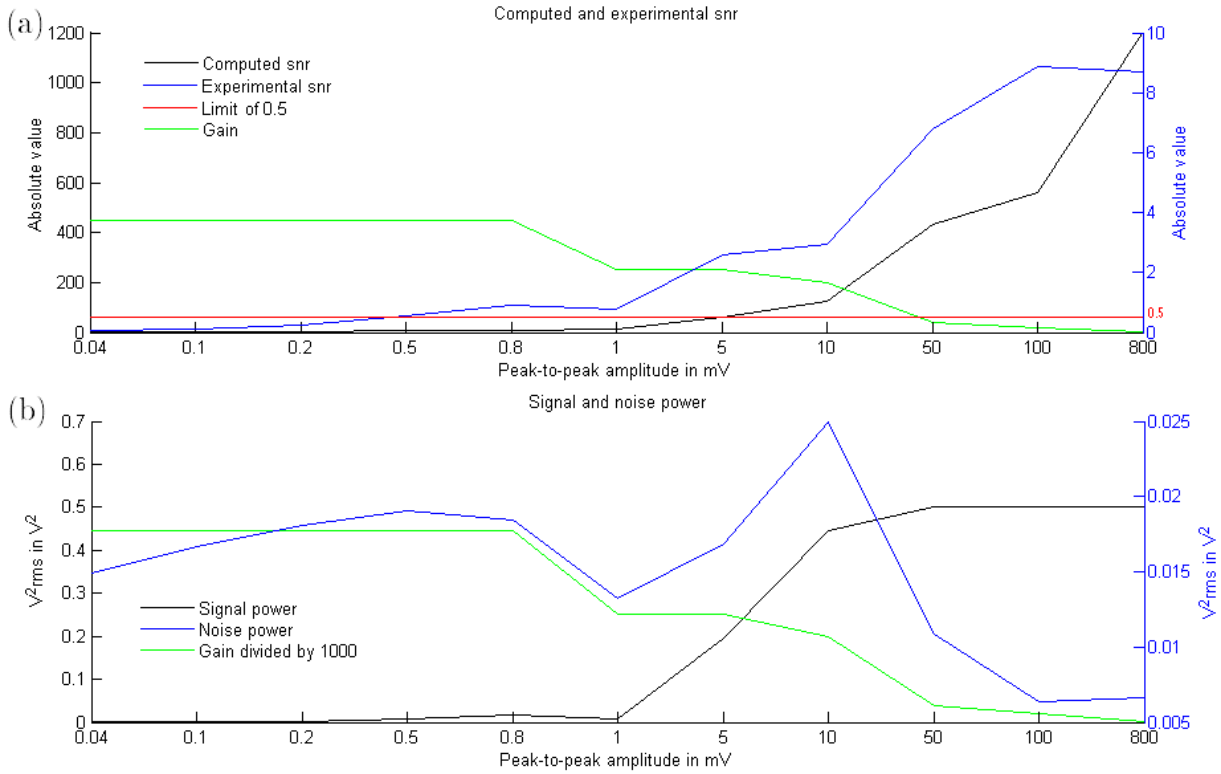


Figure 7.9: Variation of snr with reduction of input signal amplitude based on data given in appendix B. Graph (a) shows curves for snr computed in chapter 3 in black, for snr computed from experimentation in blue, for the lower limit of 0.5 in red and the gain in green. Axis on the left applies to the black and green curves and axis on the right to the blue and red curves. Graph (b) shows curves for signal and noise power expressed in root mean square: the black curve is for the signal power and the blue curve for the noise power. In green, the gain divided by a factor 1000 is represented. Axis on the left applies to the black and green curves and axis on the right to the blue curve.

Curves (a) show the snr resulting from computation in chapter 3 and resulting from experimentation. The two curves follow the same tendency (an augmentation of snr with an augmentation of input signal amplitude) but with two orders of magnitude difference. The second graph shows the signal and noise components. For low amplitude signals (below $1mV_{pp}$), the noise component is almost stable because the gain is fixed: only the augmen-

tation of input signal amplitude modifies the noise. The noise component should decrease considerably with a reduction of the gain and it is indeed observed except for the $5mV_{pp}$ and $10mV_{pp}$ input signals. On the contrary, the signal component varies accordingly to the signal amplitude for low amplitude signal and is almost stable for higher amplitudes. The *snr* component is deduced from those two graphs: for low input signals, the signal component augments more rapidly than the noise component with an augmentation of amplitude, whereas for high amplitude signals, the signal component is almost stable and the noise component diminishes with the gain. From this graph, we see that even a $500\mu V_{pp}$ signal presents an *snr* higher than 0.5 and this sets the ultimate limit.

Frequency and waveform type limits This part of the analysis focuses on detecting the frequency limits. As a reminder, action potentials vary in frequency from $100Hz$ to $6kHz$ and we designed our board to be able to handle signals ranging from $100Hz$ to $10kHz$. Testings are performed on a $100mV_{pp}$ sinusoid with gain 20 and are represented on figure 7.13. One can observe that reconstructed curves are very close to those numerically computed. Filters in our project are thus correctly handled. A small difference in sampling points is observed because both the MSP430 and TG2000 generator can present a frequency inaccuracy. For the square signal⁶, we obtain what we expect, i.e the general square shape but high frequency transitions are smoothed by the low-pass filters and the static phases are influenced by the high-pass filter.

Active offset compensation This section shows how the offset compensation works. As explained previously, this part of the board should be suppressed in future designs but the use of an offset compensation could be used for other purposes. The signal observed is a $100mV_{pp}$, $1kHz$ sinusoid with a DC offset of $50mV$ amplified by a gain of 10. Three curves are shown on figure 7.14. As expected, the DC level without offset compensation is $2.5V$ and any offset compensation modifies this DC level without affecting the rest of the signal. The active offset compensation is thus functional even if it is of no utility for us.

Variable gain: digital processing method This part of the study explores the variable gain computation. Figure 7.15 shows different strategies to adapt the gain. Curves (a) show that the strategy considered in chapter 3 is not suitable for our application: because we only consider the last value and not the maximum and minimum past values, the gain value is continuously revised and do not create a nice curve. This observation encouraged us to let go this solution for another simpler one, the one examined in section 5.2. The choice of the fraction of gain modification is primordial. From curves (b) and (d), we deduce that the factor $1/10$ is acceptable for high amplitude signals but gives poor results for low amplitude signals. However this factor has the advantage to reach a stable gain value very fast. From curves (c) and (e) we see that a factor $1/100$ manages a better trade-off

⁶A square signal is composed of an infinity of frequency.

between accuracy and settling rapidity. Nevertheless, better results for low amplitudes signals are necessary and a factor 1/1000 is considered for curve (f). This seems appropriate for this kind of signals but would lead to a too long period of settling for high amplitude signals. Our strategy for gain adaptation seems to be acceptable but amelioration could be made by adapting the factor to the signal amplitude. This point is treated in the next section.

Variable gain: keyboard action This section analyses results obtained by implementing the strategy developed in section 5.2.4. The user is able to choose the gain modification: 1/10, 1/100 or 1/1000 and augmentation or reduction. This method allows to get a more accurate gain but takes a longer period for the gain to stabilize. Indeed, the gain is changed only once by sampling period because UART interrupts are disabled during UART transfer of data and, depending on the accuracy desired, it takes more or less sampling periods (see figure 7.16) to get the final gain, whereas in the previous section, gain was settled in a single sampling period. Choice between the two methods results from a trade-off between rapidity and accuracy.

A solution for future work would be to combine the two previous methods to get an algorithm entirely ruled by software but capable of the same accuracy as the keyboard interaction method. This algorithm would consider more than one value to adapt the gain (for example, the last three hundreds samples to ensure to cover an entire period, even for the slowest frequency) and a procedure similar as in section 3.7.3. This was not possible in the present project due to limited processor resources.

7.3.2 Analysis of eight channels

All the observations made in the previous section can be broadened to the analysis of eight channels recorded simultaneously. The only difference is the length of the time period, which is shorter. The amplitude and frequency limits are the same as well as the active offset compensation behavior. For the variation of the gain, the two strategies developed previously are possible and adapted to each channel particularly. However, the gain is always adapted once per period and is based on the last sampled value which leads to even poorer results. For this reason, the last strategy (keyboard interaction) is preferred and development of a new gain adaptation method, as suggest in the last chapter, is primordial.

Different signals This section shows that each channel evolves independently both in gain and frequency. The possibility of a channel perturbing inductively or capacitively the others is eliminated. Figure 7.17 presents results for the recording of eight channels with all the same gain and input except channels 3, 5 and 8 which have a null input. We observe that the null inputs are not perturbed by the signal inputs and can conclude that

the magnetic isolation is well performed. Figure 7.18 displays results for a variation for both gain and frequency. From this figure, we see that each gain is treated independently.

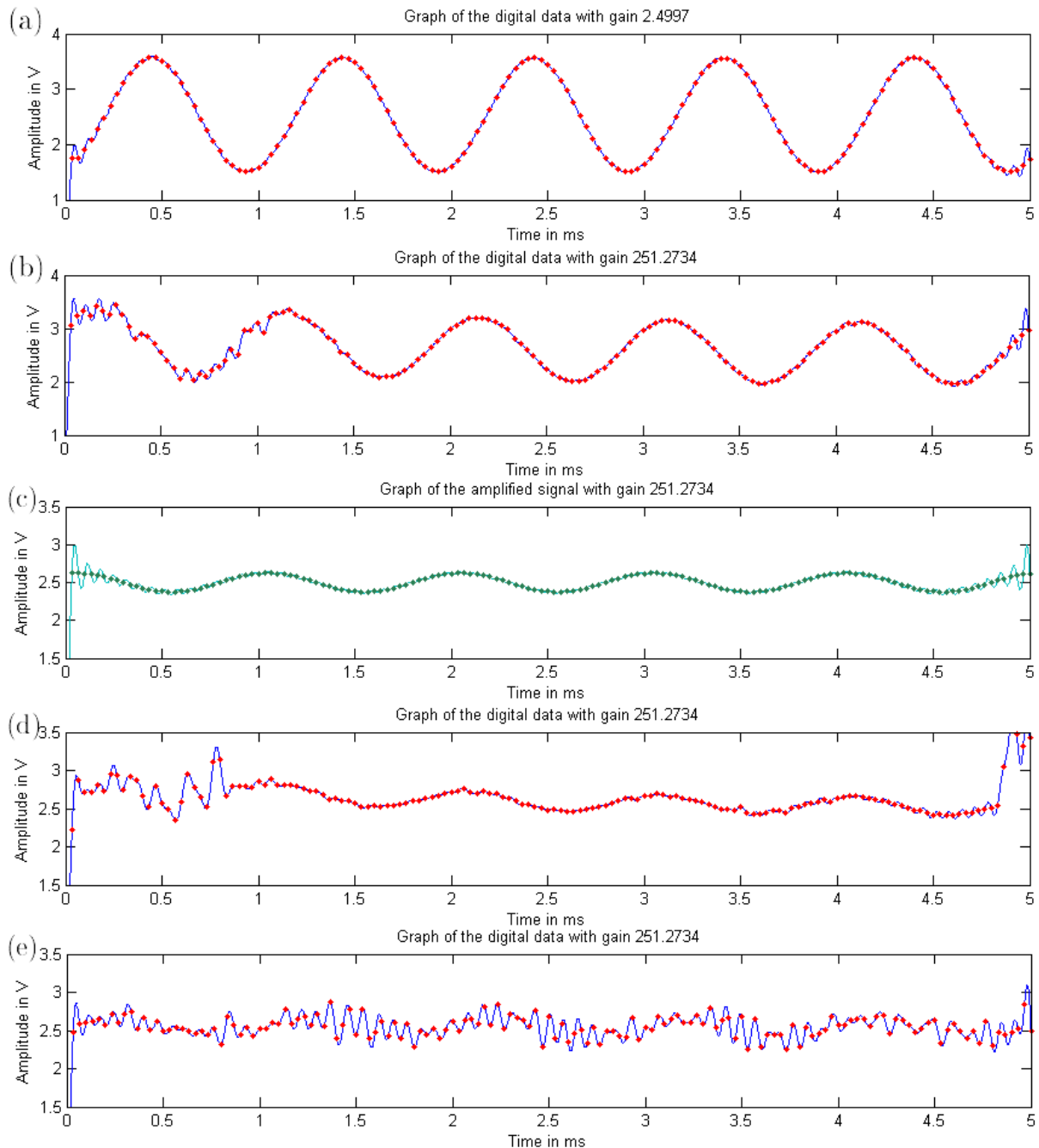


Figure 7.10: (a) Upper limit in amplitude ($800mV_{pp}$) for the AD604 amplified by a gain of 2.5. (b) $5mV_{pp}$ signal amplified by the maximum gain in the nominal operating range (251). (c), (d) and (e) graphs for $1mV_{pp}$ sinusoid. (c) represents the graph we should obtain for a gain of 251; (d) represents the reconstruction for a sinusoid generated by the TG2000; (e) represents the reconstruction for a sinusoid generated by the divider.

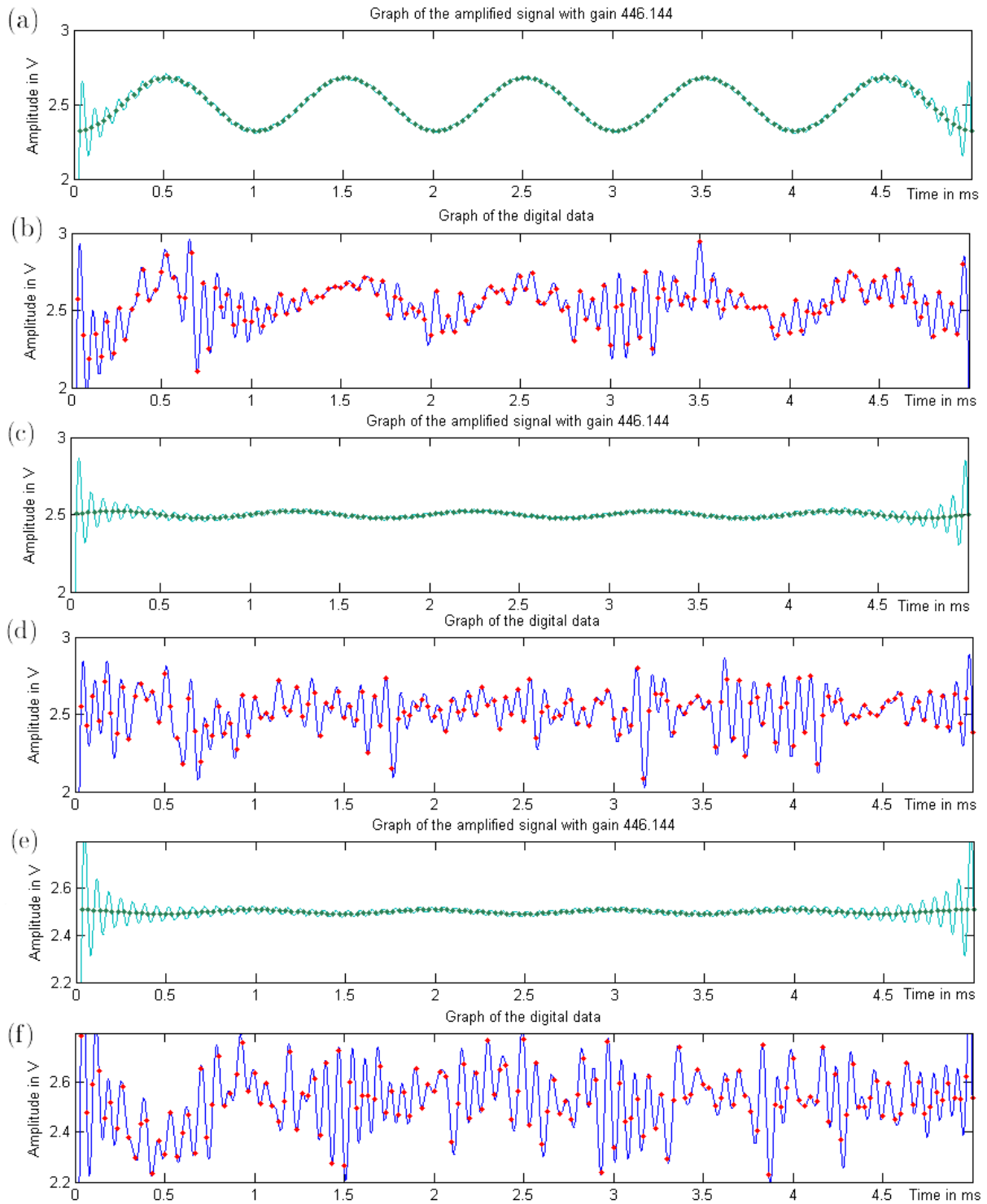


Figure 7.11: Curves for signal with amplitude below $1mV_{pp}$. (a), (c) and (e) are curves computed numerically and represents what we should get. (a) and (b) are for a $800\mu V_{pp}$ sinusoid; (c) and (d) for a $100\mu V_{pp}$ sinusoid; (e) and (f) for a $40\mu V_{pp}$ sinusoid.

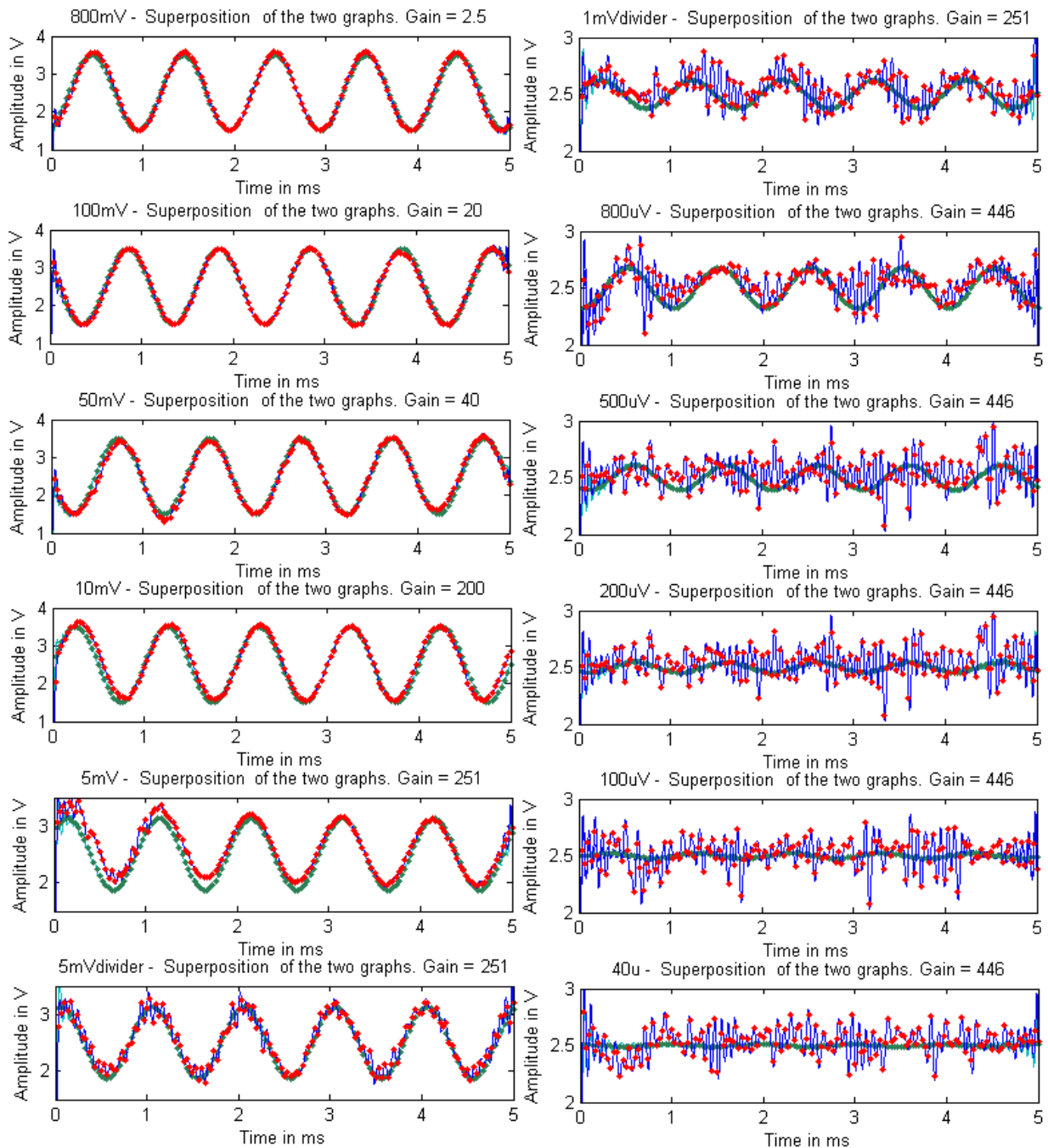


Figure 7.12: Superposition of curves computed numerically (in green) and curves reconstructed from digital data (in red and blue). With the reduction in amplitude, the signal component diminishes respectively to the noise component. Gain increases with a reduction of amplitude.

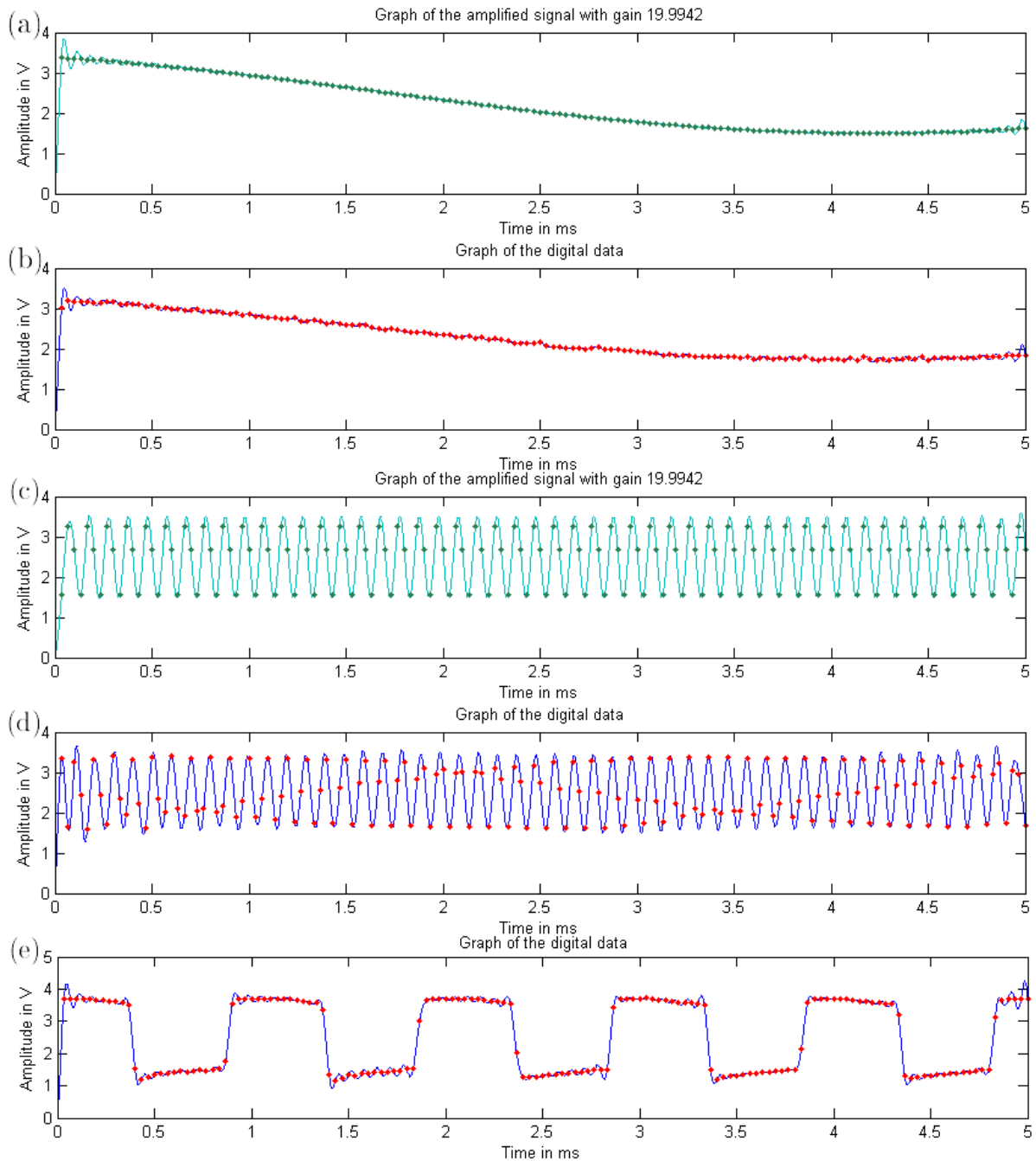


Figure 7.13: Curves for $100mV_{pp}$ sinusoid with gain 20. (a) and (c) are curves computed numerically and represents what we should get. (a) and (b) are for a $100Hz$ sinusoid; (c) and (d) for a $10kHz$ sinusoid; (e) is for a $100mV_{pp}$, $1kHz$ square signal.

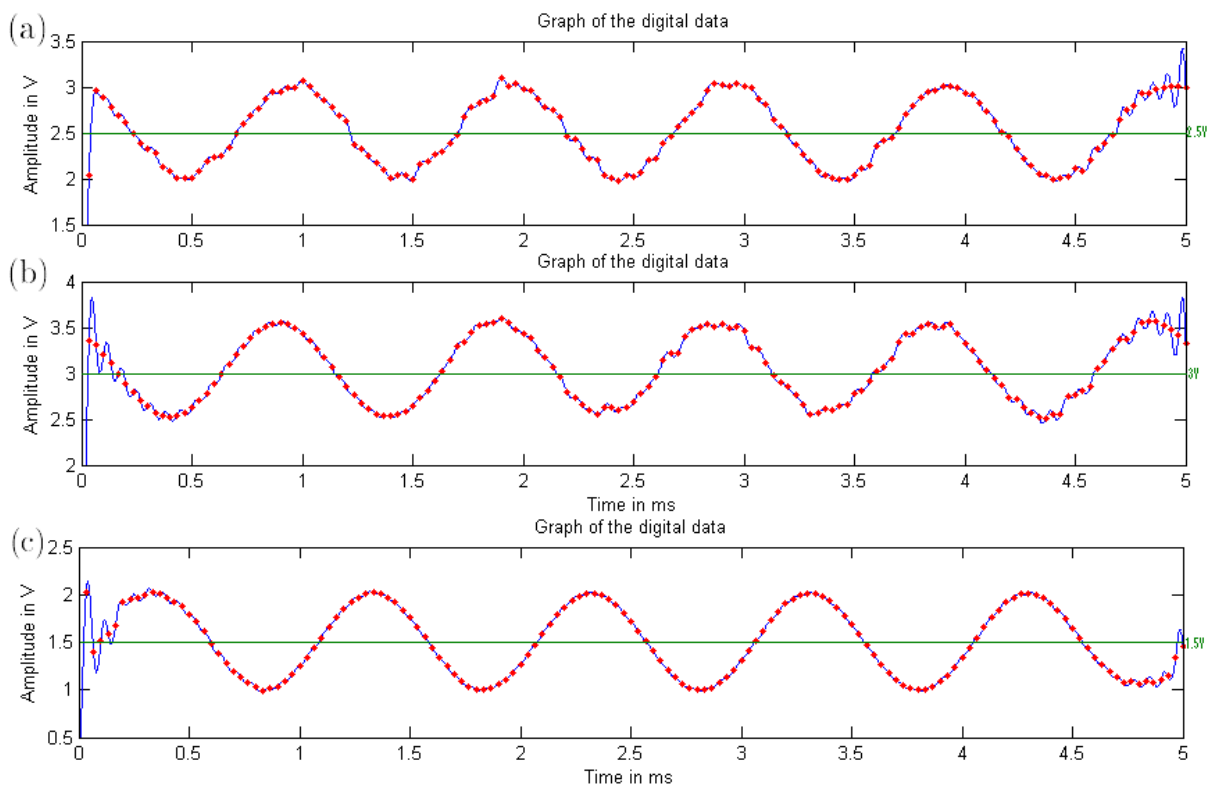


Figure 7.14: Curves for $100mV_{pp}$, $1kHz$ sinusoid with a DC offset of $50mV$ amplified by a gain of 10. (a) without offset compensation; (b) with offset compensation of $0.5V$; (c) with offset compensation of $-1V$. The DC level is indicated in green.

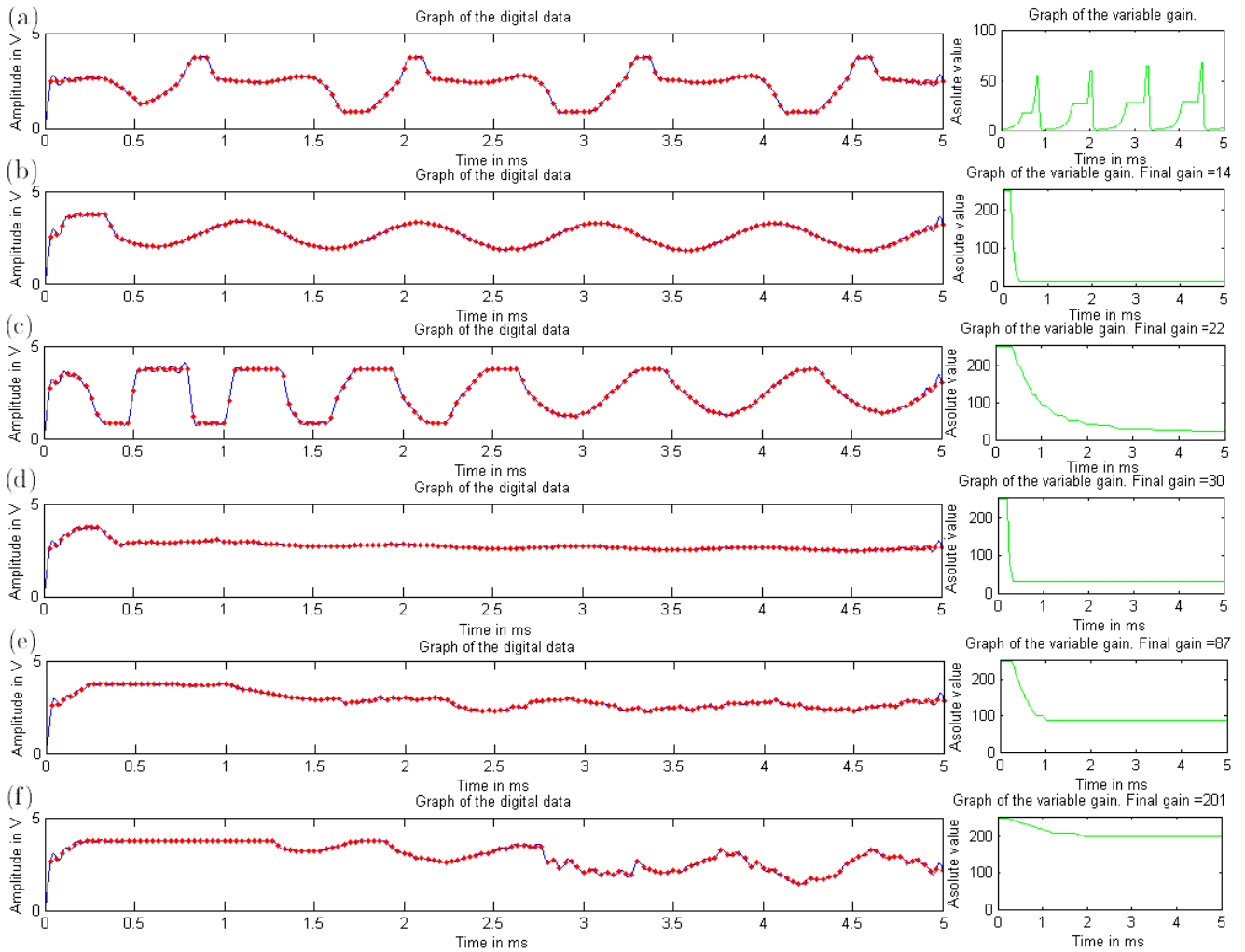


Figure 7.15: Curves for variable gains. Curves on the left represent the reconstructed signals and curves on the right the gain evolving with time. Curves (a) display results for strategy developed in chapter 3; other curves display results for strategy developed in section 5.2. Curves (a), (b) and (c) are for a $100mV_{pp}$, $1kHz$ sinusoid. (b) is for a modification of the gain by $1/10$ and (c) by $1/100$. Curves (d), (e) and (f) are for a $5mV_{pp}$, $1kHz$ sinusoid. (d) is for a modification of the gain by $1/10$, (e) by $1/100$ and (f) by $1/1000$.

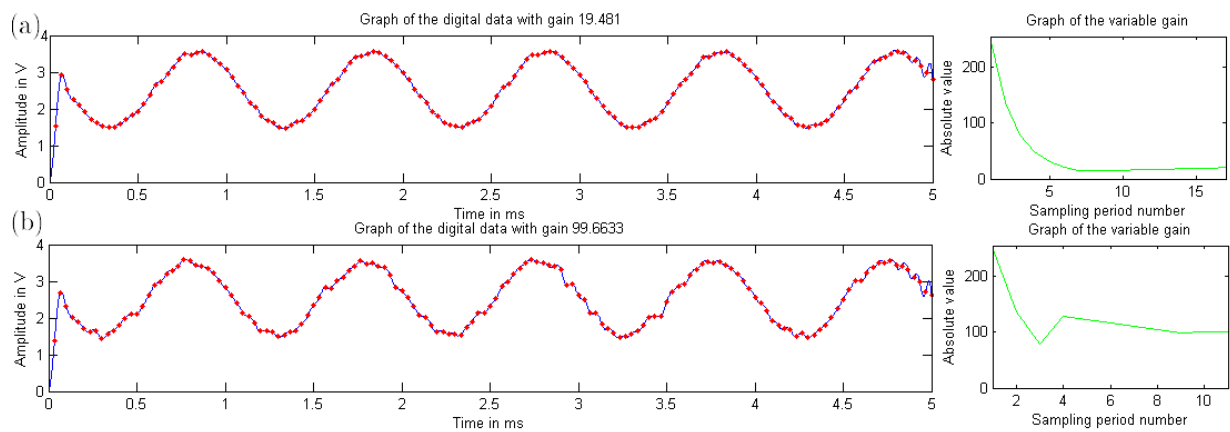


Figure 7.16: Curves for variable gains with keyboard interactions. Curves on the left represent the reconstructed signals with stable gain and curves on the right the gain evolving with the sampling periods. Curves (a) display results for a $100mV_{pp}$, $1kHz$ sinusoid; curves (b) are for a $20mV_{pp}$, $1kHz$ sinusoid.

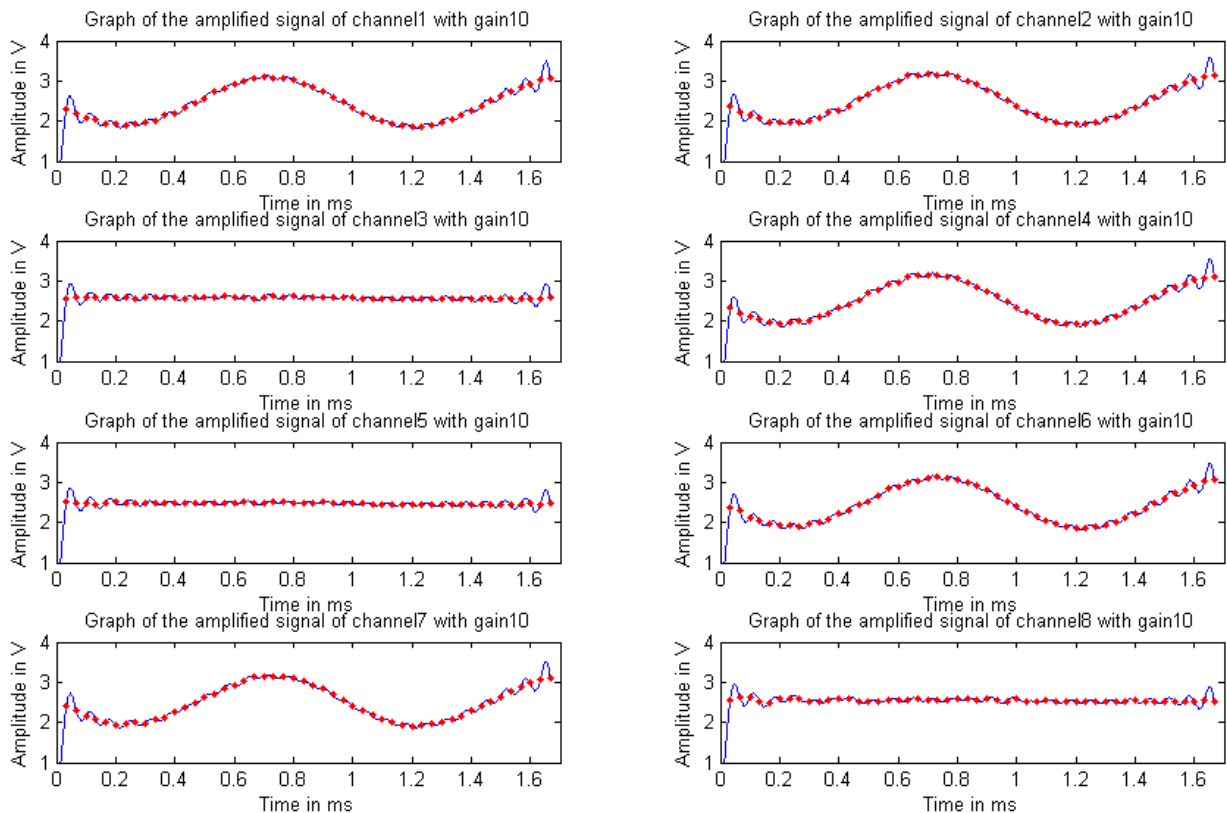


Figure 7.17: Curves for all eight channels with same gain and frequency. Channels 1, 2, 4, 6 and 7 have a $100mV$, $1kHz$ sinusoid as input. Channels 3, 5 and 8 have a null input. All channels present a gain of 10.

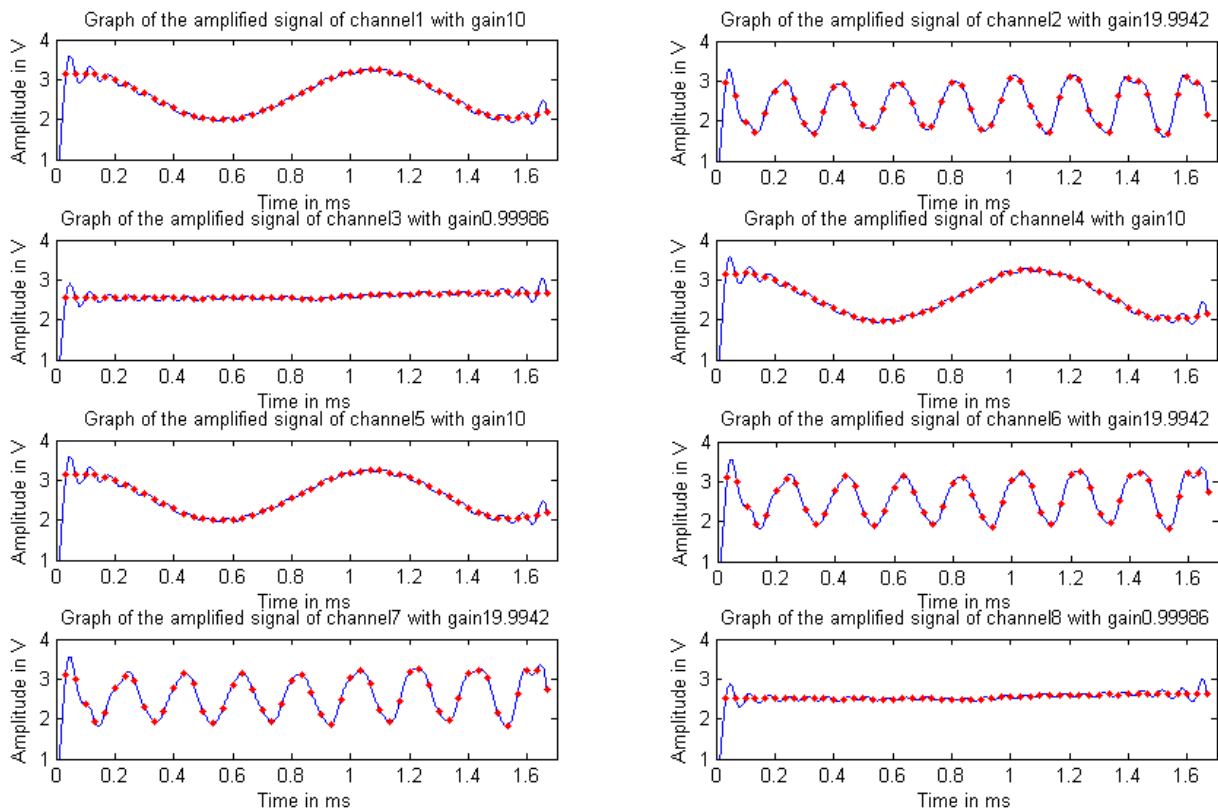


Figure 7.18: Curves for all eight channels with different gains and frequencies. Channels 1, 4 and 5 have a 100mV , 1kHz sinusoid as input with gain 10. Channels 2, 6 and 7 have a 50mV , 5kHz sinusoid as input with gain 20. Channels 3 and 8 have a null input with minimum gain (1).

7.4 Results for the wireless design

Results for this part of the project are similar to those for the wired connection. Indeed, neither the software nor the hardware change much. The power supply for the board is the same as previously: $5V$ provided by an USB cable. For the eZ430-RF2500T target board connected to our board, $3.6V$ supply is generated from $5V$ by a resistor divider. The wireless receptor connected to the PC can be either in its plastic enclosure or not, without affecting results.

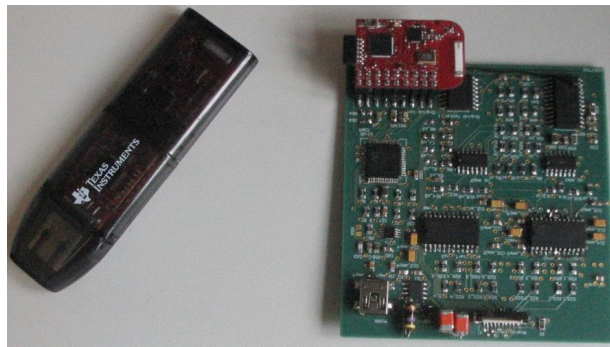


Figure 7.19: Picture of the board with its wireless receptor in its plastic enclosure.

7.4.1 Static levels

Figure 7.20 shows that static levels for all channels are the same as in the wired case. This level is the midpoint between the supply voltages $\approx 2.5V$. We can therefore expect that the references for both the ADC and DAC are the same as before and the accuracy we get is not changed.

7.4.2 Analysis of a single channel

This case is very similar to the one in section 7.3.1 and analyses previously made applied here as well. Figure 7.21 shows two gain adaptations, one for a $100mV_{pp}$ signal and one for a $5mV_{pp}$ signal. Results are exactly the same as for wired testings for both the rapidity of gain settling and accuracy.

7.4.3 Analysis of eight channels

For this case, the time period is even shorter than in the wired configuration: from $1.7ms$, it diminishes to $1.2ms$. It comes from the fact that, in the wireless case, new variables are needed to handle the SimpliciTITM network protocol and capacities for memory are

reduced. Figure 7.22 shows sampling of signals with different amplitudes, frequencies and gains. The same conclusions as for figure 7.18 can be made.

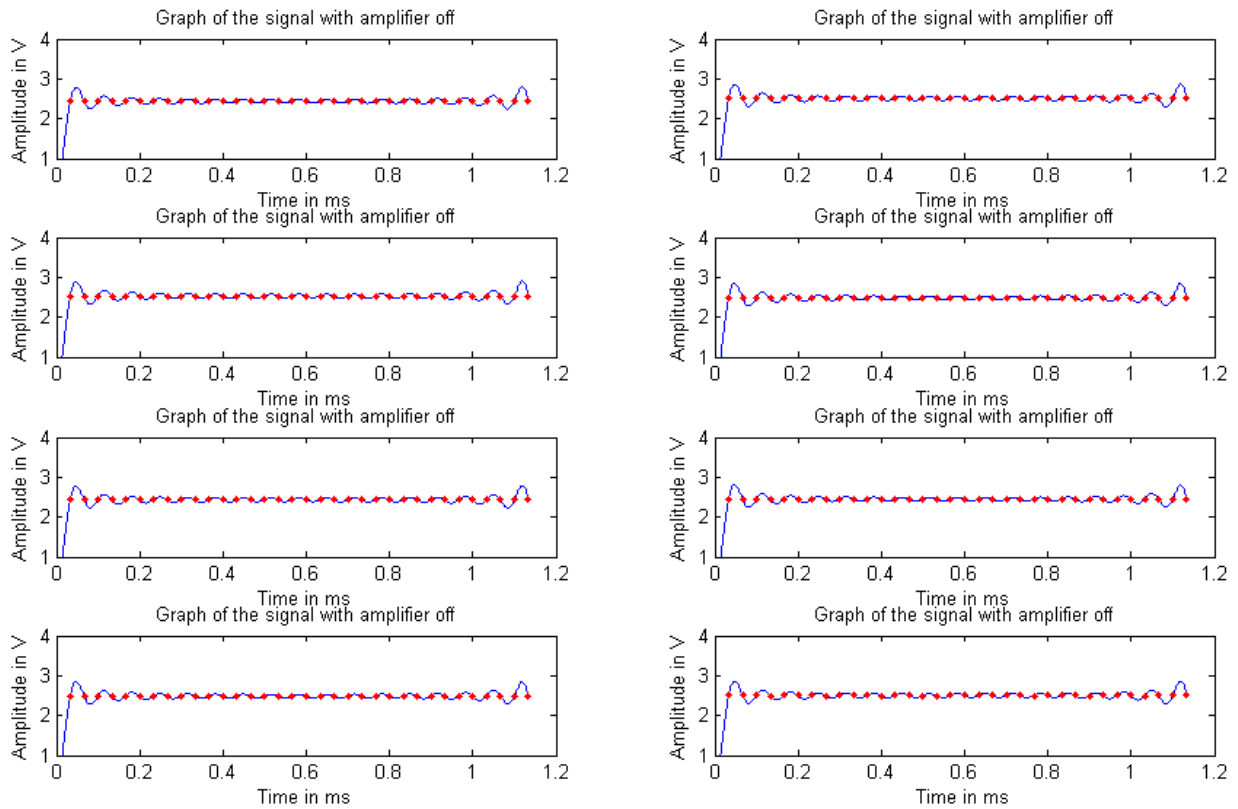


Figure 7.20: Static levels for all eight channels. Amplifiers are turned off by connecting the VGN pin to ground.

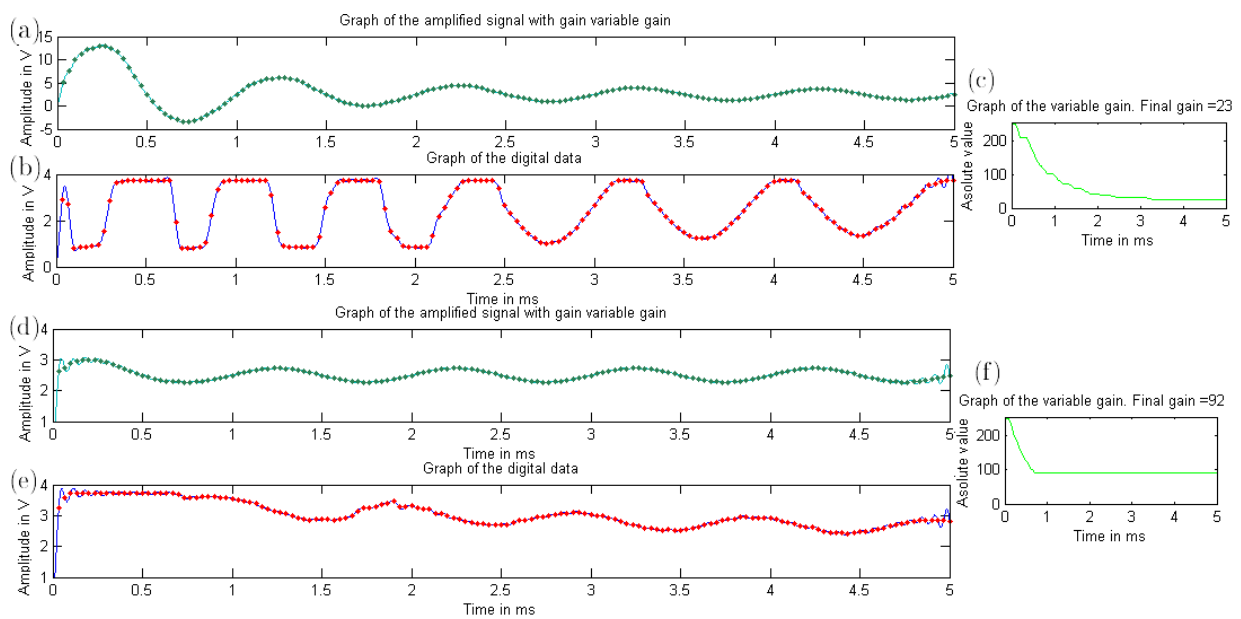


Figure 7.21: Curves for variable gains in the wireless configuration. Curves on the left represent the numerically computed signals and the reconstructed signals, and curves on the right, the gain evolving with time. Curves (a), (b) and (c) display results for a $100mV_{pp}$, $1kHz$ sinusoid. Curves (d), (e) and (f) display results for a $5mV_{pp}$, $1kHz$ sinusoid. The strategy for gain variation is the one developed in section 5.2 with a factor $1/100$.

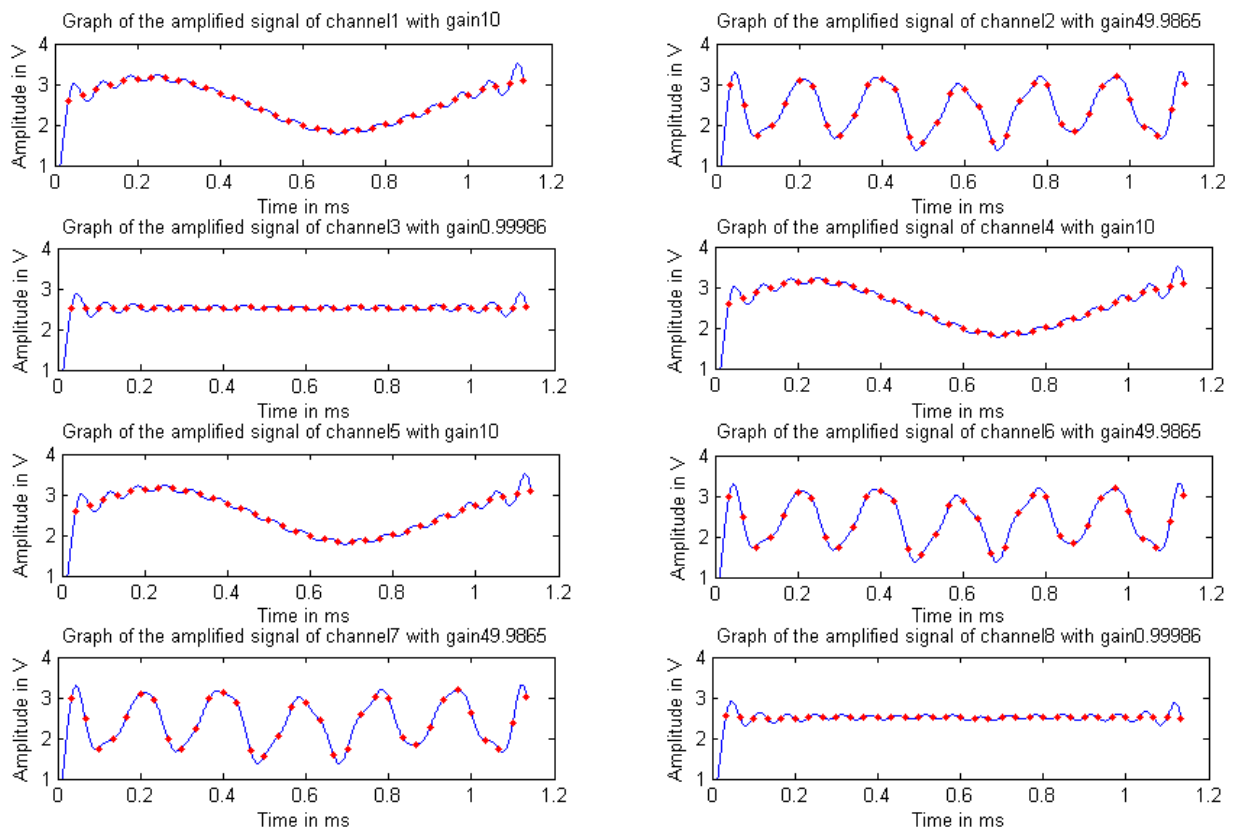


Figure 7.22: Curves for all eight channels with different gains and frequencies in the wireless configuration. Channels 1, 4 and 5 have a $100mV$, $1kHz$ sinusoid as input with gain 10. Channels 2, 6 and 7 have a $20mV$, $5kHz$ sinusoid as input with gain 50. Channels 3 and 8 have a null input with minimum gain (1).

7.5 Conclusions

From this performance analysis we know that we get very good results for both wired and wireless configurations for signals with amplitude higher than $1mV_{pp}$. When the amplitude goes lower, our design's performance rapidly decrease and the sinus shape is barely recognizable below $800\mu V_{pp}$ (an *snr* analysis sets the lower limits at $500\mu V_{pp}$). However, the setting to generate low amplitude signals is very noisy and might explain partly noisy results. Furthermore, in future designs, accuracy could be gained by suppressing the summing amplifier circuit which is unnecessary.

Our design handles frequency variations very properly and can cover the entire range of action potentials frequency. Gain variation is available with either a stand-alone digital processing method or with user's control through keyboard and achieves satisfactory results for both accuracy and rapidity.

Time duration of a sampling period is very limited, especially for eight channels recordings and could be augmented by boosting the UART communication, the SPI communication, or even the two. In addition, this would lead to a reduction of the time period between two sampling intervals.

The wireless communication does not introduce performance limitations. The RSSI we get with or without the plastic enclosure is above 50% for a radius of two meters around the wireless receptor (neural applications typically need less than one meter) and decreases very slowly with distance (a range of fifty meters is expected from specifications).

Chapter 8

Conclusion

This chapter closes the present work. It opens with a brief summary of what has been done during the project and summarizes the procedure. A brief overview of the stimulation aspect is given, results and limitations are once again mentioned, and possibilities for future research are proposed.

8.1 Summary

The goal of this master thesis was the realization of a custom multi-channel read-out and stimulation system for neural applications. The BES-group has developed a multielectrode neural probe array for single neuron recording and stimulation. The present work should interconnect with this probe to foresee a closed-loop approach (recording - stimulation - recording) that would allow for adjustment and tuning of stimulation. The major part of the thesis aimed at the analog multiplexing, filtering, and digitization of multiple channels (eight) for the recording using already a miniaturized SMD design style. In addition, adapting the control software in the MSP430 and configuring the wireless network was required.

This thesis begins with a brief historical introduction about medicine, and more specifically about biological signal processing. A description of neural implants is made and each component is detailed: the electrode array, the electronic implant, and the external block. Afterwards, the research environment at the imec research center in the BES-group is explained. Ethical aspects of deep brain stimulation are tackled very briefly. The introduction chapter ends with the description of the study main purpose and the global organization of this report.

The second chapter introduces concepts and terms necessary to understand the project. The nervous system, brain, brain mechanisms, neurons and cell excitability are covered in

this chapter.

The third chapter summarizes theoretical considerations for recording a multi-channel system. The problem is stated as well as validity criteria to accept or refute a design. A brief background on noise and noise computation is given to simplify following computations. Several choices are made in this chapter regarding the electronic components and the handling of the offset compensation. A parameter exploration is performed to accept a final design.

The fourth chapter is the hardware design. Each subcircuit is detailed with its specifications and functions. An analysis of the clock frequency is carried out to ensure the $30kHz$ sampling frequency. The eZ430-RF2500 Development Tool, and the way we use it, are described to conclude the board design. The PCB is conceived with particular attention to signal flow, form factor and analog to digital separation.

The fifth chapter presents different softwares implemented in our application. A clear distinction is made between recording a single channel or eight channels concurrently. Softwares increase in complexity throughout the chapter. Two methods for gain variation are considered: digital processing and keyboard control.

The wireless link design is explained in the sixth chapter. Both the hardware and software adaptations from the eZ430-RF2500 Development Tool are discussed. The network, made of an AP and an ED, is examined as well as specific actions of each eZ430-RF2500 target board.

The last chapters sets the testing procedure with a description of connections and instruments. Choices made previously regarding components and connections are refuted or accepted. A results analysis is performed for both the wired and the wireless configurations. Performance and limitations are deduced.

8.2 Stimulation

This thesis was also supposed to cover the design of the stimulation system for neural applications. Stimulation is achieved by the realization of a bank of current/voltage sources which allow for programmable electrical stimulation. The utility of a recording and stimulation device lies in the possibility of a closed-loop approach.

At present, the stimulation part has not been carried forward. However, the DAC used in the recording design could be reused in the stimulation part. Indeed, the DAC outputs eight channels which output voltage ranges from $0V$ to $5V$. For recording purposes, DAC

outputs are used to set gains independently. If it was to be converted to a component of the stimulation device, DAC outputs would be used as controllers for the current/voltage sources. Programming of those outputs is made by the MSP430 and allows for variation due to either digital processing or interaction with the user through the keyboard. If recording and stimulation are to be done sequentially, the same DAC can be used in the two phases: it sets gains during recording and controls current/voltage sources during stimulation.

DAC outputs can not be directly tied to the electrode array since a finer voltage offset and current flow control is needed. For example, stimulations on figure 1.3 are between $-40\mu A$ and $40\mu A$, and testings on the BES electrodes were performed with pulses of $600\mu A$ during $0.2ms$ at a frequency of $333Hz$ [23].

This part of the project is currently already studied at the imec research center.

8.3 Limitations and future research

As stated in the last chapter, our design is capable of handling a large set of amplitudes and frequencies (the entire frequency range of action potentials is covered) for both wired and wireless configurations. The read-out for eight channels is performed without great modifications from a single channel except for the sampling time period and a very small difference in sampling frequency. Offset compensation is unnecessary due to compulsory high-pass filter at the low-noise amplifier inputs to bias the signal.

However, our board seems incapable of sampling signals below $500\mu V_{pp}$ with an acceptable *snr*. This could result from two reasons: the divider introduced to diminish the input signal amplitude generates a great amount of noise due to the high value resistor and degrades the input signal too much, or/and the board we designed is not capable of achieving limits computed in chapter 3.

To improve the noise ratio of the input signal, a function generator with smaller output range could be used, but this is not an issue for *in vivo* testings. The second amelioration possible concerns the design itself: thanks to the suppression of the summing amplifier circuit, we would gain in noise reduction (suppression of two resistors and an amplifier for each channel).

Gain adaptation with three methods was performed: the first method aimed a too accurate gain adaptation by consecutive reduction and augmentation and was not possible with the very few digital processing available. It led to very poor results and was abandoned. The second method, a simplified version of the first one by allowing only reduction, was tested with different adaption factors. A good trade-off between accuracy and rapidity of gain set-

ting was achieved with a reduction of a factor $1/100$. Those two methods are stand-alone processes and function exactly identically for both wired and the wireless cases. The third method supposes user control thanks to the keyboard. He or she can choose the factor by which the gain should be diminished or augmented. Accuracy for this method can attain a very high level but rapidity is limited because only one adaptation by sampling period is allowed.

Another limitation of our design, to achieve the $30kHz$ sampling frequency when recording eight channels, is the SPI communication with only the ADC during sampling. Gain adaptation is performed only once, at the end of the sampling period. In addition, memory limitations from the MSP430 restrict the duration of the sampling period. This is mostly due to two factors: SPI communication with the ADC is very slow ($6MHz$ and two bytes) and reaches already by itself the limit frequency. The second factor is the very slow UART communication which favors a strategy of sampling, storing, and sending data, where a strategy of sampling and sending is desired. In this project, the baud rate is fixed by the back channel UART but, for further applications, speeding up this communication should be pursued.

Another important factor to be ameliorated is the size of the PCB. Indeed, an implant in the cortex should be as small as possible to limit disagreements. Area on the PCB can be gained by suppressing the two amplifiers, forty resistors and ten capacitors of the summing amplifier circuit. The use of DIP active components and 0201 or 0402 passive components could greatly reduce the total size, as would an IC design. Also, in further designs, the MSP430, RF2500 and antenna should be incorporated directly on the board. A design of a flex-PCB would allow the board to adapt better to its environment and relax size restrictions.

Last but not least, power supply and dissipation should be considered. To allow for sufficient accuracy, a power supply of $5V$ is used. Computation of the supply current reaches almost $500mA$. The needed power is thus close to $2.5W$. This is too much for self-powered or battery-powered implanted devices. Moreover, heat dissipation would damage severely surrounding tissues. Several solutions are possible: limiting devices function in time by, for example, turning off or configuring in low-power mode the DAC and ADC while wireless transfer is performed and *vice versa*. This solution would lead to a great power consumption but only sporadically. Another solution is to look for other components. From table 4.1, we see that low-noise amplifiers are very greedy in power and require more than 50% of the supply current. Replacement by other low-noise amplifiers could be considered. Power supplies mentioned in section 1.2.3 such as air-tissue transformer, battery, or biofuel cell should be studied. Finally, going for an IC design would also greatly diminish energy consumption.

To conclude, the actual design provides already very good functional results in a lot of aspects. Going for a mixed PCB/IC design inspired from observations previously made is now possible and would lead to even better results. Power supply, size and shape of the PCB should be considered for a final prototype before going to a full IC design. The stimulation function is to be added to existing functions and acceleration of UART communication should be foreseen.

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Appendices

Appendix A

Noise

A noise, due to its intrinsic property of being a random signal, is only well represented by its *power spectral density*¹. To define this term, we first need the definition of the *root mean square* value [14]:

$$v_{rms} = \sqrt{\frac{1}{T} \int_{t_0}^{t_0+T} v^2(t) dt} \quad (\text{A.1})$$

where $v(t)$ represents the instantaneous value of the signal, t_0 an arbitrary time and T the time period.

The expression within the radical symbol resembles to a power and for a stationary resistor r , one has:

$$P = \frac{1}{rT} \int_{t_0}^{t_0+T} v^2(t) dt = \frac{1}{r} v_{rms}^2 \quad (\text{A.2})$$

In a frequency zone $[f, f + df]$, the *spectral density* is defined by:

$$v_{sd}^2 = \frac{dv_{rms}^2}{df} \quad (\text{A.3})$$

To retrieve the root mean square in a frequency bandwidth delimited by f_{min} and f_{max} from the spectral density, one uses the following formula:

$$v_{rms}^2 = \int_{f_{min}}^{f_{max}} v_{sd}^2 df \quad (\text{A.4})$$

The definition of the SNR is:

$$SNR \equiv \frac{P_{signal}}{P_{noise}} \quad (\text{A.5})$$

¹This entire section is based on [34].

In the case of a stationary resistor, one can define the voltage SNR by the ratio of the power dissipated by a resistor thanks to equation A.2:

$$SNR \equiv \frac{P_{signal}}{P_{noise}} = \frac{v_{rms,signal}^2}{v_{rms,noise}^2} \quad (\text{A.6})$$

and from this definition, one can introduce the square root of the SNR:

$$snr \equiv \frac{v_{rms,signal}}{v_{rms,noise}} \quad (\text{A.7})$$

Thus, in our case, we only need to compute the root mean square of the noise or, giving the same result eventually, its spectral density. For a white noise, the power spectral density is constant and its root mean square can be easily evaluated:

$$v_{rms}^2 = \int_{f_{min}}^{f_{max}} v_{sd}^2 df = v_{sd}^2 [f_{max} - f_{min}] \quad (\text{A.8})$$

$$v_{rms} = v_{sd} \sqrt{f_{max} - f_{min}} = v_{sd} \sqrt{B} \quad (\text{A.9})$$

where B is the bandwidth in which the noise is measured.

The computation of the root mean square of the signal is much tougher. Indeed, we do not have a real input signal from which the computation is a direct application of formula A.1. The signal shape is represented in figure A.1(a). From this figure, we see that a correct approximation of each spike is a triangular signal. The formula to compute the v_{rms}^2 of a triangular signal of amplitude V_0 (see figure A.1 (b)) is:

$$\begin{aligned} v_{rms}^2 &= \frac{1}{T} \int_{t_0}^{t_0+T} v^2(t) dt \\ &= 2 \frac{1}{T} \int_0^{T/2} \left(V_0 \frac{2}{T} t \right)^2 dt \\ &= 2 \frac{1}{T} \frac{4}{T^2} V_0^2 \frac{t^3}{3} \Big|_0^{T/2} \\ &= \frac{8}{T^3} V_0^2 \frac{T^3}{8 * 3} \end{aligned} \quad (\text{A.10})$$

$$v_{rms} = \frac{V_0}{\sqrt{3}} \quad (\text{A.11})$$

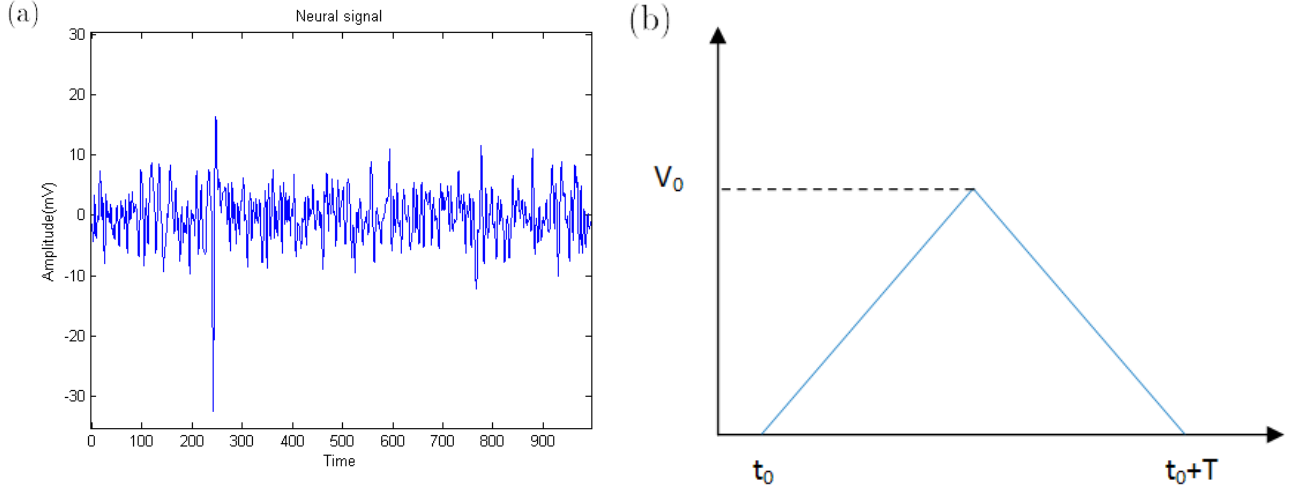


Figure A.1: (a) Representative cortical recording traces. (b) Representation of a triangular signal.

Eventually, to sum up several noises, we need the following theorems [34]:

Theorem 2. *When several (uncorrelated) noise sources add up in a circuit, root mean square voltages add up quadratically.*

Theorem 3. *Any amplifier circuit, as complicated it might be, is characterized by two noise parameters:*

- E_b : the noise electromotive force at the input;
- I_b : the noise current at the input.

E_b is dominant if the source resistance is negligible compared to the input resistance of the amplifier; I_b is dominant in the other case.

Theorem 4. *When several amplifiers are cascaded together, one has:*

$$\begin{aligned}
 v_{rms,noise}^{out} &= G_2 \sqrt{(v_{rms,noise2}^{in})^2 + G_1^2 (v_{rms,noise1}^{in})^2} \\
 &= G \sqrt{\frac{(v_{rms,noise2}^{in})^2}{G_1^2} + (v_{rms,noise1}^{in})^2} \\
 &\cong G v_{rms,noise1}^{in}
 \end{aligned} \tag{A.12}$$

where

G_1 is the gain of the first amplifier

G_2 is the gain of the second amplifier

G is the gain resulting from the cascade of the two amplifiers

$v_{rms,noise1}^{in}$ is the root mean square input noise of the first amplifier

$v_{rms,noise2}^{in}$ is the root mean square input noise of the second amplifier.

This approximation holds true if G_1 is orders of magnitude bigger than $v_{rms,noise2}^{in}$.

Appendix B

Data for signal-to-noise ratio analysis

A MATLAB[®] script computes the signal and noise power from the experimental data. The *snr* is deduced from these previous computations. The signal and noise data are discrete values and their root mean square is given by the following formula:

$$v_{rms}^2 = \frac{1}{T} \sum_{i=1}^T v_i^2 \quad (\text{B.1})$$

where T is the number of discrete data and v_i the data number i .

For the signal, we get:

$$v_{rms,signal}^2 = \frac{1}{T} \sum_{i=1}^T v_{i,S}^2 \quad (\text{B.2})$$

where $v_{i,S}$ represents the discrete data we should get for a given input signal and gain.

For the noise, we get:

$$v_{rms,noise}^2 = \frac{1}{T} \sum_{i=1}^T (v_{i,S} - v_{i,exp})^2 \quad (\text{B.3})$$

where $v_{i,S}$ represents the discrete data we should get for a given input signal and gain and $v_{i,exp}$ the data we got experimentally.

The *snr* is then (from equation A.7):

$$snr = \sqrt{\frac{v_{rms,signal}^2}{v_{rms,noise}^2}} \quad (\text{B.4})$$

From experimental data used to generate figure 7.12, we get table B.1.

Amplitude of the input signal	Gain	$v_{rms,signal}^2$	$v_{rms,noise}^2$	snr
$40\mu V_{pp}$	446	$0.0000V^2$	$0.0149V^2$	0.0517
$100\mu V_{pp}$	446	$0.0002V^2$	$0.0167V^2$	0.1221
$200\mu V_{pp}$	446	$0.0010V^2$	$0.0180V^2$	0.2349
$500\mu V_{pp}$	446	$0.0062V^2$	$0.0191V^2$	0.5712
$800\mu V_{pp}$	446	$0.0159V^2$	$0.0185V^2$	0.9285
$1mV_{pp}$ with divider	251	$0.0079V^2$	$0.0133V^2$	0.7715
$5mV_{pp}$ with divider	251	$0.1973V^2$	$0.0166V^2$	3.4525
$5mV_{pp}$	251	$0.1973V^2$	$0.0290V^2$	2.6069
$10mV_{pp}$	200	$0.4445V^2$	$0.0250V^2$	2.9339
$50mV_{pp}$	40	$0.5001V^2$	$0.0109V^2$	6.7805
$100mV_{pp}$	20	$0.4997V^2$	$0.0064V^2$	8.8645
$800mV_{pp}$	2.5	$0.4999V^2$	$0.0066V^2$	8.6900

Table B.1: Computed data for the snr analysis.

Appendix C

Schematics

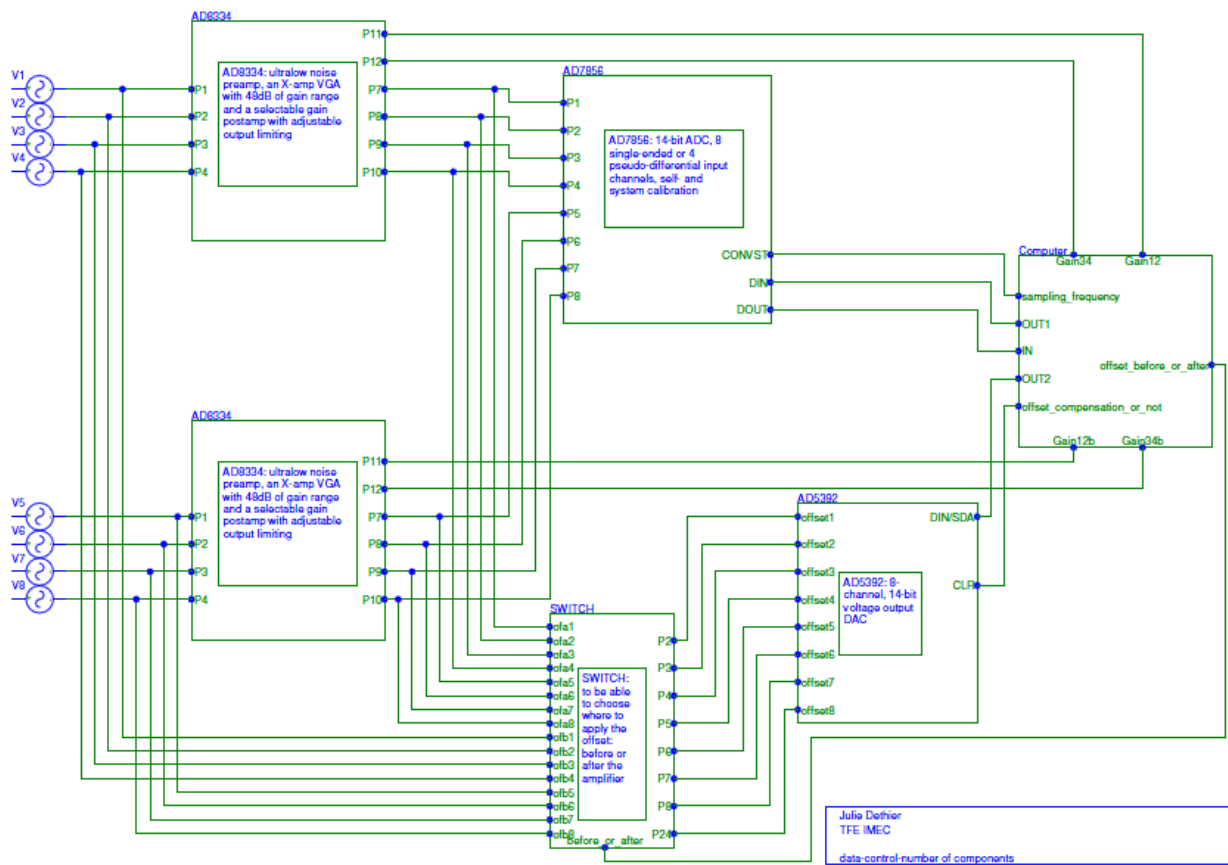


Figure C.1: High level view of the first design.

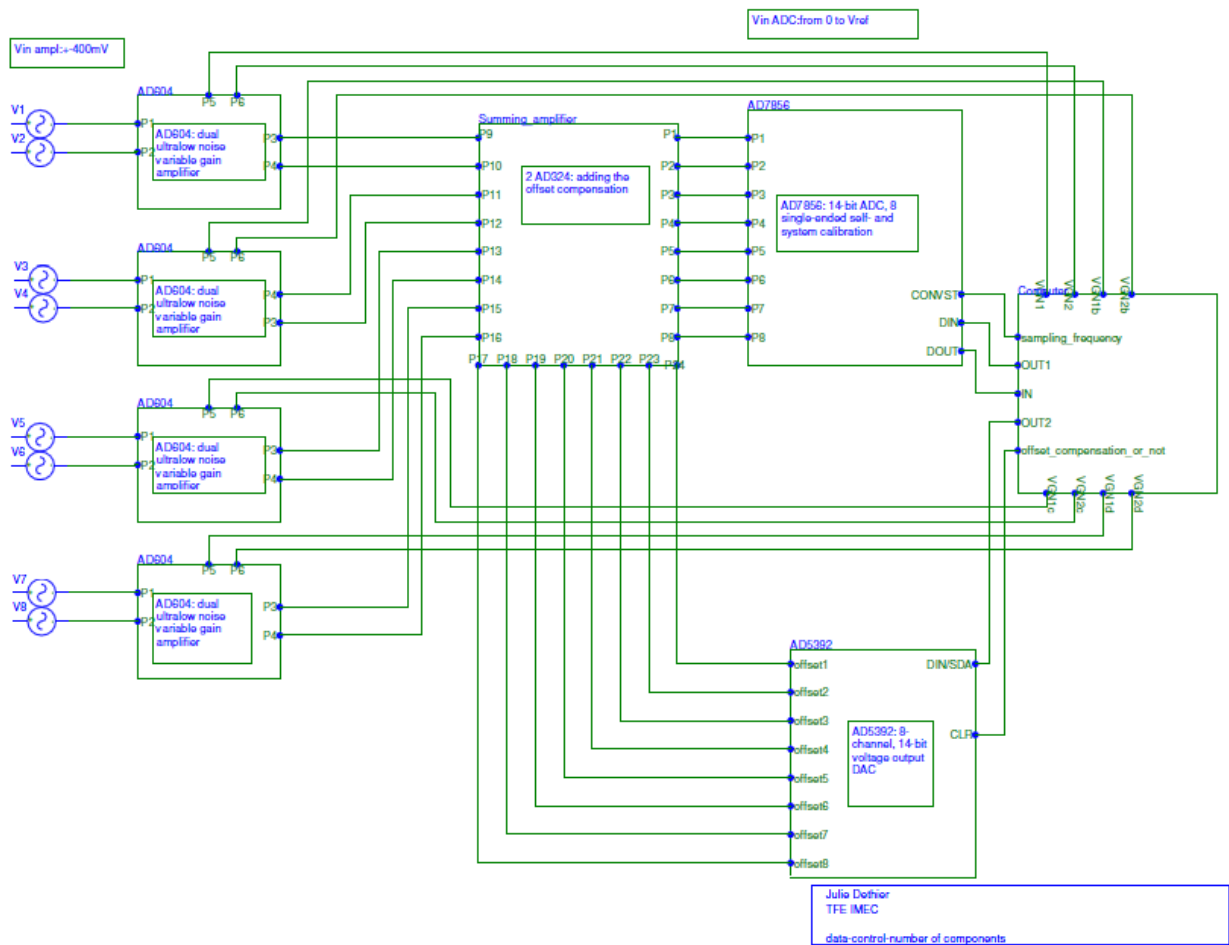


Figure C.2: High level view of the second design.

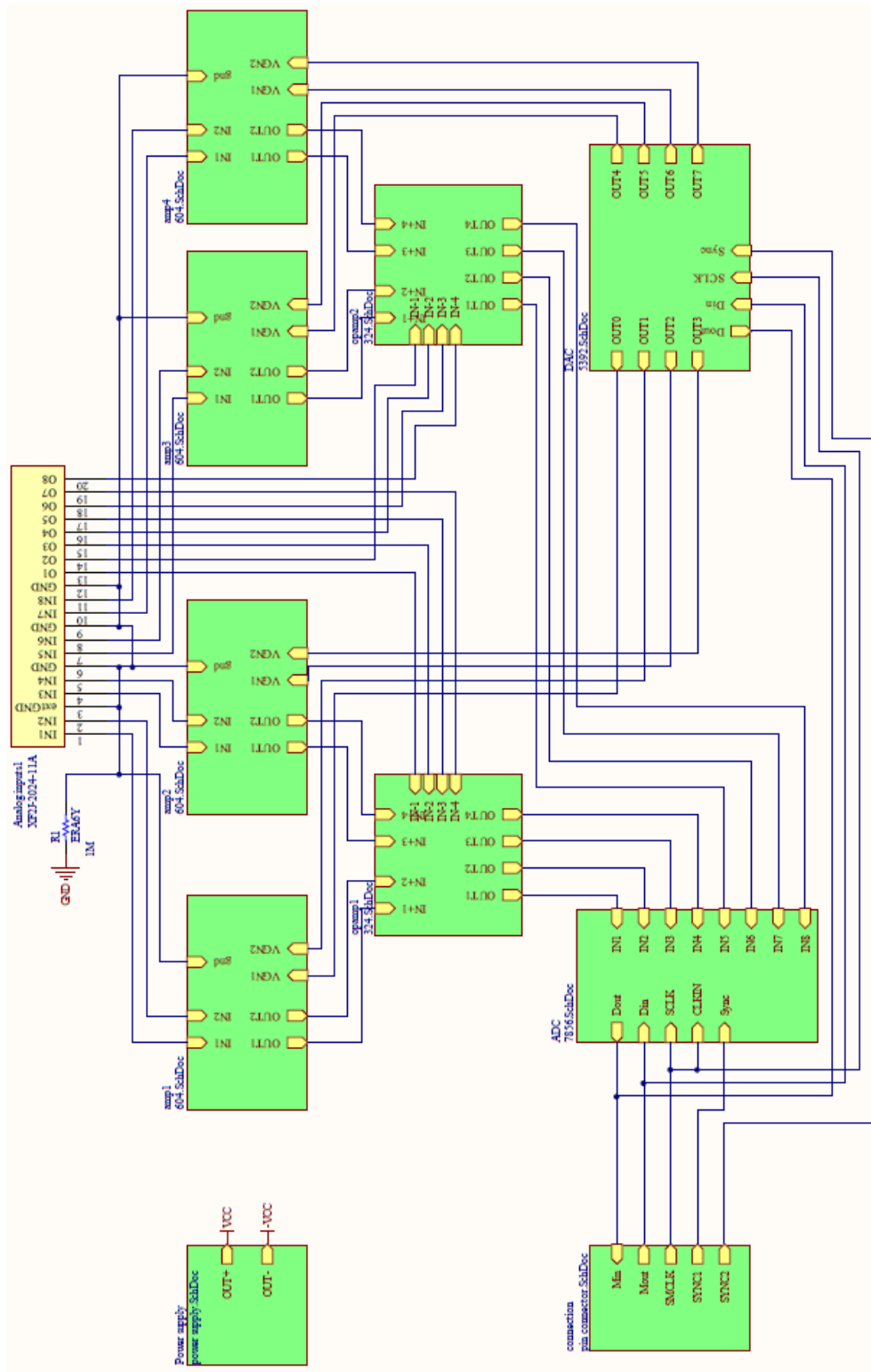


Figure C.3: Schematic of the first PCB.

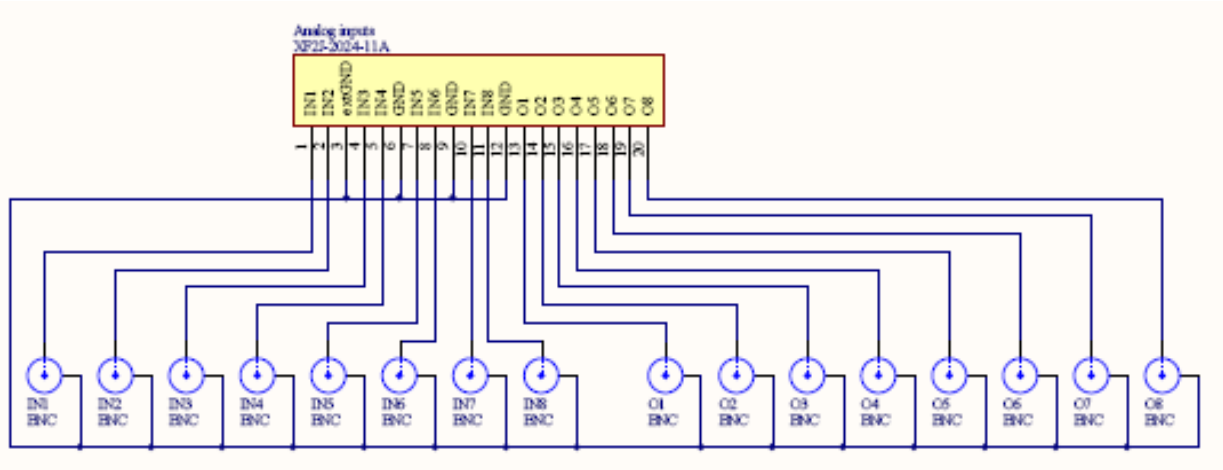


Figure C.4: Schematic of the second PCB.

Appendix E

Components count

	Analog inputs	Power supply	Amplifiers	Operational amplifiers	ADC	DAC	Connectors	Total
Number	1	1	4	2	1	1	1	11
Numbers of active parts for 1 component	1	3	1	1	1	1	2	
Numbers of active parts for all components	1	3	4	2	1	1	2	14
Numbers of R (ERA6Y) for 1 component	1	4	8	20	10	8	4	
Numbers of R (ERA6Y) for all components	1	4	32	40	10	8	4	99
Numbers of C (0805) for 1 component	0	5	10	5	15	11	2	
Numbers of C (0805) for all components	0	5	40	10	15	11	2	83
Numbers of C (1206) for 1 component	0	0	0	0	1	1	0	
Numbers of C (1206) for all components	0	0	0	0	1	1	0	2
Numbers of C (595D) for 1 component	0	2	0	0	0	0	0	
Numbers of C (595D) for all components	0	2	0	0	0	0	0	2
Numbers of diode (ZHCS750) for 1	0	1	0	0	0	0	0	
Numbers of diode (ZHCS750) for all	0	1	0	0	0	0	0	1
Numbers of L (DR125-470-R) for 1 component	0	1	0	0	0	0	0	
Numbers of L (DR125-470-R) for all components	0	1	0	0	0	0	0	1
Total								213

Figure E.1: Table with a components count for our PCB. From this table, we observe that passive components number surpasses active components number by a great amount. This gives us an idea of the PCB size.